

400/200GbE PCS Overview

**Next-generation 200 Gb/s and 400 Gb/s MMF PHYs
Study Group**

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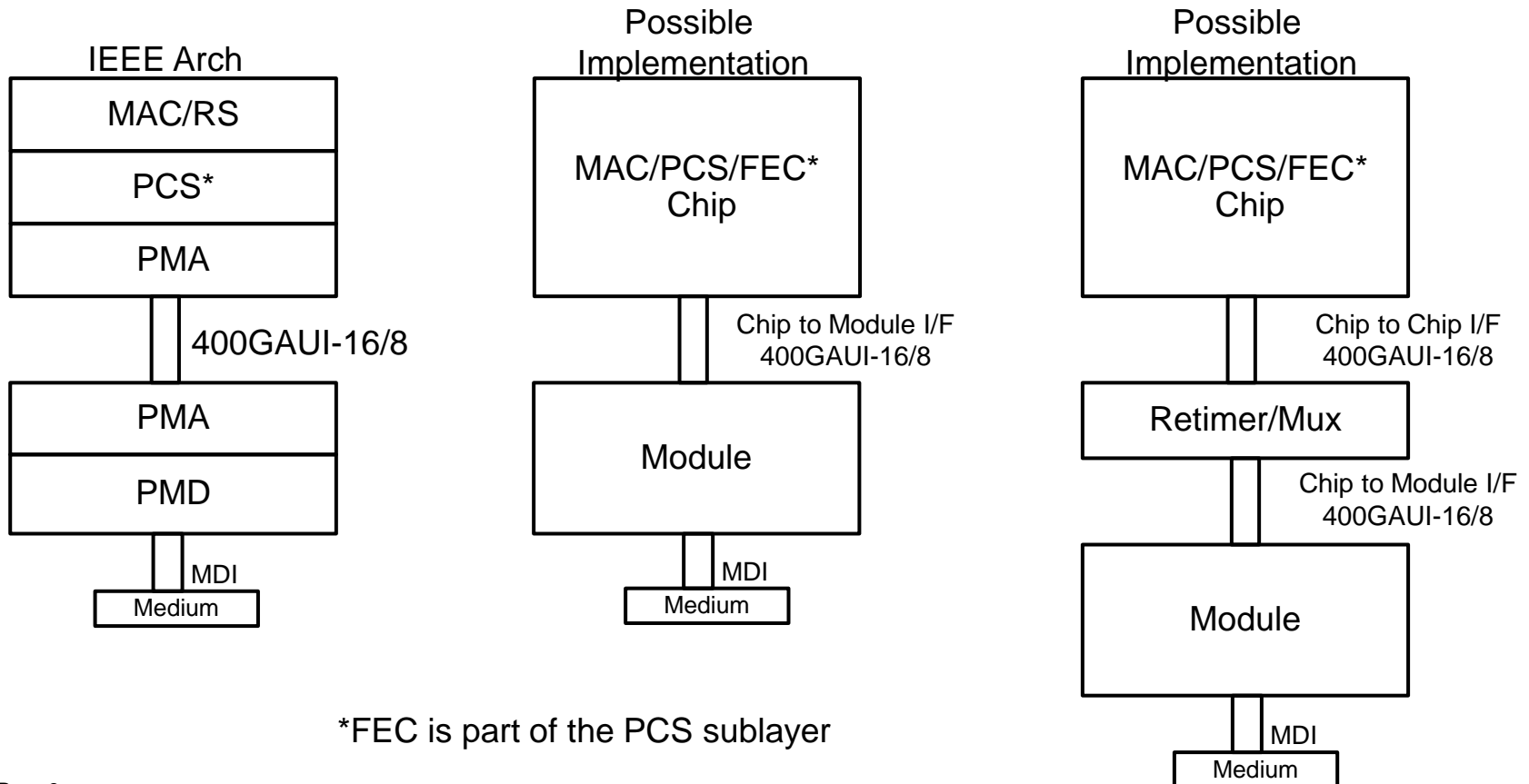
Early draft for consensus building

Introduction

➤ TBD

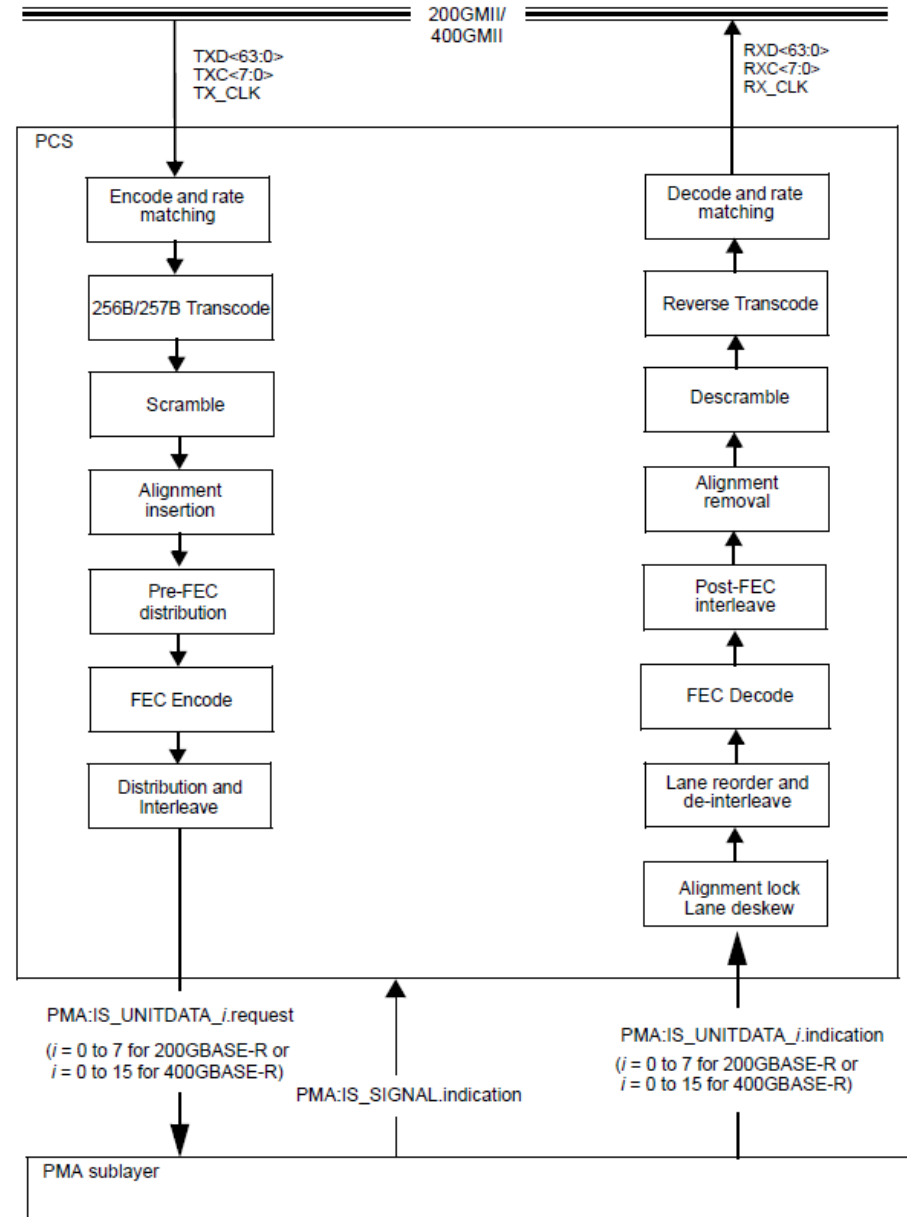
802.3bs Architecture

- Adopted architecture and possible implementations are shown below for 400GbE
 - 200GbE is identical except for # lanes and data rate
- A single FEC is used in the PCS sublayer, RS(544,514) aka KP4 FEC
- An extender sublayer is also defined



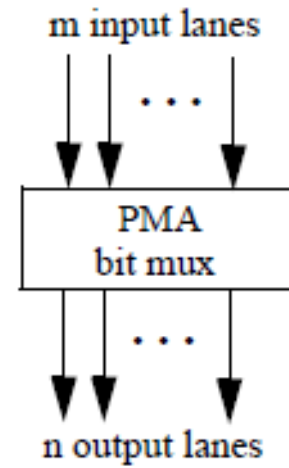
802.3bs PCS

- PCS processing flow is shown in the figure
- The PCS distributes data to 16 PCS lanes for 400GbE and 8 PCS lane for 200GbE



802.3bs PMA

- From a muxing point of view, the PMA is simple, m input lanes are bit muxed to n output lanes
- Bit muxing is blind, lanes can move around, the RX PCS sorts things out
- Clock content and baseline wander simulations have been performed for 1:1, 2:1 and 4:1 muxing scenarios



802.3bs Architecture Applicability to Next Gen MMF

- If it was decided to support 400GBASE-SR4.2 for instance:
 - You have 8 bit streams across the PMD
 - For a 400GAUI-8 you directly connect up electrical lane to optical ‘lane’
 - PCS lanes are 2:1 multiplexed onto each electrical and optical ‘lane’
- The BER budget is split out across AUI interfaces and the PMD budget
 - 1×10^{-5} for the AUI interfaces
 - 2.4×10^{-4} for the PMD interface
 - provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.223) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap
 - The new PMD would need to match these requirements, if they do, then the current 802.3 architecture and PCS is directly applicable to this project

Conclusion

➤ TBD

Thanks!