45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

~~Modify~~ Change reserved register space (1.1809 through 1.32767) in Table 45-3 as shown below

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.1809 through 1.~~32767~~2303	Reserved	
1.2304	BASE-T1 PMA ~~Control Register~~control	45.2.1.130a
1.2305	1000BASE-T1 PMA ~~Status Register~~ status	45.2.1.130b
1.2306	1000BASE-T1 ~~Training Register~~ training	45.2.1.130c
1.2307	1000BASE-T1 ~~Link Partner Training Register~~ link partner training	45.2.1.130d
1.2308	1000BASE-T1 ~~Test~~ test mode control	45.2.1.130e
1.2309 through 32767	Reserved	

45.2.1.130a BASE-T1 PMA ~~Control Register~~ control register (Register 1.2304)

The assignment of bits in the BASE-T1 PMA control register is shown in Table 45–98a.

Table 45–98a—BASE-T1 PMA ~~Control Register~~control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2304.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2304.14:12	Reserved	~~Set to 0s~~Value always 0	~~R/W~~RO
1.2304.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
1.2304.10:5	Reserved	~~Set to 0s~~Value always 0	~~R/W~~RO
1.2304.4	Master/Slave	1 = Master 0 = Slave	R/W
1.2304.3:0	PHY Type	BASE-T1 PHY speed when Auto-negotiation is disabled 0000 = Reserved 0001 = Reserved 0010 = 1000BASE-T1 Else = Reserved	R/W

[a]RO = Read only, R/W = Read/Write, SC = Self clearing

45.2.1.130a.1 ~~BASE-T1~~ Reset (1.2304.15)

Resetting ~~a~~ the BASE-T1 PMA/PMD is accomplished by setting bit 1.2304.15 to a one. This action shall set all BASE-T1 PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the BASE-T1 PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self clearing, and ~~a~~ the BASE-T1 PMA/PMD shall return a value of one in bit 1.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. ~~A~~ The BASE-T1 PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2304.15.

During a reset, ~~a~~ the BASE-T1 PMD/PMA shall respond to reads from register bits 1.2304.15 and 1.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.1.130a.2 ~~BASE-T1~~ Low power (1.2304.11)

~~A~~ The BASE-T1 PMA/PMD may be placed into a low-power mode by setting bit 1.2304.11 to a one. This action may also initiate a low power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the BASE-T1 PMA/PMD. The behavior of the BASE-T1 PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2304.11 is zero.

NOTE—This operation interrupts data communication. The data path of ~~a~~ the BASE-T1 PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

45.2.1.130a.3 ~~BASE-T1~~ Master/Slave (1.2304.4)

When Auto-Negotiation is disabled, this bit is used to configure the BASE-T1 PHY to be master or slave. When set as a one the BASE-T1 PHY is configured to be a master. When set as a zero the BASE-T1 PHY is configured to be a slave. The setting of this bit shall be ignored when Auto-Negotiation is enabled.

45.2.1.130a.4 ~~BASE-T1~~ PHY ~~Type~~ type (1.2304.3:0)

When Auto-Negotiation is disabled these bits are used to configure the BASE-T1 PHY type. The setting of these bits shall be ignored when Auto-Negotiation is enabled.

45.2.1.130b 1000BASE-T1 PMA ~~Status Register~~ status register (Register 1.2305)

The assignment of bits in the 1000BASE-T1 ~~training~~ PMA status register is shown in Table 45–98b.

45.2.1.130b.1 ~~1000BASE-T1~~ OAM ~~Ability~~ ability (1.2305.11)

When read as a one, this bit indicates that the 1000BASE-T1 PHY supports OAM. When read as a zero, this bit indicates that the 1000BASE-T1 PHY does not support OAM.

45.2.1.130b.2 ~~1000BASE-T1~~ EEE ~~Ability~~ ability (1.2305.10)

When read as a one, this bit indicates that the 1000BASE-T1 PHY supports EEE. When read as a zero, this bit indicates that the 1000BASE-T1 PHY does not support EEE.

Table 45–98b—1000BASE-T1 PMA ~~Status Register~~status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2305.15:12	Reserved	~~Set to 0s~~Value always 0	RO
1.2305.11	OAM Ability	1 = PHY has OAM ability 0 = PHY does not have OAM ability	RO
1.2305.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2305.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2305.8	Low-power ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	RO
1.2305.7:3	Reserved	~~Ignore when read~~Value always 0	RO
1.2305.2	Receive ~~Polarity~~polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2305.1	Receive ~~Fault~~fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2305.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LH

[a]RO = Read only, LH = Latching high

45.2.1.130b.3 ~~1000BASE-T1~~ Receive fault ability (1.2305.9)

When read as a one, bit 1.2305.9 indicates that the 1000BASE-T1 PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2305.9 indicates that the 1000BASE-T1 PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.130b.4 ~~1000BASE-T1~~ Low-power ability (1.2305.8)

When read as a one, bit 1.2305.8 indicates that the 1000BASE-T1 PMA/PMD supports the low-power feature. When read as a zero, bit 1.2305.8 indicates that the 1000BASE-T1 PMA/PMD does not support the low-power feature. If ~~a~~ the 1000BASE-T1 PMA/PMD supports the low-power feature, then it is controlled using ~~the low-power~~ bit 1.2304.11.

45.2.1.130b.5 ~~1000BASE-T1~~ Receive ~~Polarity~~ polarity (1.2305.2)

When read as zero, bit 1.2305.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2305.2 indicates that the polarity of receiver is reversed.

45.2.1.130.6 1000BASE-T1 Receive ~~Fault~~ fault (1.2305.1)

When read as a one, bit 1.2305.1 indicates that the 1000BASE-T1 PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2305.1 indicates that the 1000BASE-T1 PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2305.9. ~~A~~ The 1000BASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.130.7 ~~1000BASE-T1~~ Receive link status (1.2305.0)

When read as a one, bit 1.2305.0 indicates that the 1000BASE-T1 PMA/PMD receive link is up. When read as a zero, bit 1.2305.0 indicates that the 1000BASE-T1 PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior.

45.2.1.130c 1000BASE-T1 ~~Training Register~~ training register (Register 1.2306)

The assignment of bits in the 1000BASE-T1 training register is shown in Table 45–98c.

Table 45–98c—1000BASE-T1 ~~Training Register~~training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2306.15:11	Reserved	~~Set to 0s~~Value always 0	~~R/W~~RO
1.2306.10:4	User ~~Field~~field	7 bit user defined field to send to the link partner	R/W
1.2306.1	OAM ~~Advertisement~~advertisement	1 = OAM ability advertised to link partner 0 = OAM ability not advertised to link partner	R/W
1.2306.0	EEE ~~Advertisement~~advertisement	1 = EEE ability advertised to link partner 0 = EEE Ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.130c.1 ~~1000BASE-T1~~ User ~~Field~~ field (1.2306.10:4)

This register is a user defined 7 bit field that is transmitted to the link partner during training.

45.2.1.130c.2 ~~1000BASE-T1~~ OAM ~~Advertisement~~ advertisement (1.2306.1)

When set as a one, this bit indicates to the link partner that the 1000BASE-T1 PHY is advertising OAM capability.When set as a zero, this bit indicates to the link partner that the 1000BASE-T1 PHY is not advertising OAM capability. This bit shall be set to 0 if the 1000BASE-T1 PHY does not support OAM.

45.2.1.130c.3 ~~1000BASE-T1~~ EEE ~~Advertisement~~ advertisement (1.2306.0)

When set as a one, this bit indicates to the link partner that the 1000BASE-T1 PHY is advertising EEE capability. When set as a zero, this bit indicates to the link partner that the 1000BASE-T1 PHY is not advertising EEE capability. This bit shall be set to 0 if the 1000BASE-T1 PHY does not support EEE.

45.2.1.130d 1000BASE-T1 ~~Link Partner Training Register~~ link partner training register (Register 1.2307)

The assignment of bits in the 1000BASE-T1 link partner training register is shown in Table 45–98d. The values in this register are not valid until link is up.

45.2.1.130d.1 ~~1000BASE-T1~~ Link ~~Partner User Field Register~~ partner user field (1.2307.10:4)

This register is a user defined 7 bit field that is received from the link partner during training.

Table 45–98d—1000BASE-T1 ~~Link Partner Training Register~~link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2307.15:11	Reserved	~~Ignore when read~~Value always 0	RO
1.2307.10:4	Link ~~Partner User Field~~partner user field	7 bit user defined field received from the link partner	RO
1.2307.3:2	Reserved	~~Ignore when read~~Value always 0	RO
1.2307.1	Link ~~Partner~~ partner OAM ~~Advertisement~~advertisement	1 = Link partner has OAM ability 0 = Link partner does not have OAM ability	RO
1.2307.0	Link ~~Partner~~ partner EEE ~~Advertisement~~advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.130d.2 ~~1000BASE-T1~~ Link ~~Partner~~ partner OAM ~~Advertisement Register~~ advertisement (1.2307.1)

When read as a one, this bit indicates the link partner is advertising OAM capability. When read as a zero, this bit indicates the link partner is not advertising OAM capability. OAM capability shall be enabled only when both the 1000BASE-T1 PHY and link partner are advertising OAM capability.

45.2.1.130d.3 ~~1000BASE-T1~~ Link ~~Partner~~ partner EEE ~~Advertisement Register~~ advertisement (1.2307.0)

When read as a one, this bit indicates the link partner is advertising EEE capability. When read as a zero, this bit indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the 1000BASE-T1 PHY and link partner are advertising EEE capability.

45.2.1.130e 1000BASE-T1 ~~Test Mode Control~~ test mode control register (Register 1.2308)

The assignment of bits in the 1000BASE-T1 ~~Test~~ test mode control register is shown in Table 45–98e. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–98e—1000BASE-T1 ~~Link Mode Control~~test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2308.15:13	~~Reserved~~ Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	RO
1.2308.12:0	Reserved	~~Set to 0s~~Value always 0	RO

[a]RO = Read only

45.2.1.130e.1 ~~1000BASE-T1~~ Test mode control (1.2308.15:13)

Transmitter test mode operations defined by bits 1.2307.15:13, are described in 97.5.2 and Table 97–10. The default value for bits 1.2308.15:13 is zero.

45.2.3 PCS Registers

~~Modify~~ Change reserved register space (3.1809 through 3.32767) in Table 45-119 as shown below

Table 45–119—PCS registers

Register address	Register name	Subclause
3.1809 through 3.~~32767~~2303	Reserved	
3.2304	BASE-T1 PCS ~~Control Register~~control	45.2.3.50a
3.2305	BASE-T1 PCS ~~Status 1 Register~~ status 1	45.2.3.50b
3.2306	BASE-T1 PCS ~~Status 2 Register~~ status 2	45.2.3.50c
3.2307	Reserved	
3.3208	OAM ~~Transmit Register~~transmit	45.2.3.50d
3.2309 through 3.3212	OAM ~~Message Registers~~message	45.2.3.50e
3.2313	OAM ~~Receive Register~~receive	45.2.3.50f
3.2314 through 3.3217	Link ~~Partner~~ partner OAM ~~Message Registers~~message	45.2.3.50g
3.2318 through 3.32767	Reserved	

45.2.3.50a BASE-T1 PCS ~~Control Register~~ control register (Register 3.2304)

The assignment of bits in the BASE-T1 PCS control register is shown in Table 45–163a. The default value for each bit of the BASE-T1 PCS control ~~1~~ register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45–163a—BASE-T1 ~~Control Register~~PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2304.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
3.2304.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2304.13:0	Reserved	~~Set to 0s~~Value always 0	~~R/W~~RO

[a]RO = Read only, R/W = Read/Write, SC = Self Clearing

45.2.3.50a.1 ~~BASE-T1~~ Reset (3.2304.15)

Resetting ~~a~~ the BASE-T1 PCS is accomplished by setting bit 1.2304.15 to a one. This action shall set all BASE-T1 PCS registers to their default states. As a consequence, this action may change the internal state of the BASE-T1 PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and ~~a~~ the BASE-T1 PCS shall return a value of one in bit 1.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. ~~A~~ The

BASE-T1 PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2304.15. During a reset, ~~a~~ the BASE-T1 PCS shall respond to reads from register bits 3.2304.15 and 3.8.15:14. All other register bits should be ignored.

NOTE—This operation may interrupt data communication.

45.2.3.50a.2 ~~BASE-T1 Low power~~ Loopback (3.2304.14)

The BASE-T1 PCS shall be placed in a loopback mode of operation when bit 3.2304.14 is set to a one. When bit 3. 2304.14 is set to a one, the BASE-T1 PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2304.14 is zero.

45.2.3.50b BASE-T1 PCS ~~Status~~ status 1 ~~Register~~ register (Register 3.2305)

The assignment of bits in the BASE-T1 ~~Status~~ PCS status 1 register is shown in Table 45–163b. All the bits in the BASE-T1 PCS status 1 register are read only; a write to the BASE-T1 PCS status 1 register shall have no effect.

Table 45–163b—BASE-T1 ~~Status~~ status 1 ~~Register~~register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2305.15:12	Reserved	~~Ignore when read~~Value always 0	RO
3.2305.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.10	Rx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2305.6:3	Reserved	~~Ignore when read~~Value always 0	RO
3.2305.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2305.1:0	Reserved	~~Ignore when read~~Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.50b.1 ~~BASE-T1 Transmit~~ Tx LPI received (3.2305.11)

When read as a one, bit 3.2305.11 indicates that the transmit BASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.11 indicates that the BASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.50b.2 ~~BASE-T1 Receive~~ Rx LPI received (3.2305.10)

When read as a one, bit 3.2305.10 indicates that the receive BASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.10 indicates that the BASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.50b.3 ~~BASE-T1 Transmit~~ Tx LPI indication (3.2305.9)

When read as a one, bit 3.2305.9 indicates that the transmit BASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.9 indicates that the BASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.50b.4 ~~BASE-T1 Receive~~ Rx LPI indication (3.2305.8)

When read as a one, bit 3.2305.8 indicates that the receive BASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.8 indicates that the BASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.50b.5 ~~BASE-T1~~ Fault (3.2305.7)

When read as a one, bit 3.1.7 indicates that the BASE-T1 PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.1.7 indicates that the BASE-T1 PCS has not detected a fault condition.

45.2.3.50b.6 ~~BASE-T1~~ PCS receive link status (3.2305.2)

When read as a one, bit 3.2305.2 indicates that the BASE-T1 PCS receive link is up. When read as a zero, bit 3.2305.2 indicates that the BASE-T1 PCS receive link is down. This bit is a latching low version of bit 3.2306.10. The receive link status bit shall be implemented with latching low behavior.

45.2.3.50c BASE-T1 PCS ~~Status~~ status 2 ~~Register~~ register (Register 3.2306)

The assignment of bits in the BASE-T1 ~~Status~~ PCS status 2 register is shown in Table 45–163c. All the bits in the BASE-T1 PCS status 2 register are read only; a write to the BASE-T1 PCS status 2 register shall have no effect.

Table 45–163c—BASE-T1 ~~Status~~ PCS status 2 ~~Register~~register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2306.15:11	Reserved	~~Ignore when read~~Value always 0	RO
3.2306.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2306.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2306.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2306.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LL
3.2306.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2305.5:0	~~BER~~BER count	BER counter	RO/NR

[a]RO = Read only, LL = Latching Low, NR = Non Roll-over

45.2.3.50c.1 ~~BASE-T1~~ Receive link status (3.2306.10)

When read as a one, bit 3.2306.10 indicates that the BASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2306.10 indicates that the BASE-T1 PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 97.3.7.1

45.2.3.50c.2 ~~BASE-T1~~ PCS high BER (3.2306.9)

When read as a one, bit 3.2306.9 indicates that the BASE-T1 PCS receiver is detecting a BER of > 4 ~~x~~ × 10^{-4}. When read as a zero, bit 3.~~32~~2306.~~1~~9 indicates that the BASE-T1 PCS receiver is detecting a BER of > 4 ~~x~~ × 10^{-4}. This bit is a direct reflection of the state of the hi_rfer variable defined in 97.3.7.1.

45.2.3.50c.3 ~~BASE-T1~~ PCS block lock (3.2306.8)

When read as a one, bit 3.2306.8 indicates that the BASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2306.8 indicates that the BASE-T1 PCS receiver has not achieved block lock. This bit is a direct reflection of the state of the block_lock variable defined in 97.3.7.1.

45.2.3.50c.4 ~~BASE-T1~~ Latched high BER (3.2306.7)

When read as a one, bit 3.2306.7 indicates that the BASE-T1 PCS has detected a high BER. When read as a zero, bit 3.2306.7 indicates that the BASE-T1 PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. This bit is a latching high version of the BASE-T1 PCS high BER status bit (3.2306.9).

45.2.3.50c.5 ~~BASE-T1~~ Latched block lock (3.2306.6)

When read as a one, bit 3.2306.6 indicates that the BASE-T1 PCS has achieved block lock. When read as a zero, bit 3.2306.6 indicates that the BASE-T1 PCS has lost block lock. The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the BASE-T1 PCS block lock status bit (3.2306.8).

45.2.3.50c.6 ~~BASE-T1~~ BER count (3.2306.5:0)

The BER counter is a six bit count as defined by RFER_count in 97.3.7.2. These bits shall be reset to all zeros when the BASE-T1 PCS status 2 register is read by the management function or upon execution of the BASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.50d OAM ~~Transmit Register~~ transmit register (Register 3.2308)

The assignment of bits in the OAM transmit register is shown in Table 45–163d.

45.2.3.50d.1 OAM ~~Message Valid~~ message valid (3.2308.15)

This bit shall be set to 1 when the OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2308.11:8 are properly configured to be transmitted. This register shall be cleared by the state machine to indicate whether the next OAM message can be written into the registers.

Table 45–163d—OAM Transmit Register

Bit(s)	Name	Description	R/W
3.2308.15	OAM Message Valid	Used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be atomically loaded. This bit shall self clear when registers are atomically loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2308.14	Toggle Value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2308.13	OAM Message Received	This bit shall self clear on read. 1 = OAM message received by link partner 0 = OAM message not received by link partner	RO, LH
3.2308.12	Received Message Toggle Value	Toggle value of message that was received by link partner as indicated in 3.2308.13.	RO
3.2308.11:8	Message Number	user-defined message number to send	R/W
3.2308.7:4	Reserved	Set to 0s	R/W
3.2308.3	Ping Received	Received PingTx value from latest good OAM frame received	RO
3.2308.2	Ping Transmit	Ping value to send to link partner	R/W
3.2308.1:0	Local SNR	00 = PHY link is dying and will drop link and re-link within 2 to 4 ms after the end of the current OAM frame. 01 = LPI refresh insufficient for maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

45.2.3.50d.2 Toggle ~~Value~~ value (3.2308.14)

The state machine shall assign a value alternating between 0 and 1 to associate with the 8 octet OAM message transmit by the 1000BASE-T1 PHY. This bit should be read and recorded prior to setting 3.2308.15 to 1. The recorded value can be correlated with 3.2308.12 as a confirmation that the OAM message is received by the link partner.

45.2.3.50d.3 OAM ~~Message Received~~ message received (3.2308.13)

This bit shall indicate whether the most recently transmitted OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner. This variable shall clear on read.

45.2.3.50d.4 Received ~~Message Toggle Value~~ message toggle value (3.2308.12)

This bit indicates the toggle bit value of the OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if 3.2308.13 is 1.

45.2.3.50d.5 Message ~~Number~~ number (3.2308.11:8)

The OAM message number to be transmitted. This field is user defined but is recommended that it be used to indicate the meaning of the 8 octet OAM message. If used this way, up to 16 different 8 octet messages

Table 45–163d—OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2308.15	OAM message valid	Used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be atomically loaded. This bit shall self clear when registers are atomically loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2308.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2308.13	OAM message received	This bit shall self clear on read. 1 = OAM message received by link partner 0 = OAM message not received by link partner	RO, LH
3.2308.12	Received message toggle value	Toggle value of message that was received by link partner as indicated in 3.2308.13.	RO
3.2308.11:8	Message number	user-defined message number to send	R/W
3.2308.7:4	Reserved	Value always 0	RO
3.2308.3	Ping received	Received PingTx value from latest good OAM frame received	RO
3.2308.2	Ping transmit	Ping value to send to link partner	R/W
3.2308.1:0	Local SNR	00 = PHY link is dying and will drop link and re-link within 2 to 4 ms after the end of the current OAM frame. 01 = LPI refresh insufficient for maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

can be exchanged. The message number is user defined and its definition is outside the scope of this standard.

45.2.3.50d.6 Ping ~~Received~~ received (3.2308.3)

This bit is a delayed version of the value in 3.2308.2 that is loopback by the link partner.

45.2.3.50d.7 Ping ~~Transmit~~ transmit (3.2308.2)

This bit is set by the 1000BASE-T1 PHY to for the link partner to loopback. The loopback value should be received after a small delay in 3.2308.3.

45.2.3.50d.8 Local SNR (3.2308.1:0)

These bits are set by the 1000BASE-T1 PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.50e OAM ~~Message Registers~~ message register (Registers 3.2309 to 3.2312)

The 8 octet OAM message data to be transmitted. The 8 octet message data is user defined and its definition is outside the scope of this standard.

Table 45–163e—~~OAM Message Register~~
Table 45–163e—OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2309.15:8	OAM ~~Message~~ message 1	Message octet 1. LSB transmitted first.	R/W
3.2309.7:0	OAM ~~Message~~ message 0	Message octet 0. LSB transmitted first.	R/W
3.2310.15:8	OAM ~~Message~~ message 3	Message octet 3. LSB transmitted first.	R/W
3.2310.7:0	OAM ~~Message~~ message 2	Message octet 2. LSB transmitted first.	R/W
3.2311.15:8	OAM ~~Message~~ message 5	Message octet 5. LSB transmitted first.	R/W
3.2311.7:0	OAM ~~Message~~ message 4	Message octet 4. LSB transmitted first.	R/W
3.2312.15:8	OAM ~~Message~~ message 7	Message octet 7. LSB transmitted first.	R/W
3.2312.7:0	OAM ~~Message~~ message 6	Message octet 6. LSB transmitted first.	R/W

[a]R/W = Read/Write

45.2.3.50f OAM ~~Receive Register~~ receive register (Register 3.2313)

Table 45–163f—OAM Receive Register

Bit(s)	Name	Description	R/W
3.2313.15	Link Partner OAM Message Valid	Used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are valid and ready to be atomically loaded. This bit shall self clear when registers 3.2317 is read. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2313.14	Link Partner Toggle Value	Toggle value received with message.	RO
3.2313.13:12	Reserved	Reserved - 0s	RO
3.2313.11:8	Link Partner Message Number	Message number from link partner	RO
3.2313.7:2	Reserved	Reserved - 0s	RO
3.2313.1:0	Link Partner SNR	00 = PHY link is dying and will drop link and re-link within 2 to 4 ms after the end of the current OAM frame. 01 = LPI refresh insufficient for maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

The assignment of bits in the OAM receive register is shown in Table 45–163f

Table 45–163f—OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2313.15	Link partner OAM message valid	Used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are valid and ready to be atomically loaded. This bit shall self clear when registers 3.2317 is read. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2313.14	Link partner toggle value	Toggle value received with message.	RO
3.2313.13:12	Reserved	Value always 0	RO
3.2313.11:8	Link partner message number	Message number from link partner	RO
3.2313.7:2	Reserved	Value always 0	RO
3.2313.1:0	Link partner SNR	00 = PHY link is dying and will drop link and re-link within 2 to 4 ms after the end of the current OAM frame. 01 = LPI refresh insufficient for maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, SC = Self-clearing

45.2.3.50f.1 Link ~~Partner~~ partner OAM ~~Message Valid~~ message valid (3.2313.15)

This bit shall be set to 1 when the OAM message from the link partner is stored into registers 3.2314, 3.2315, 3.2316, and 3.2317 and the message number in 3.2313.11:8. This register shall be cleared when register 3.2317 is read.

45.2.3.50f.2 Link ~~Partner Toggle Value~~ partner toggle value (3.2313.14)

The bit indicates the toggle value associate with the 8 octet OAM message from the link partner.

45.2.3.50f.3 Link ~~Partner Message Number~~ partner message number (3.2313.11:8)

The OAM message number from the link partner.

45.2.3.50f.4 Link ~~Partner~~ partner SNR (3.2313.1:0)

These bits indicate the status of the link partner receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.50g Link ~~Partner~~ partner OAM ~~Message Registers~~ message register (Registers 3.2314 to 3.2317)

The 8 octet OAM message data from the link partner. Register 3.2313.15 shall be cleared when register 3.2317 is read.

45.2.7 Auto-Negotiation registers

~~*Modify*~~ *Change reserved register space (7.62 through 7.32767) in Table 45-200 as shown below*

Table 45–163g—Link ~~Partner~~ partner OAM ~~Message Register~~message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2314.15:8	Link ~~Partner~~ partner OAM ~~Message~~ message 1	Message octet 1. LSB transmitted first.	RO
3.2314.7:0	Link ~~Partner~~ partner OAM ~~Message~~ message 0	Message octet 0. LSB transmitted first.	RO
3.2315.15:8	Link ~~Partner~~ partner OAM ~~Message~~ message 3	Message octet 3. LSB transmitted first.	RO
3.2315.7:0	Link ~~Partner~~ partner OAM ~~Message~~ message 2	Message octet 2. LSB transmitted first.	RO
3.2316.15:8	Link ~~Partner~~ partner OAM ~~Message~~ message 5	Message octet 5. LSB transmitted first.	RO
3.2316.7:0	Link ~~Partner~~ partner OAM ~~Message~~ message 4	Message octet 4. LSB transmitted first.	RO
3.2317.15:8	Link ~~Partner~~ partner OAM ~~Message~~ message 7	Message octet 7. LSB transmitted first.	RO
3.2317.7:0	Link ~~Partner~~ partner OAM ~~Message~~ message 6	Message octet 6. LSB transmitted first.	RO

[a]RO = Read only

Table 45–200—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.62 through 7.~~32 767~~511	Reserved	
7.512	BASE-T1 AN ~~control register~~control	45.2.7.14a
7.513	BASE-T1 AN status	45.2.7.14b
7.514 through 7.516	BASE-T1 AN ~~advertisement register~~advertisement	45.2.7.14c
7.517 through 7.519	BASE-T1 AN LP Base Page ~~ability register~~ability	45.2.7.14d
7.520 through 7.522	BASE-T1 AN ~~NEXT PAGE transmit register~~Next Page transmit	45.2.7.14e
7.523 through 7.525	BASE-T1 AN LP ~~NEXT PAGE ability register~~Next Page ability	45.2.7.14f
7.526 through 7.32767	Reserved	

45.2.7.14a BASE-T1 AN control register (Register 7.512)

The assignment of bits in the BASE-T1 AN control register is shown in Table 45–211a. The default value for each bit of the BASE-T1 AN control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

45.2.7.14a.1 AN reset (7.512.15)

Resetting AN is accomplished by setting bit 7.512.15 to a one. This action shall set all BASE-T1 AN registers to their default states. As a consequence, this action may change the internal state of AN and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same

Table 45–211a—~~Link Partner OAM Message Register~~
Table 45–211a—BASE-T1 AN control register bit definitions

Bit(s)	Name	Description	R/W[a]
7.512.15	AN reset	1 = AN reset 0 = AN normal operation	R/W, SC
7.512.14:13	Reserved	Value always 0	RO
7.512.12	Auto-Negotiation enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W, SC
7.512.11:10	Reserved	Value always 0	RO
7.512.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process 0 = Auto-Negotiation in process, disabled, or not supported	R/W, SC
7.512.8:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

package. This bit is self-clearing, and AN shall return a value of one in bit 7.512.15 when a reset is in progress and a value of zero otherwise. AN is not required to accept a write transaction to any of its registers until the reset process is complete. The reset process shall be completed within 0.5 s from the setting of bit 7.512.15. During an AN reset, AN shall respond to reads from register bit 7.512.15. All other register bits should be ignored.

The default value for bit 7.512.15 is zero.

NOTE—This operation may interrupt data communication.

45.2.7.14a.2 Auto-Negotiation enable (7.512.12)

The Auto-Negotiation function shall be enabled by setting bit 7.512.12 to a one. If bit 7.512.12 is set to one, then PHY type bits 1.2304.3:0 Master/Slave bits 1.2304.4 shall have no effect on the link configuration, and the Auto-Negotiation process determines the link configuration. If bit 7.512.12 is cleared to zero, then bits 1.2304.3:0 and 1.2304.4 determines the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

The default value of bit 7.512.12 is one, unless the BASE-T1 PHY reports via bit 7.513.3 that it lacks the ability to perform Auto-Negotiation, in which case the default value of bit 7.512.12 is zero.

45.2.7.14a.3 Restart Auto-Negotiation (7.512.9)

If the BASE-T1 PMA/PMD reports (via bit 7.513.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the BASE-T1 PMA/PMD shall return a value of zero in bit 7.512.9 and any attempt to write a one to bit 7.512.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 7.512.9 to one. This bit is self-clearing, and ~~a~~ the BASE-T1 PMA/PMD shall return a value of one in bit 7.512.9 until the Auto-Negotiation process has been initiated. If Auto-Negotiation was completed prior to this bit being set, the process shall be ~~reinitiated~~reinitialized. The Auto-Negotiation process shall not be affected by clearing this bit to zero.

The default value for 7.512.9 is zero.

45.2.7.14b BASE-T1 AN status (Register 7.513)

The assignment of bits in the BASE-T1 AN status register is shown in Table 45–211b. All the bits in the BASE-T1 AN status register are read only; therefore, a write to the BASE-T1 AN status register shall have no effect.

Table 45–211b—BASE-T1 AN status ~~register~~register bit definitions

Bit(s)	Name	Description	R/W[a]
7.513.15:7	Reserved	Value always 0	RO
7.513.6	Page received	1 = A page has been received 0 = A page has not been received	RO, LH
7.513.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.513.4	Remote fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO, LH
7.513.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.513.2	Link status	1 = Link is up 0 = Link is down	RO, LH
7.513.1	Reserved	Value always 0	RO
7.513.0	Link partner Auto-Negotiation ability	1 = LP is able to perform Auto-Negotiation 0 = LP is not able to perform Auto-Negotiation	RO

[a]RO = Read only, LH = Latching High

45.2.7.14b.1 Page received (7.513.6)

The Page received bit (7.513.6) shall be set to one to indicate that a new link codeword has been received and stored in the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 or the BASE-T1 AN LP ~~NEXT PAGE~~ Next Page ability registers 7.523 to 7.525. The contents of the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 are valid when bit 7.513.6 is set the first time during the Auto-Negotiation. The Page received bit shall be reset to zero on a read of the BASE-T1 AN status register (Register 7.513).

45.2.7.14b.2 Auto-Negotiation complete (7.513.5)

When read as a one, bit 7.513.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the Auto-Negotiation register 7.514 to 7.516 and 7.517 to 7.519 are valid. When read as a zero, bit 7.513.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of 7.517 through 7.525 registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. ~~A~~ The BASE-T1 PMA/PMD shall return a value of zero in bit 7.513.5 if Auto-Negotiation is disabled by clearing bit 7.512.12. ~~A~~ The BASE-T1 PMA/PMD shall also return a value of zero in bit 7.513.5 if it lacks the ability to perform Auto-Negotiation.

45.2.7.14b.3 Remote fault (7.513.4)

When read as one, bit 7.513.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is AN specific. The remote fault bit shall be implemented with a latching function, such that the occurrence of a remote fault causes the bit 7.513.4 to become set and

remain set until it is cleared. Bit 7.513.4 shall be cleared each time register 7.513 is read via the management interface, and shall also be cleared by a AN reset.

45.2.7.14b.4 Auto-Negotiation ability (7.513.3)

When read as a one, bit 7.513.3 indicates that the BASE-T1 PMA/PMD has the ability to perform BASE-T1 Auto-Negotiation. When read as a zero, bit 7.513.3 indicates that the BASE-T1 PMA/PMD lacks the ability to perform BASE-T1 Auto-Negotiation.

45.2.7.14b.5 Link status (7.513.2)

When read as a one, bit 7.513.2 indicates that the BASE-T1 PMA/PMD has determined that a valid link has been established. When read as a zero, bit 7.513.2 indicates that the link has been invalid after this bit was last read. Bit 7.513.2 is set to one when the variable link_status equals OK and is cleared to zero when the variable link_status equals FAIL. The link status bit shall be implemented with a latching function, such that the occurrence of a link_status equals FAIL condition causes the link status bit to become cleared and remain cleared until it is read via the management interface. Bit 7.513.2 shall be cleared upon AN reset. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

45.2.7.14b.6 Link partner Auto-Negotiation ability (7.513.0)

The link partner Auto-Negotiation ability bit shall be set to one to indicate that the link partner is able to participate in the Auto-Negotiation function. This bit shall be reset to zero if the link partner is not Auto-Negotiation able.

45.2.7.14c BASE-T1 AN advertisement register (Registers 7.514, 7.515, and 7.516)

The assignment of bits in the BASE-T1 AN advertisement register is shown in Table 45–211c.

The Selector field (7.514.4:0) is set to the IEEE 802.3 code as specified in Annex 98A. The Acknowledge bit (7.514.14) is set to zero.

The technology ability field, as defined in 98.2.1.2, represents the technologies supported by the local device. Only bits representing supported technologies may be set. Management may clear bits in the technology ability field and restart Auto-Negotiation to negotiate an alternate common mode.

The management entity initiates renegotiation with the link partner using alternate abilities by setting the Restart Auto-Negotiation bit (7.512.9) in the AN control register to one.

Any writes to this register prior to completion of Auto-Negotiation, as indicated by bit 7.513.5, should be followed by a renegotiation for the new values to take effect. Once Auto-Negotiation has completed, software may examine this register along with the LP Base Page ability register to determine the highest common denominator technology.

The Base Page value is transferred to mr_adv_ability when register 7.514 is written. Therefore, if used, registers 7.515 and 7.516 should be written before 7.514.

45.2.7.14d BASE-T1 AN LP Base Page ability register (Registers 7.517, 7.518, and 7.519)

~~All~~ The assignment of ~~the~~ bits in the BASE-T1 AN LP Base Page ability register ~~are read only. A write to the BASE-T1 AN LP Base Page ability register shall have no effect~~is shown in Table 45–211d.

All of the bits in the BASE-T1 AN LP Base Page ability register are read only. A write to the BASE-T1 AN LP Base Page ability register shall have no effect.

Table 45–211c—BASE-T1 AN advertisement register bit definitions

Bit(s)	Name	Description	R/W[a]
7.514.15	Next Page	See 98.2.1.2.9	R/W
7.514.14	Acknowledge	Value always 0~~, writes ignored~~	RO
7.514.13	Remote fault	See 98.2.1.2.7	R/W
7.514.12:5	D12:D5	See 98.2.1.2	R/W
7.514.4:0	Selector field	See Annex 98A	R/W
7.515.15:0	D31:D16	See 98.2.1.2	R/W
7.516.15:0	D47:D32	See 98.2.1.2	R/W

[a]RO = Read only, R/W = Read/Write

The value of the registers 7.518 and 7.519 is latched when register 7.517 is read and reads of registers 7.518 and 7.519 return the latched value rather than the current value.

Table 45–211d—AN LP Base Page ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.517.15:0	D15:D0	See 98.2.1.2	RO
7.518.15:0	D31:D16	See 98.2.1.2	RO
7.519.15:0	D47:D32	See 98.2.1.2	RO

[a]RO = Read only

45.2.7.14e BASE-T1 AN ~~NEXT PAGE~~ Next Page transmit register (Registers 7.520, 7.521, and 7.522)

The assignment of bits in the BASE-T1 AN Next Page transmit register is shown in Table 45–211e.

The register contains the BASE-T1 AN LD Next Page link codeword as defined in 98.2.4.3.

On power-up or AN reset, this register shall contain the default value, which represents a Message Page with the message code set to Null Message. This value may be replaced by any valid Extended Next Page message code that the device intends to transmit.

A write to register 7.521 or 7.522 does not set mr_next_page_loaded. Only a write to register 7.520 sets mr_next_page_loaded true as described in 98.5.1. Therefore registers 7.521 and 7.522 register should be written before register 7.520.

45.2.7.14f BASE-T1 AN LP ~~NEXT PAGE~~ Next Page ability register (Registers 7.523, 7.524, and 7.525)

BASE-T1 AN LP ~~NEXT PAGE~~ Next Page ability register (registers 7.523, 7.524, and 7.525) store BASE-T1 link partner Extended Next Pages as shown in Table 45–211f. All of the bits in the BASE-T1 AN LP ~~NEXT PAGE~~ Next Page ability register are read only. A write to the BASE-T1 AN LP ~~NEXT PAGE~~ Next Page ability register shall have no effect.

Table 45–211e—BASE-T1 AN ~~NEXT PAGE~~ Next Page transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
7.520.15	Next ~~Page~~page	See 98.2.4.3	R/W
7.520.14	Reserved	Value always 0	RO
7.520.13	Message ~~Page~~page	See 98.2.4.3	R/W
7.520.12	Acknowledge 2	See 98.2.4.3	R/W
7.520.11	Toggle	See 98.2.4.3	RO
7.520.10:0	Message/Unformatted ~~Code Field~~code field	See 98.2.4.3	R/W
7.521.15:0	Unformatted ~~Code Field~~ code field 1	See 98.2.4.3	R/W
7.522.15:0	Unformatted ~~Code Field~~ code field 2	See 98.2.4.3	R/W

[a]RO = Read only, R/W = Read/Write

Table 45–211f—AN LP ~~NEXT PAGE~~ Next Page ability register bit definitions

Bit(s)	Name	Description	R/W[a]
7.523.15	Next ~~Page~~age	See 98.2.4.3	RO
7.523.14	Acknowledge	See 98.2.4.3	RO
7.523.13	Message ~~Page~~page	See 98.2.4.3	RO
7.523.12	Acknowledge 2	See 98.2.4.3	RO
7.523.11	Toggle	See 98.2.4.3	RO
7.523.10:0	Message/Unformatted ~~Code Field~~code field	See 98.2.4.3	RO
7.524.15:0	Unformatted ~~Code Field~~ code field 1	See 98.2.4.3	RO
7.525.15:0	Unformatted ~~Code Field~~ code field 2	See 98.2.4.3	RO

[a]RO = Read only

The value of registers 7.524 and 7.525 is latched when register 7.523 is read and reads of registers 7.524 and 7.525 return the latched value rather than the current value.

NOTE—If this register is used to store multiple link partner Extended Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent link partner Extended Next Pages.