1000Base-T Auto Negotiation

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LEVEL ONE

Overview

- Brief Auto Negotiation Overview
- General Next Page Exchange
- 1000BASE-T Next Page Exchange
- Priority Table
- Registers
- GMII Pin Order

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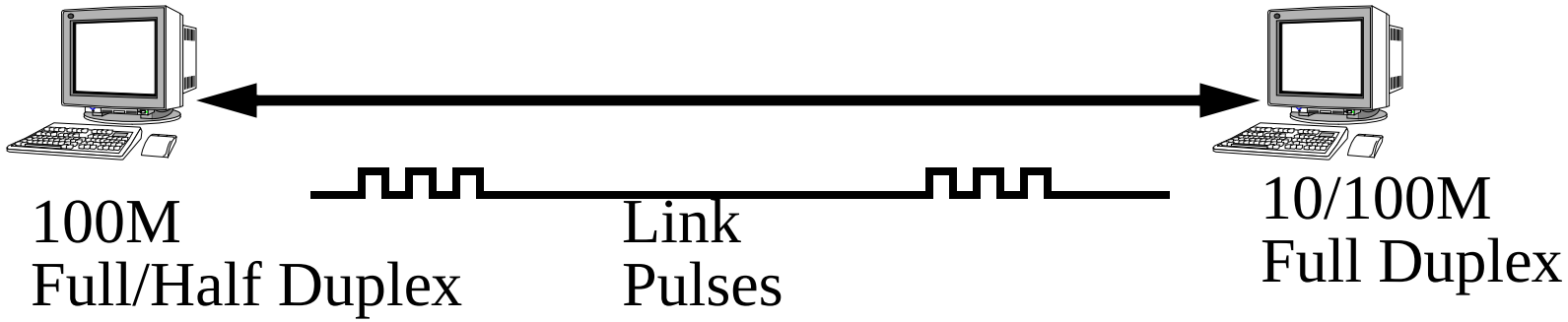
What is Auto Negotiation?

- Method used to exchange information between 2 stations
- Used to Configure operating parameters such as speed and duplex
- Uses 10Base-T Link Pulses for backwards compatibility
- Allows for automatic link establishment without user intervention



Requirements

- Requires the ability to Receive and Transmit 10Base-T Link Pulses
- 10Base-T and 100Base-T support parallel detection, hence Auto Negotiation was optional
- 1000Base-T Requires the use of Auto Negotiation, No Parallel Detection only scheme can be supported.
- Next Page exchanges must be used to convey 1000Base-T information
- Utilizes existing clause 28 scheme
  - Little/No modification required
  - Minimize/do not use new registers

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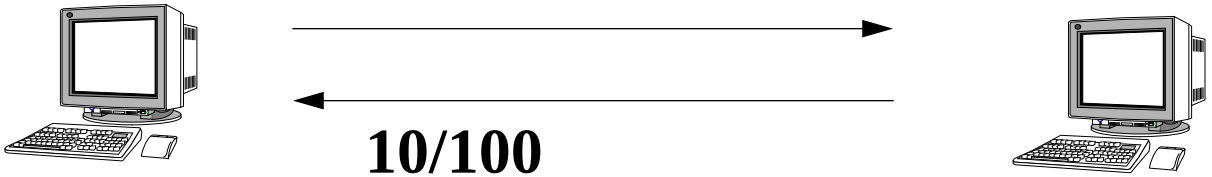
Base Page Exchange



10/100
TX/T4
FD/HD
PAUSE

This must still be supported, even if the PHY is not capable of 10Mbps or 100Mbps modes
Utilizes Registers 4 and 5.
Does not require Next Pages(optional)

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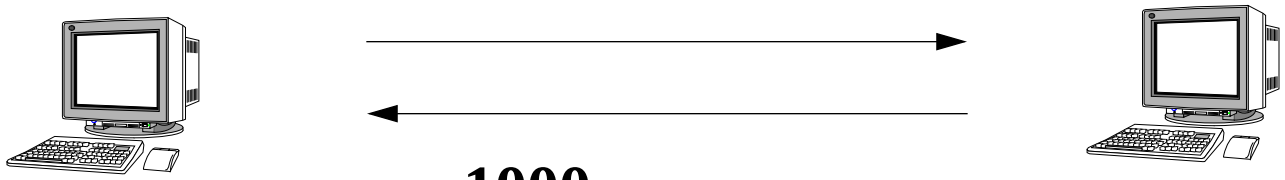
Next Page Exchange



1000
FD/HD
ASYM PAUSE
MASTER/SLAVE

Utilizes Register 7 for Transmitting and Register 8 for Receiving.

One page at a time is exchanged.
Toggle and other bits are used for synchronization.

1000Base-T Next Page Information

- Master/Slave Overide
- Repeater/DTE
- 1000Base-T Full Duplex
- 1000Base-T Half Duplex
- Asymetric Pause
- TX Coding Type
- Master/Slave Random Seed

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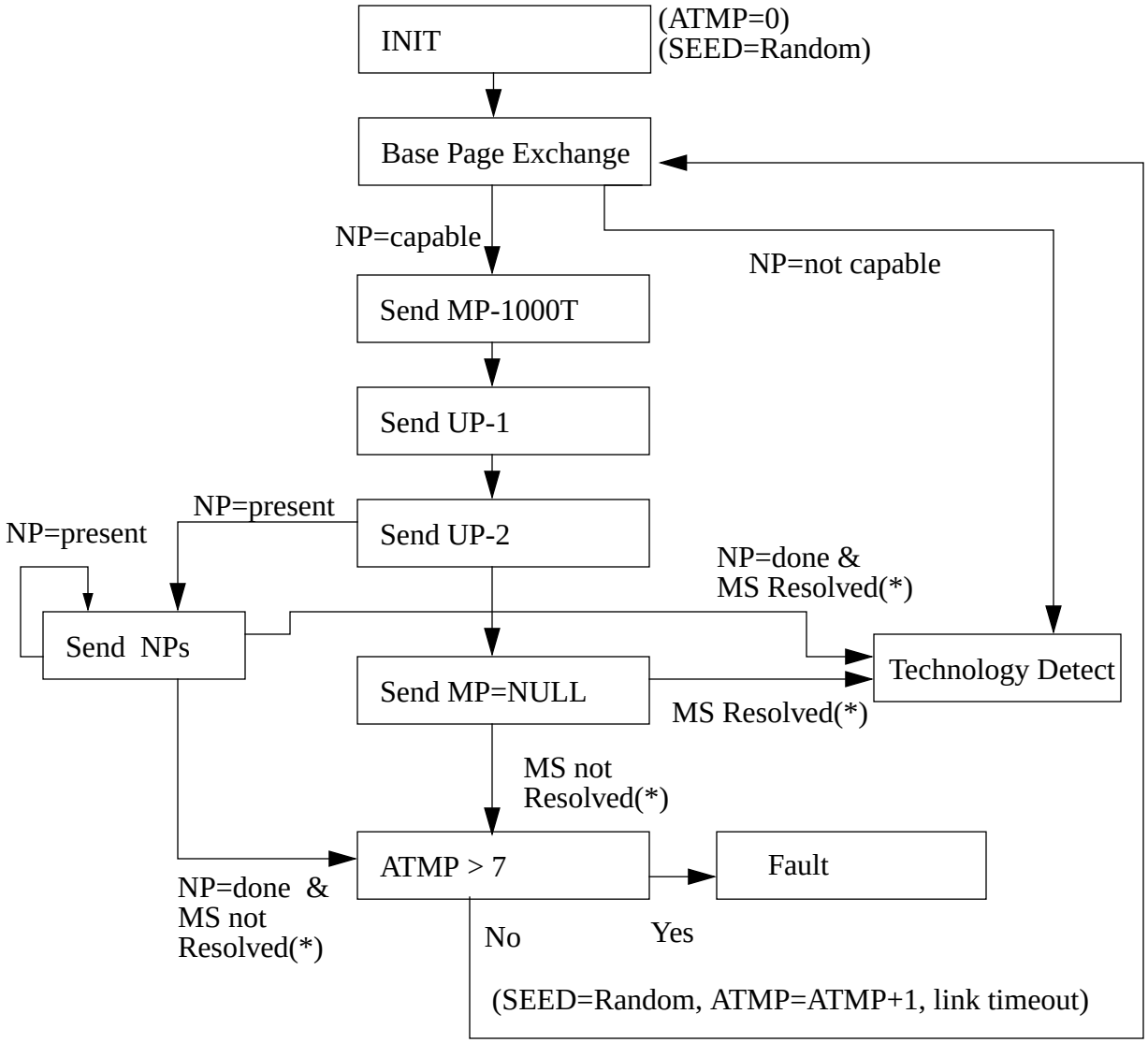
1000Base-T Use of Next Pages

- Uses the Clause 28 Next Page exchange mechanism.
- Sends 1 Message Code(9) followed by 2 unformatted pages containing the relevant information.
- Scheme does NOT utilize ACK2 bit!
- PHY device must intercept all 1000T Next pages and store them internally for resolution functions.
- PHY device must also source all 1000T Next pages from internal registers.

1000Base-T Next Page Flow



Note:
for illustration only

*all next pages from link partner have also been received

*MS Resolved only matters if HCD is 1000T, otherwise bit should be set to true.

ATMP = number of MS resolution attempts

SEED = random seed used for MS resolution

MS = Master/Slave

NP = Next Pages

UP = Unformatted Page

MP = Message Page

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1000Base-T Master/Slave Resolution

- If both devices want to be Master or Slave a tie breaker is needed.
- Using a random seed, the device with the higher value becomes master.
- A maximum of 7 attempts are made to resolve the Master/Slave status.
- More information is available via 100Base-T2 spec or clause 40

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1000Base-T Priority Table

Table 1—Update to 28B.3 Priority Resolution

Priority Level	Technology
a ** (highest)	**1000BASE-T Full Duplex**
b**	**1000BASE-T**
c	100BASE-T2 Full Duplex
d	100BASE-T2
e	100BASE-TX Full Duplex
f	100BASE-T4
g	100BASE-TX
h	10BASE-T Full Duplex
i (lowest)	10BASE-T
**** represents changes requested**	

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1000Base-T Next Page Bit Order

Table 2: Next page data ordering

Bit	MP	UP-1	UP-2
15	NP	NP	NP
14	ACK/Rsvd	ACK/Rsvd	ACK/Rsvd
13	MP	MP	MP
12	ACK2	ACK2	ACK2
11	T	T	T
10	0	Rsvd	SB10
9	0	Rsvd	SB9
8	0	Rsvd	SB8
7	0	Rsvd	SB7
6	0	ASM DIR	SB6
5	0	TX CODING	SB5
4	0	1000T HD	SB4
3	1	1000T FD	SB3
2	0	RPTR/DTE	SB2
1	0	M/S MAN CFG	SB1
0	1	M/S CFG ENAB	SB0

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Registers Required(1000Base-T)

All standard 10/100 Registers

+

Next Page Transmit(7)
Next Page Receive(8)
1000Base-T Configuration(9)
1000Base-T Status(10)
Extended Status(15)

Next Page Transmit

Table 3: Auto Negotiation Next Page Transmit Register (Address 7)

Bit	Name	Description	Type [1]
7.15	Next Page (NP)	1 = Additional next pages follow 0 = Last page	R/W
7.14	Reserved	Write as 0, ignore on read	RO
7.13	Message Page (MP)	1 = Message page 0 = Unformatted page	R/W
7.12	Acknowledge 2 (ACK2)	1 = Will comply with message 0 = Can not comply with message	R/W
7.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	R/W
7.10:0	Message/Unformatted Code Field		R/W

1. R/W = Read/Write
   RO = Read Only

Next Page Receive

Table 4: Auto Negotiation Link Partner Next Page Ability Register (Address 8)

Bit	Name	Description	Type [1]
8.15	Next Page (NP)	1 = Link Partner has additional next pages to send 0 = Link Partner has no additional next pages to send	RO
8.14	Acknowledge (ACK)	1 = Link Partner has received Link Code Word from CHEETAH 0 = Link Partner has not received Link Code Word from CHEE-TAH	RO
8.13	Message Page (MP)	1 = Page sent by the Link Partner is a Message Page 0 = Page sent by the Link Partner is an Unformatted Page	RO
8.12	Acknowledge 2 (ACK2)	1 = Link Partner Will comply with the message 0 = Link Partner can not comply with the message	RO
8.11	Toggle (T)	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	RO
8.10:0	Message/Unformatted Code Field		RO

1. R/W = Read/Write
   RO = Read Only

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1000Base-T Configuration

Table 5: 1000BASE-T/100BASE-T2 Control Register (Address 9)

Bit	Name	Description	Type [1]
9.15:14	Transmit Test mode	Default bit values are “00”	R/W
9.13	Receive Test mode	Default bit value is “0”	R/W
9.12	Master/Slave Config Enable	1=Enable MASTER-SLAVE Manual configuration value 0=Disable MASTER-SLAVE Manual configuration value	R/W
9.11	Master/Slave Config Value	1=Configure PHY as MASTER during MASTER-SLAVE negotiation, only when 9.13 is set to logical one. 0=Configure PHY as SLAVE during MASTER-SLAVE negotiation, only when 9.13 is set to logical one.	R/W
9.10	Repeater/DTE	1=Repeater device port 0=DTE device	R/W
9.9	1000T Full Duplex	1=Advertise 1000BASE-T Full Duplex 0=Advertise 1000BASE-T Full Duplex	R/W
9.8	1000T Half Duplex	1=Advertise 1000BASE-T Half Duplex 0=Advertise 1000BASE-T Half Duplex	R/W
9.7	TX Coding	1=Advertise to Link Partner to use 6db transmit coding 0=Advertise to Link Partner to use 3db transmit coding	R/W
9.6	ASM DIR	Advertise Asymetric Pause direction bit. See 37.4 for more details. This bit is used in conunction with PAUSE.	R/W
9.5:0	Reserved	Reserved	R/W

1. R/W = Read/Write
   RO = Read Only

Bits 9.15:9.10 are exactly the same as 100Base-T2

Bits 9.9:9.6 are applicable only to 1000Base-T

Bits 9.9 and 9.8 are a subset of register 15

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1000Base-T Status

Table 6: 1000BASE-T/100BASE-T2 Status Register (Address 10)

Bit	Name	Description	Type [1]
10.15	Master/Slave config fault	1=MASTER-SLAVE manual configuration fault detected 0=No MASTER-SLAVE manual configuration fault detected	RO
10.14	Master/Slave resolution complete	1=MASTER-SLAVE configuration resolution has completed 0=MASTER-SLAVE configuration resolution has not completed	RO
10.13	Local Receiver Status	1=Local Receiver OK 0=Local Receiver not OK	RO
10.12	Remote Receiver Status	1=Remote Receiver OK 0=Remote Receiver not OK	RO
10.11	LP 1000T FD	1=Link Partner is capable of 1000BASE-T Full Duplex 0=Link Partner is not capable of 1000BASE-T Full Duplex	RO
10.10	LP 1000T HD	1=Link Partner is capable of 1000BASE-T Half Duplex 0=Link Partner is not capable of 1000BASE-T Half Duplex	RO
10.9	LP TX CODING	1=Link Partner requests that 6db coding be utilized 0=Link Partner requests that 3db coding be utilized	RO
10.8	LP ASM DIR	Link Partners Asymetric Pause Direction bit. See 37.4 for mappings. This bit is used in conjunction with PAUSE	RO
10.7:0	Idle Error Count	Idle Error Count	RO/SC

1. R/W = Read/Write
   RO = Read Only

Bits 10.15:10.12 are exactly the same as 100Base-T2

Bits 10.11:10.8 are applicable only to 1000Base-T

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Extended Status

Table 7: Extended Status Register (Address 15)

Bit	Name	Description	Type [1]
15.15	1000BASE-X Full Duplex	1 = PHY able to perform full-duplex 1000BASE-X 0 = PHY not able to perform full-duplex 1000BASE-X	RO
15.14	1000BASE-X Half Duplex	1 = PHY able to perform half-duplex 1000BASE-X 0 = PHY able to perform half-duplex 1000BASE-X	RO
15.13	1000BASE-T Full Duplex	1 = PHY able to perform full-duplex 1000BASE-T 0 = PHY not able to perform full-duplex 1000BASE-T	RO
15.12	1000BASE-T Full Duplex	1 = PHY able to perform half-duplex 1000BASE-T 0 = PHY able to perform half-duplex 1000BASE-T	RO
15.11:0	Reserved	ignore when read	RO

1. RO = Read Only

LEVEL ONE

Why Build Mechanism internal to PHY?

- Allows Management-less configuration
- Allows priority resolution to be done internally
- Does not require manual configuration/ intervention
- Minimizes changes to Clause 28
- Utilizes existing NP mechanism

Why not have a register for all LP information?

- Master/Slave information resolution unimportant beyond initial setup
- We have register bits to cover error status
- Would require additional registers
- Repeater/DTE bit is only useful to the link, not the end user

Alternate Solution(not recommended)

- Priority resolution done externally
- Requires manual configuration
- Requires management interaction
- Use Register 0 to set the speed of the device after all NPs have been exchanged
- Then add a bit to register 9 to inform the device to utilize the register 0 configuration values
- Master Slave resolution done externally