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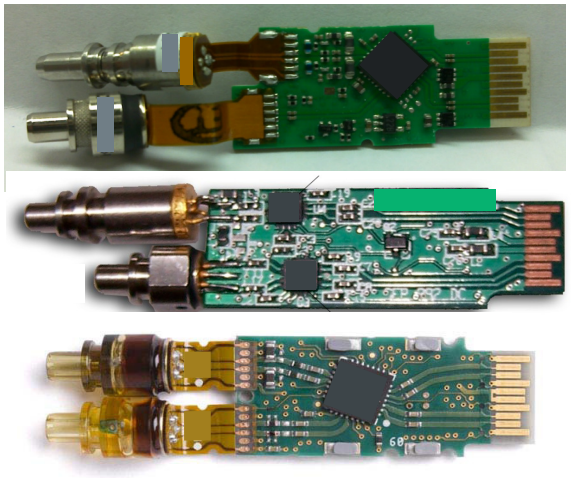
June 29, 2010

Historical perspective

- **What was done for 10-16G modules?**
- **As the rates increases, module retiming becomes omnipresent**
- **Good connector technology is essential but is rarely sufficient**
- **Small form factor has not prevented retimed modules**

10G+ Module Type	Interface
300pin (10G)	Retimed
X2/XENPAK/XPAK (10G)	Retimed
XFP (10G)	Retimed
SFP+ (8G/10G)	Limiting / Linear
Next Gen SFP+ (16G/10G)	Retimed
CFP (40/100G)	Retimed
CFP2 (100G)	Retimed ?



Which one is not retimed?

S parameter comparison at Nyquist

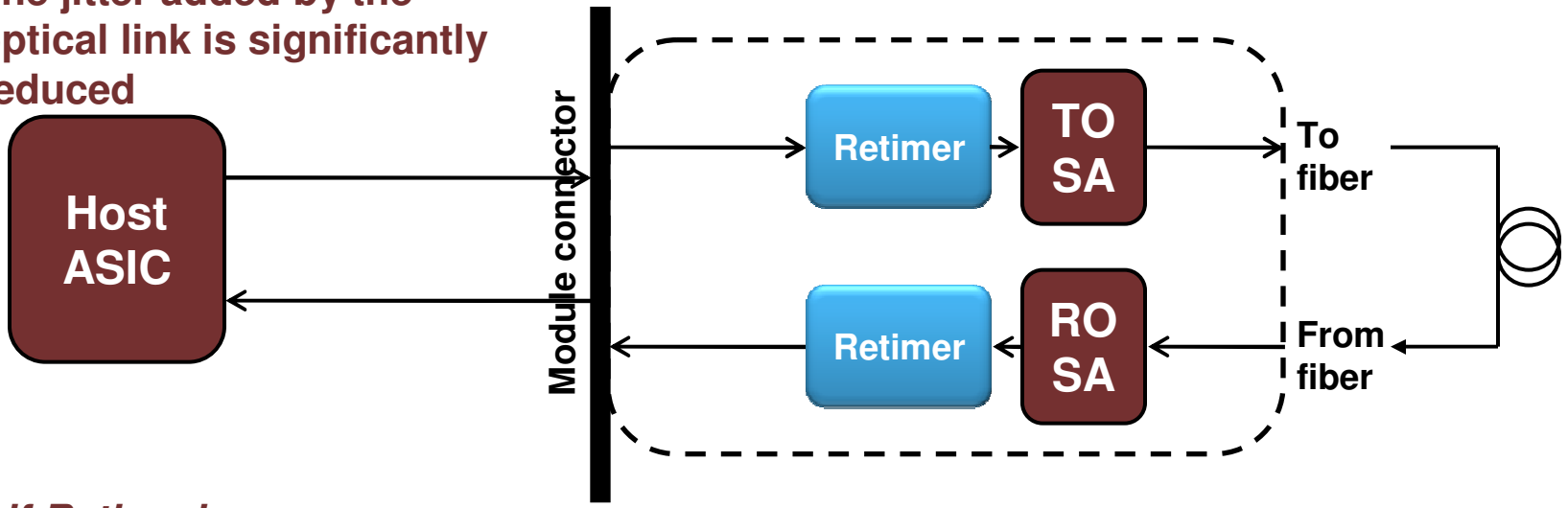
		SFP+ QSFP	Next Gen SFP+	CFP2
Data Rate		10 Gbps	14 Gbps	25-28 Gbps
Connector	Sdd21@nyquist	0.2 dB	0.2dB	0.5-1.2 dB
Connector	Sdd11@nyquist	14-17 dB	17-20dB	8-14 dB
Target channel	Total insertion loss @ nyquist	6.5 dB	12dB	12dB

- **New connector technology targeted for CFP2 is a major improvement over SFP/QSFP**
- **This improvement is not sufficient to compensate for the 2.5X data rate increase**
- **This is a very challenging objective**

Retimed vs. Non-retimed Rx interface

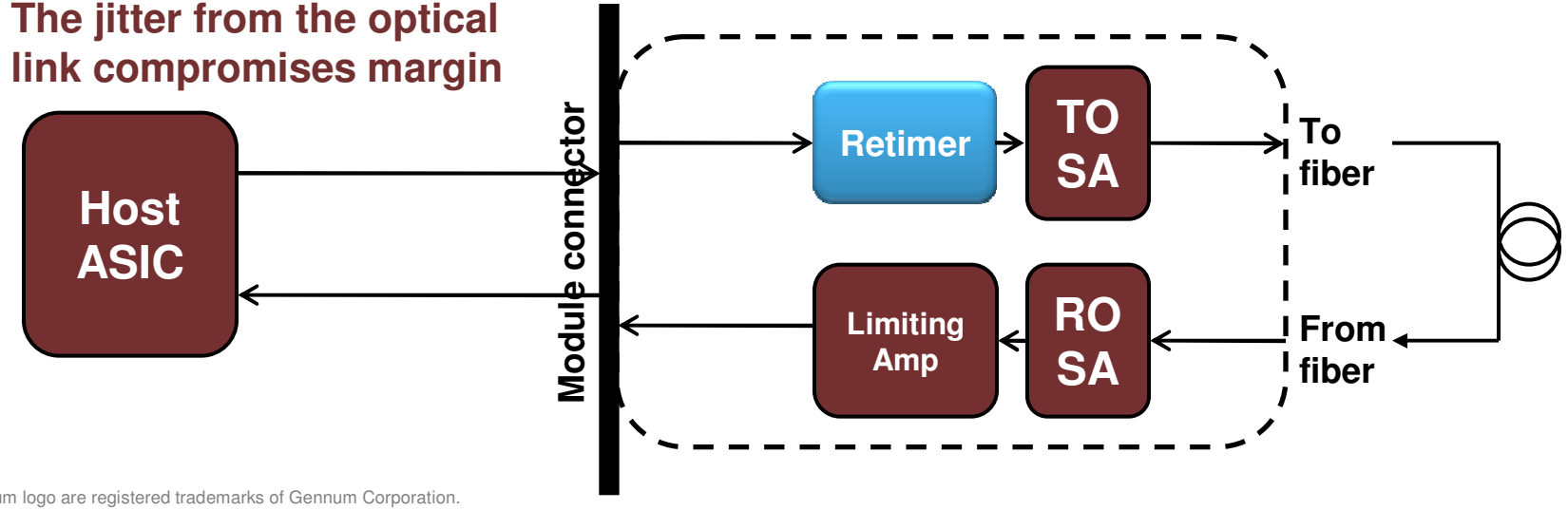
Full Retimed

- **The jitter added by the optical link is significantly reduced**

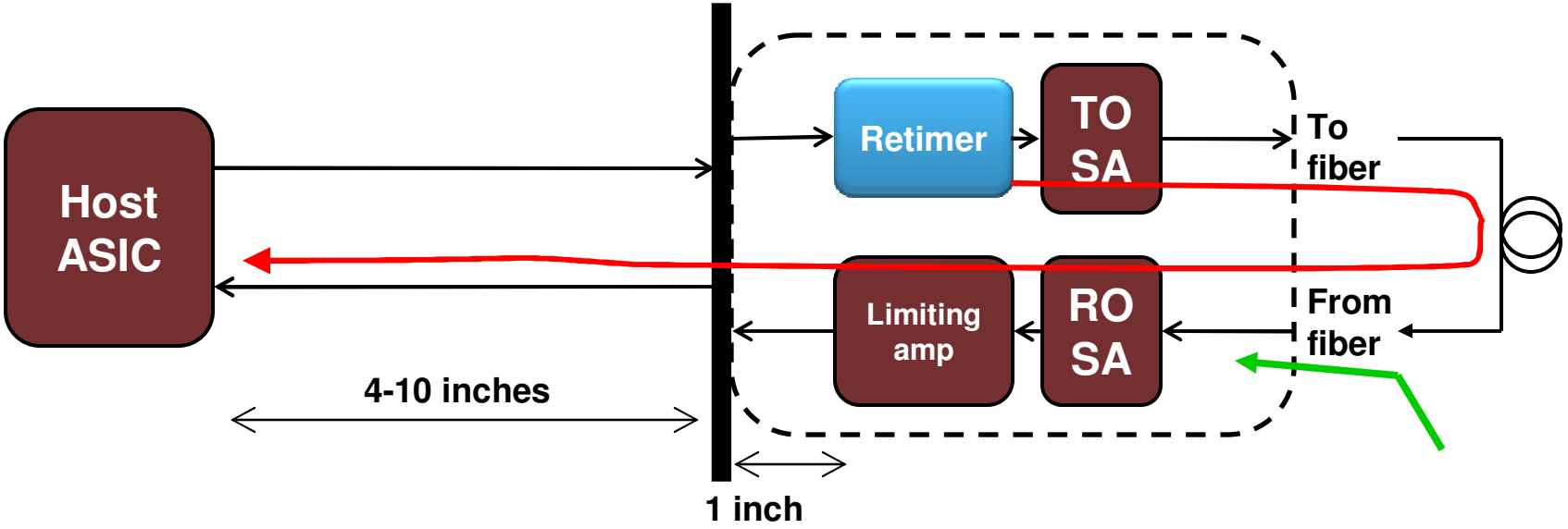


Half-Retimed

- **The jitter from the optical link compromises margin**



Non-retimed Rx interface with 4-10” to ASIC

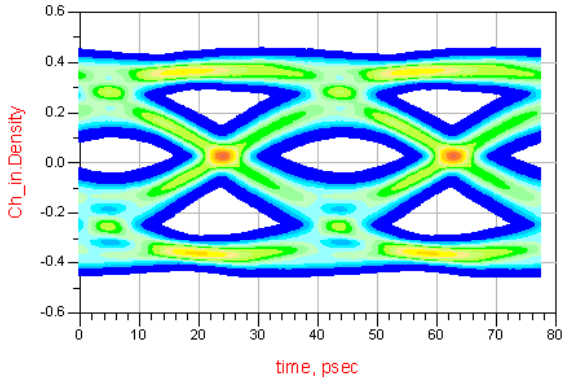


- **Red path is accumulating a lot of jitter before the ASIC can retime it**
- **Insertion loss is up to ~17dB at nyquist**
- **Stressed eye optical source as described in table 88-8 is injected at the optical input of the module (green arrow)**
- **ROSA noise & LA jitter have NOT been included yet**

ASIC @ 10 inches, 17dB at Nyquist, un-retimed Rx path

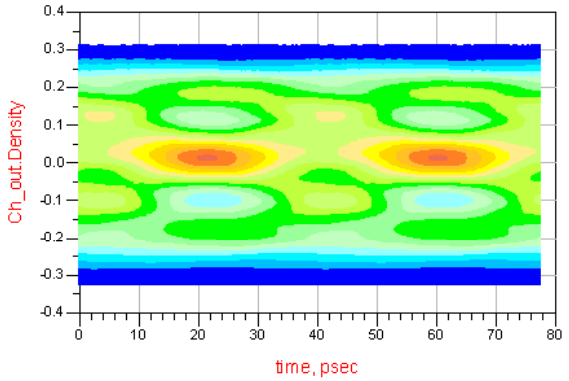
Module Connector

measurement	Ch_in.Summary
Level1	0.280
Level0	-0.250
Amplitude	0.530
Height	0.105
Width	2.463E-11
RiseTime	2.667E-11
FallTime	2.579E-11
JitterPP	1.181E-11
JitterRMS	2.361E-12
WidthAtBER	1.144E-11
HeightAtBER	0.053



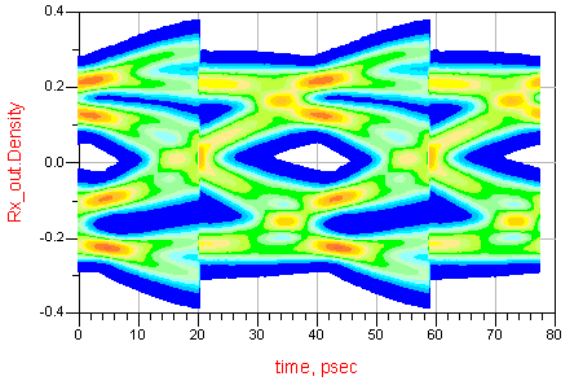
ASIC input

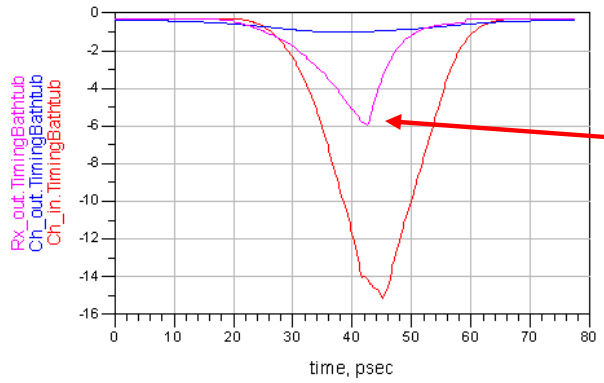
measurement	Ch_out.Summary
Level1	0.000
Level0	0.000
Amplitude	0.000
Height	0.000
Width	0.000
RiseTime	0.000
FallTime	0.000
JitterPP	0.000
JitterRMS	0.000
WidthAtBER	0.000
HeightAtBER	-0.257

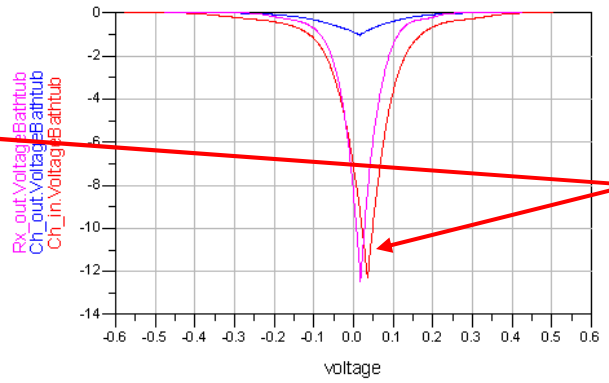


After DFE

measurement	Rx_out.Summary
Level1	0.172
Level0	-0.159
Amplitude	0.331
Height	0.055
Width	4.848E-12
RiseTime	2.324E-11
FallTime	2.298E-11
JitterPP	2.831E-11
JitterRMS	5.661E-12
WidthAtBER	5.042E-12
HeightAtBER	0.017





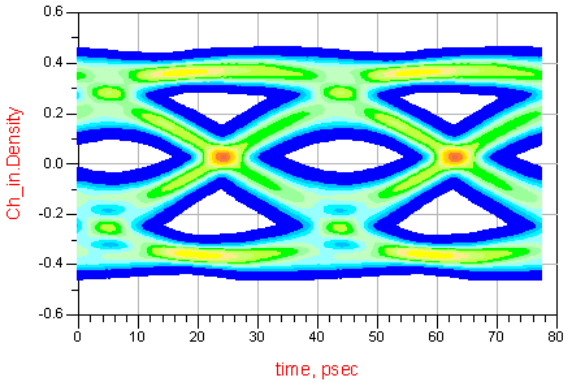


DFE has no margin even without ROSA & LA noise

ASIC @ 6 inches, 12dB at Nyquist, un-retimed Rx path

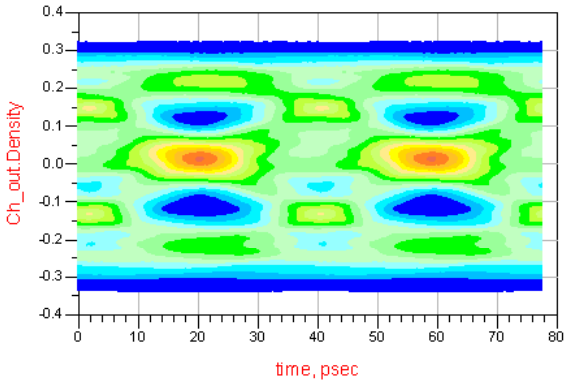
Module Connector

measurement	Ch_in.Summary
Level1	0.281
Level0	-0.249
Amplitude	0.530
Height	0.106
Width	2.424E-11
RiseTime	2.659E-11
FallTime	2.573E-11
JitterPP	1.219E-11
JitterRMS	2.438E-12
WidthAtBER	9.309E-12
HeightAtBER	0.038



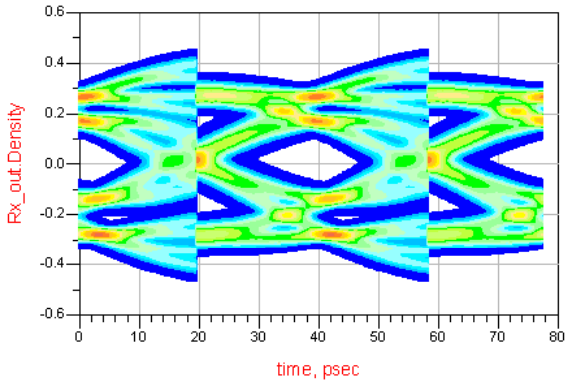
ASIC input

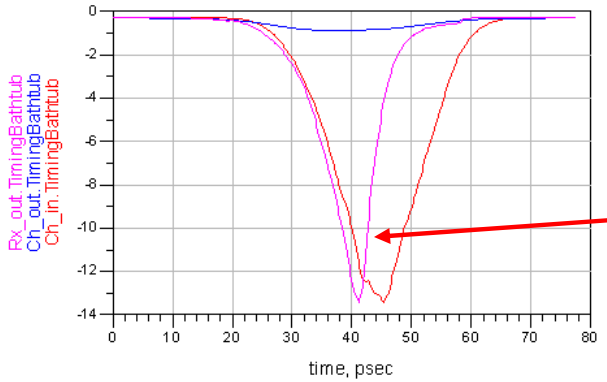
measurement	Ch_out.Summary
Level1	0.122
Level0	-0.161
Amplitude	0.283
Height	0.000
Width	0.000
RiseTime	2.323E-11
FallTime	2.208E-11
JitterPP	3.879E-11
JitterRMS	9.950E-12
WidthAtBER	0.000
HeightAtBER	-0.172

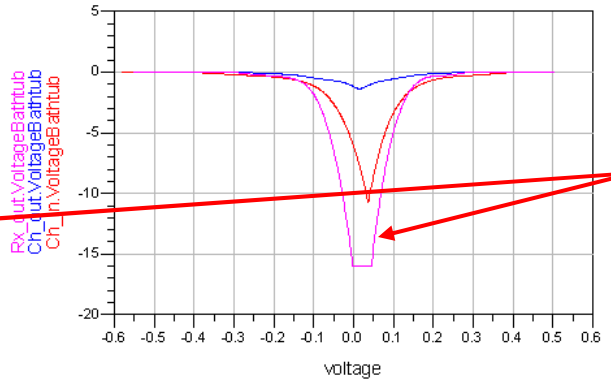


After DFE

measurement	Rx_out.Summary
Level1	0.217
Level0	-0.205
Amplitude	0.422
Height	0.091
Width	1.008E-11
RiseTime	2.267E-11
FallTime	2.321E-11
JitterPP	2.535E-11
JitterRMS	5.069E-12
WidthAtBER	1.067E-11
HeightAtBER	0.092

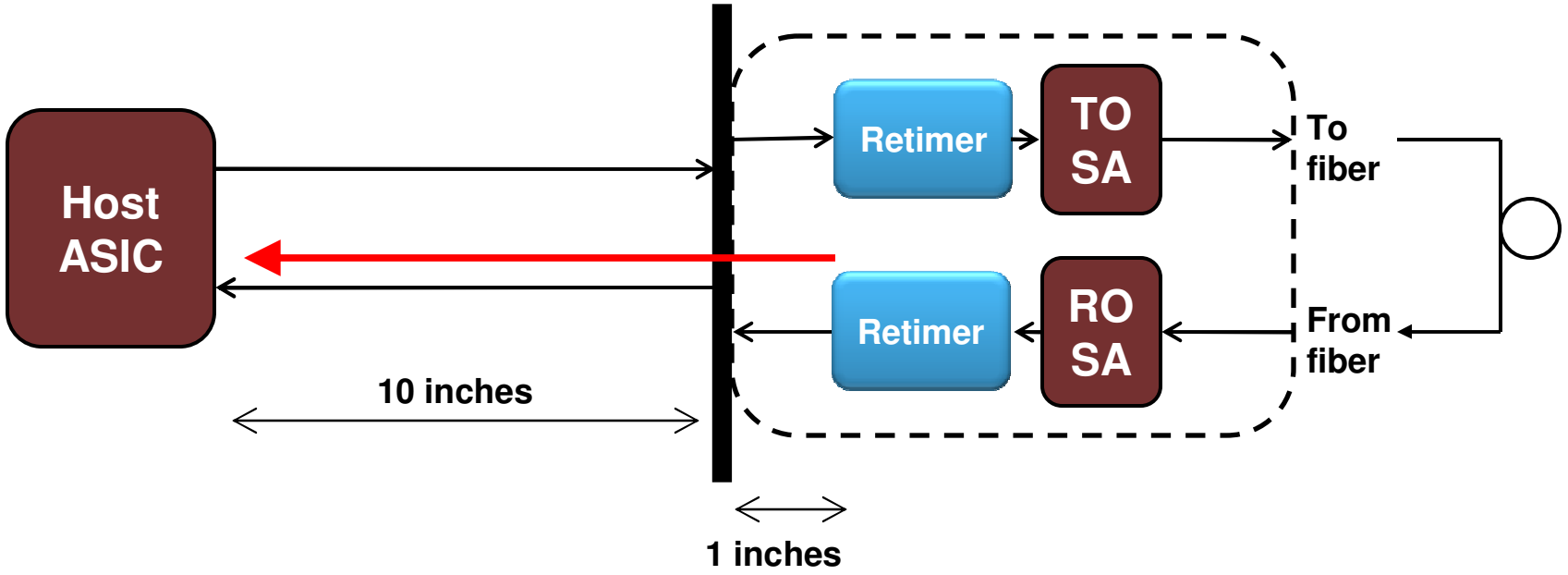






DFE has no margin even without ROSA & LA noise

Retimed Rx interface with 10” from module to ASIC



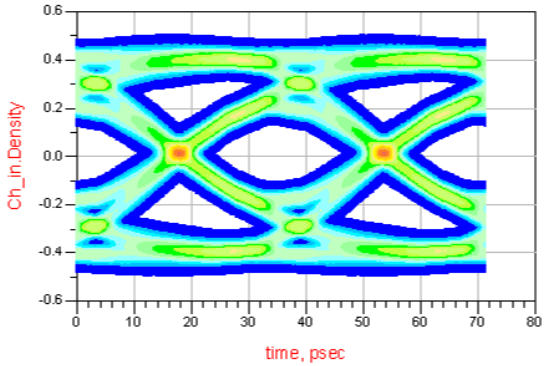
- **Module retimer can handle optical jitter**
- **Red path is a clear transmission line**
- **ASIC DFE can efficiently retime the link from the module**
- **DFE will be able to work over 10 inches and more**

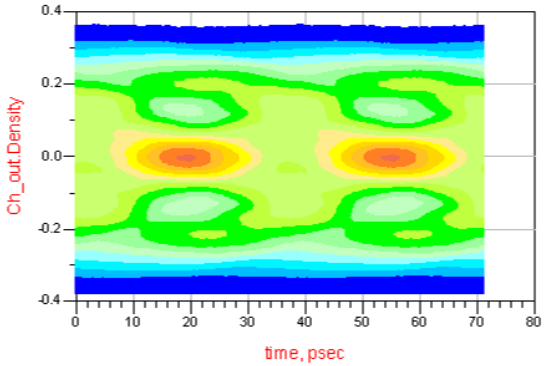
Full retimed module with 10” to ASIC

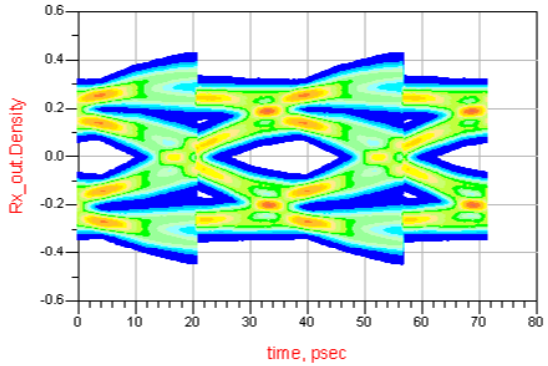
measurement	Ch_in.Summary
Level1	0.307
Level0	-0.291
Amplitude	0.598
Height	0.202
Width	2.446E-11
RiseTime	2.440E-11
FallTime	2.456E-11
JitterPP	9.417E-12
JitterRMS	1.883E-12
WidthAtBER	1.946E-11
HeightAtBER	0.190

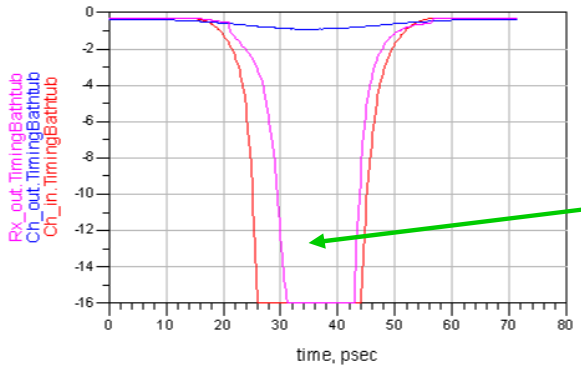
measurement	Ch_out.Summary
Level1	0.121
Level0	-0.148
Amplitude	0.268
Height	0.000
Width	0.000
RiseTime	1.864E-11
FallTime	1.844E-11
JitterPP	3.571E-11
JitterRMS	9.523E-12
WidthAtBER	0.000
HeightAtBER	-0.265

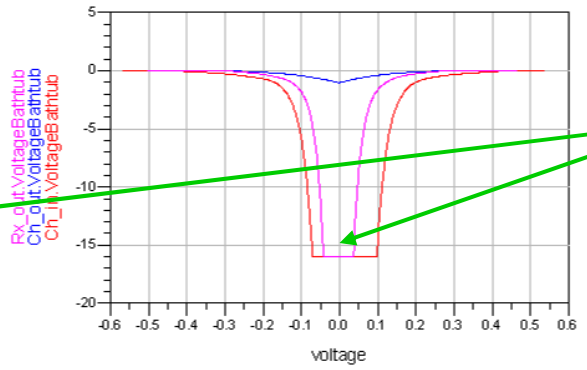
measurement	Rx_out.Summary
Level1	0.192
Level0	-0.203
Amplitude	0.395
Height	0.093
Width	1.786E-11
RiseTime	2.121E-11
FallTime	2.120E-11
JitterPP	1.524E-11
JitterRMS	3.049E-12
WidthAtBER	1.625E-11
HeightAtBER	0.112











DFE has enough margin, ROSA noise is not an issue

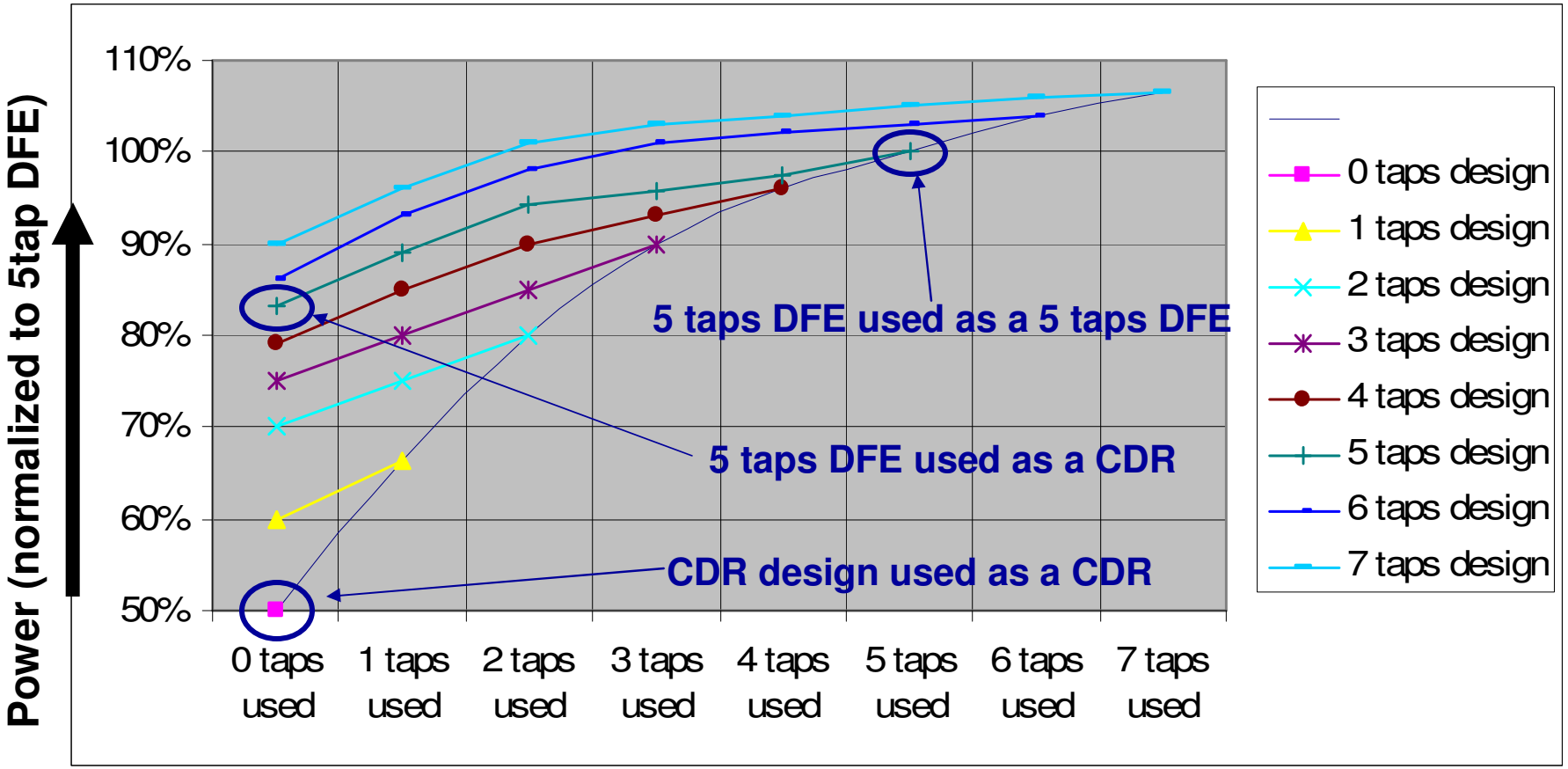
Summary

	Retimer in	PCB loss	line card distance	module distance	vertical eye	horizontal eye	Link
	Module	dB at Nyquist	inches	inches	mV	mUI	Margin
Case A	NO	17	10	1	17	129	very poor
Case B	NO	12	6	1	92	276	poor
Case C	YES	17	10	1	130	421	good

- **Next step is to add ROSA noise and other impairments**
- **This confirms initial intuition:**
  "this module will require full retiming."

POWER
CDR vs. DFE vs. Limiting Amp

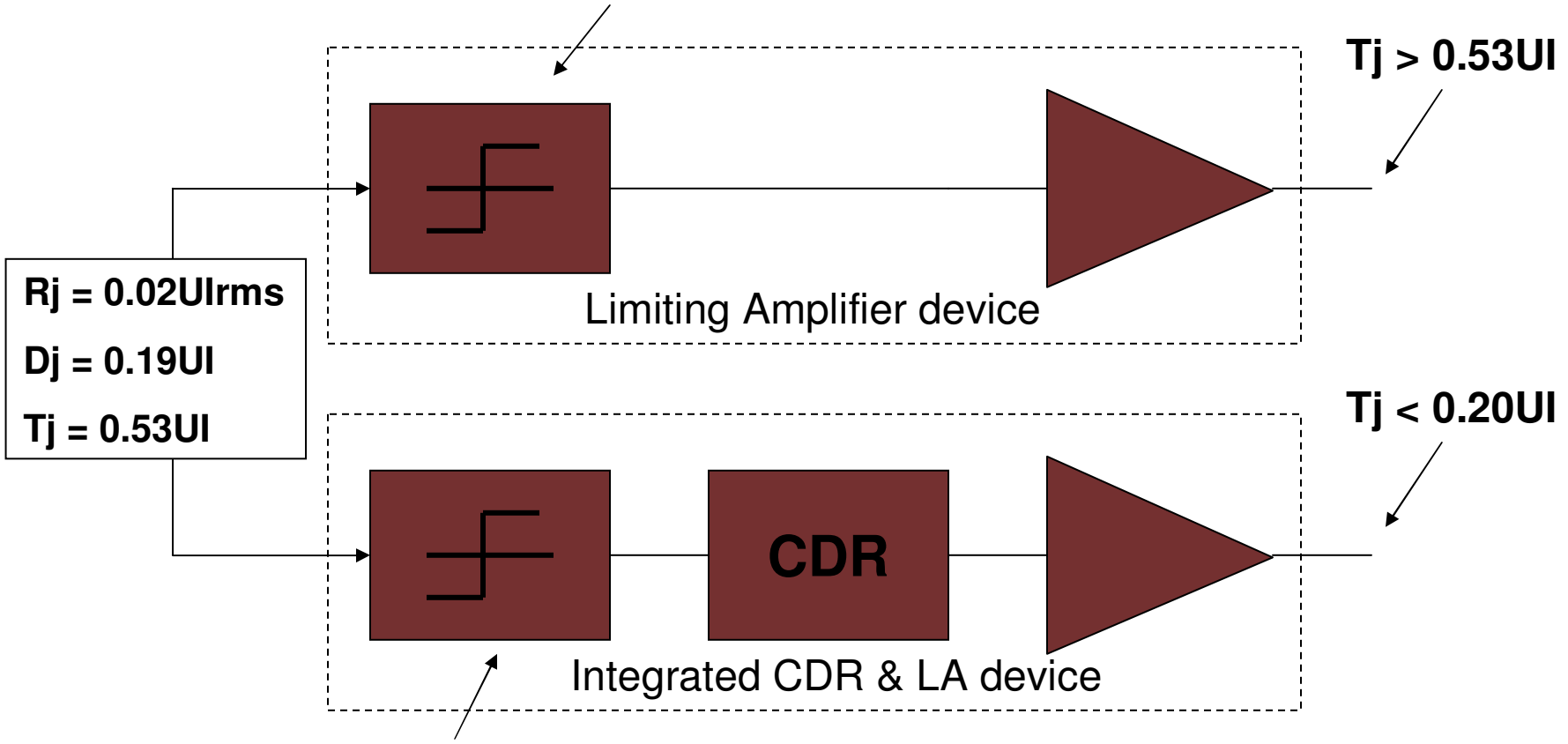
Power of DFE design used as a CDR



- **Unused DFE taps are not free**

Limiting amp vs CDR design

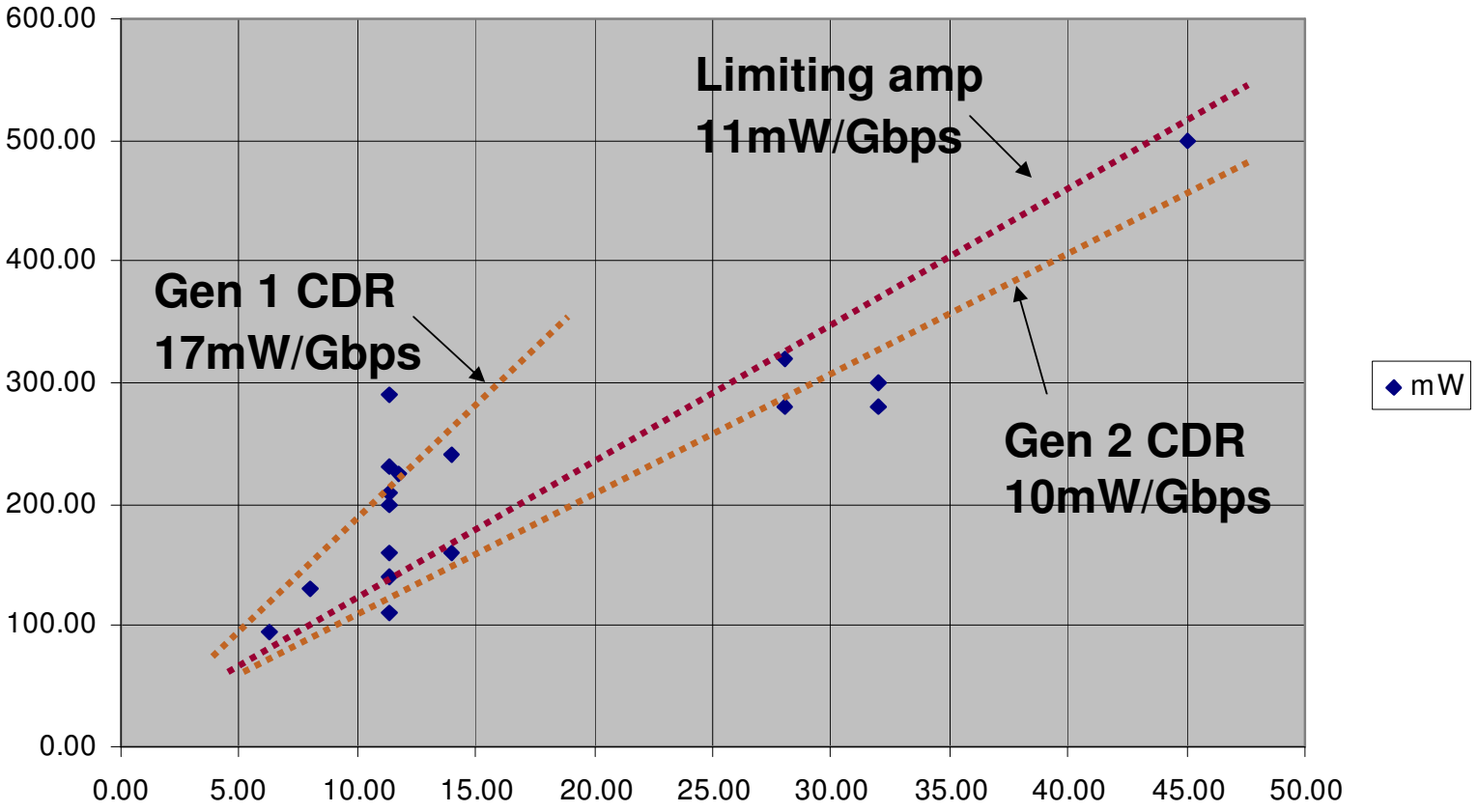
- **Large current required to minimize additive jitter**



- **Current can be reduced since any additive jitter will be removed**
- **Job of the limiting amp is to increase the amplitude at the sampling point**
- **Enables the CDR+LA design to be similar power to than stand alone LA**

Industry survey CDR

CDR+LA & LA
device power (mW) vs datarate (Gbps)



Conclusion

- **CFP2 Module will require full retiming to manage the optical impairments**
- **Power of full-retimed module is virtually equal to half-retimed module with limiting amplifier in the Rx path**