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# Power Considerations
# IEEE OIF Liaison

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# Outline

- Dual Power Supply Proposal for New Connectors
- Power of DFE design used as a CDR
- Summary

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# *Dual Power Supply Proposal*

# Connector pin definition

- The OIF CEI Workshop in Santa Clara (February 2010) highlighted power density in the module as a large concern.
- Leverage State of the Art
  - Latest CMOS reduces geometries and IC core power with lower power supply voltages
    - Reduce heat density in module
    - Reduce real estate in module
- BUT….
  - Current Module Pin assignments not provisioned for lower power supplies

# Dual Power Supply Proposal

**Propose dual power supply into new connector pin definition: 1.2V and 3.3V**

- Avoids using DC-DC regulator for CMOS CDR technology
  - Extra power
  - Extra real-estate including support components
- 1.2V works well for optical AND copper modules

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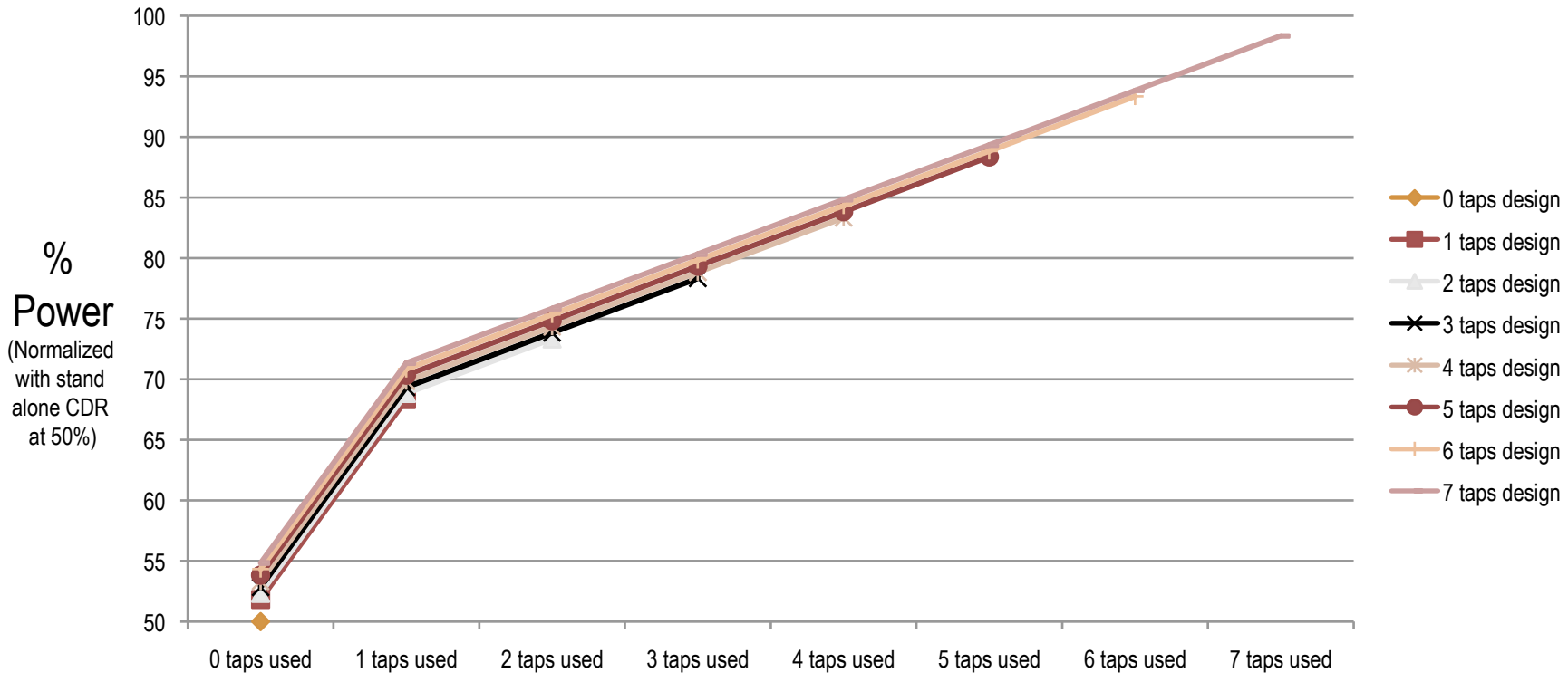
# *Power of DFE Design*

# Power of DFE design used as a CDR




- Equalizer can be designed to shut off unused DFEs w/ ~10% penalty per unused tap
- Unused DFE taps are essentially free

# Summary

- Propose dual power supply into new connector pin definition: 1.2V and 3.3V to take advantage of lower power CMOS IC in the module
- DFE architecture can make unused DFEs turn off with negligible power