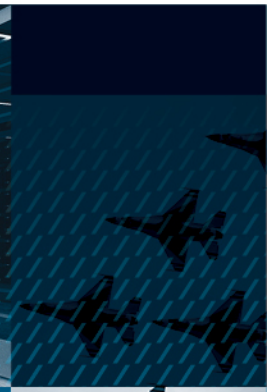
MACOM™

Partners from RF to Light

SERDES for 100Gbps



May 24, 2017

Bart Zeydel, Francesco Caggioni, Tom Palkert

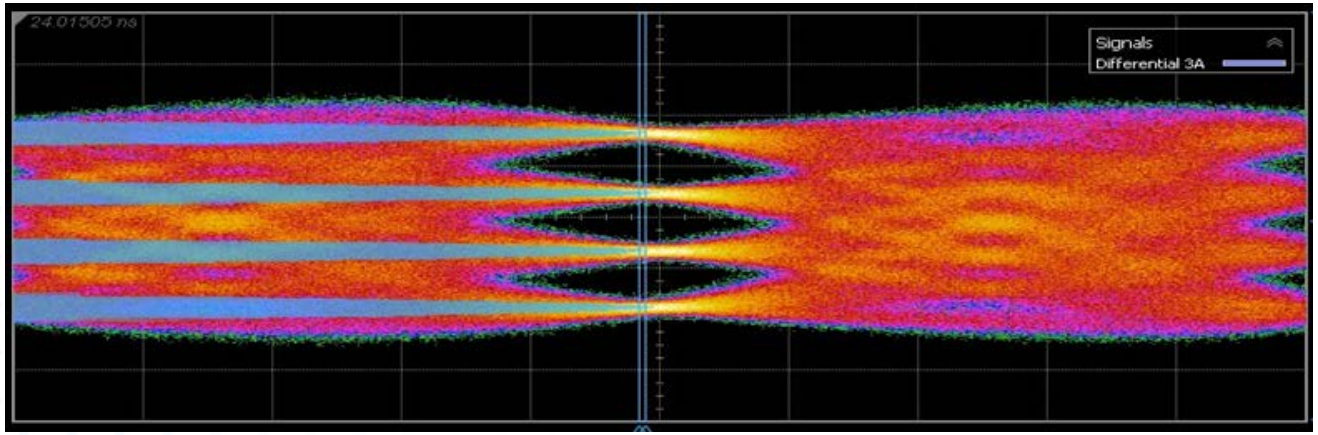
Outline

- Narva
  - 16nm FinFET CMOS transceiver for demonstrating 100GE PAM-4 links
  - 100GE single λ link measurements
    - SERDES interface operating at 53.125GBaud PAM-4
- CEI-112G VSR PAM-4
  - System analysis
  - Narva Measurements
  - Considerations
- Conclusions

Narva:
Proof of Concept Vehicle for 100Gbps SERDES

- Narva
  - DSP
    - Tx and Rx Equalization
    - PRBS31 generator and checker.
  - Data Converters ADC and DAC.
- Enables >100Gbps on a single differential pair using PAM-4

- DAC output @53.125GBaud



Narva Optical Link Set-Up

Single λ100 Gbps
Narva Eval Board

Linear Driver:

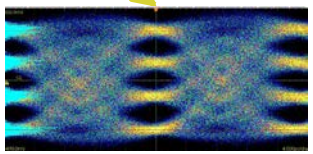
Laser

1550nm

Splitter

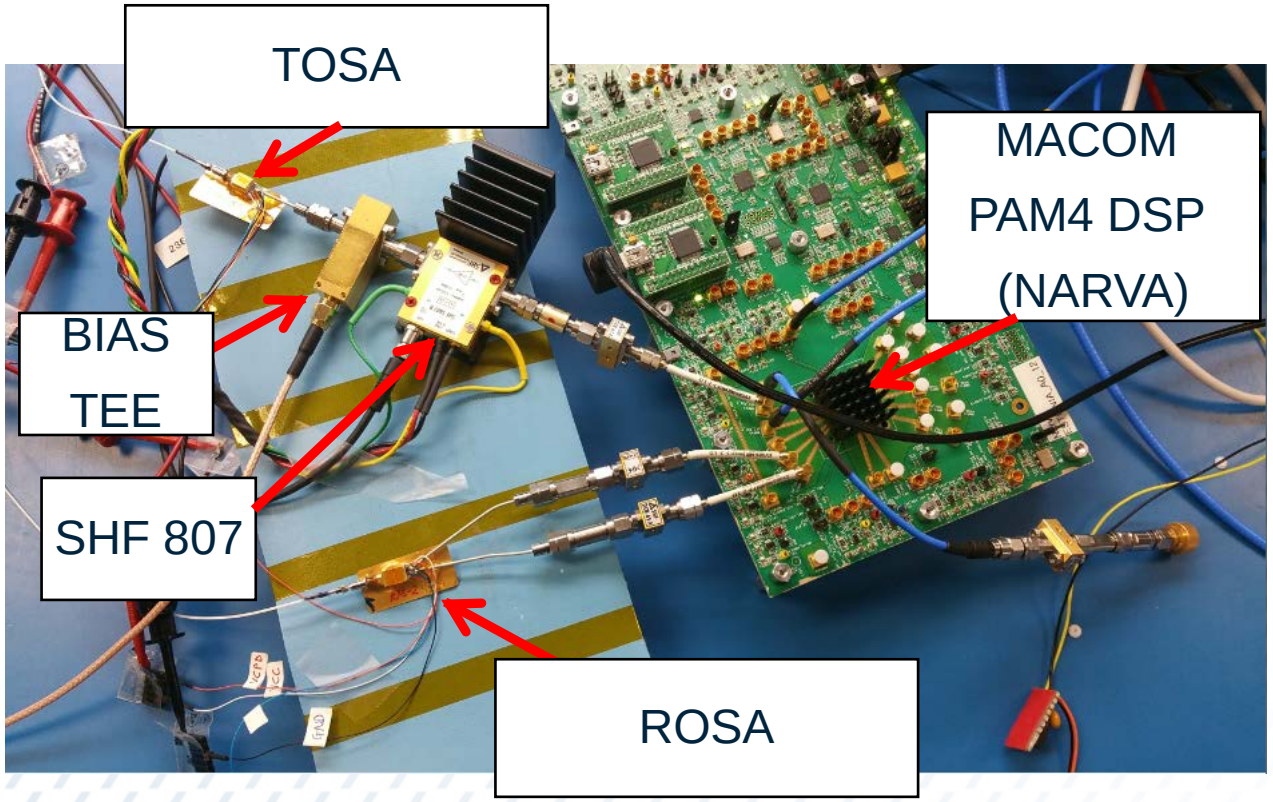
PD +
Linear TIA

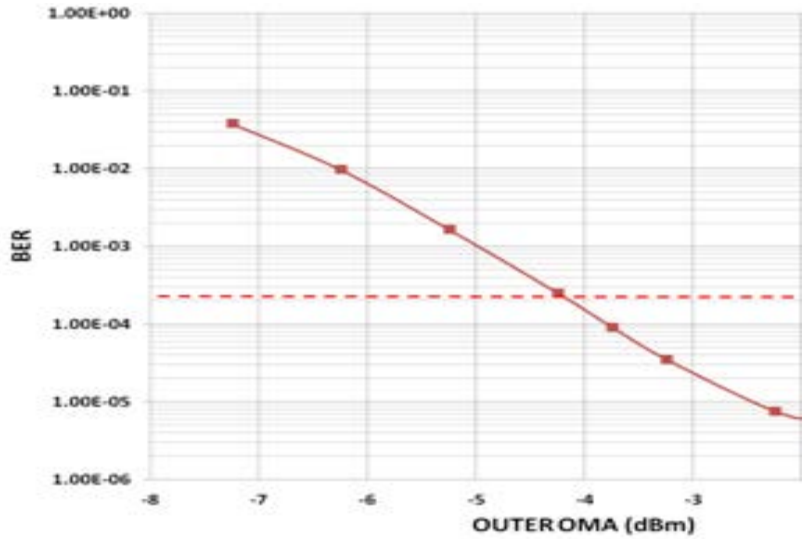
VOA



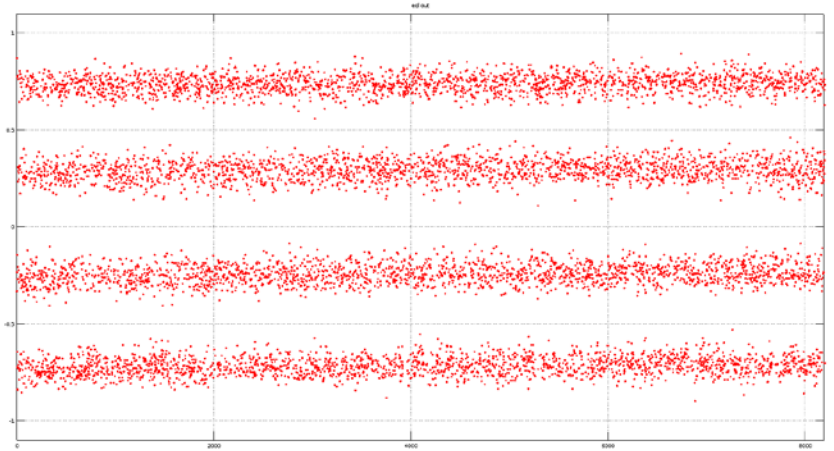
MACOM Integrated Optical Development Platform:

MACOM PAM-4 DSP (Narva), Bias TEE, SHF 807 linear Driver, TOSA, ROSA



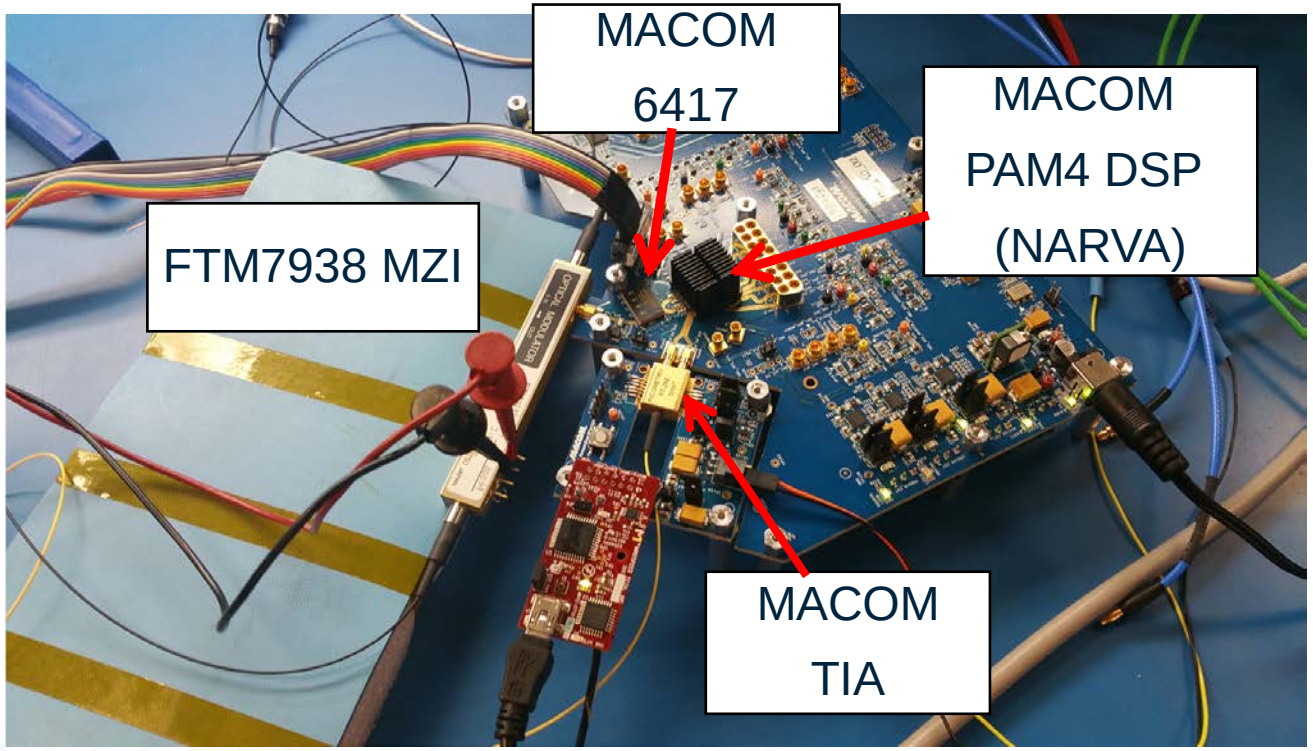


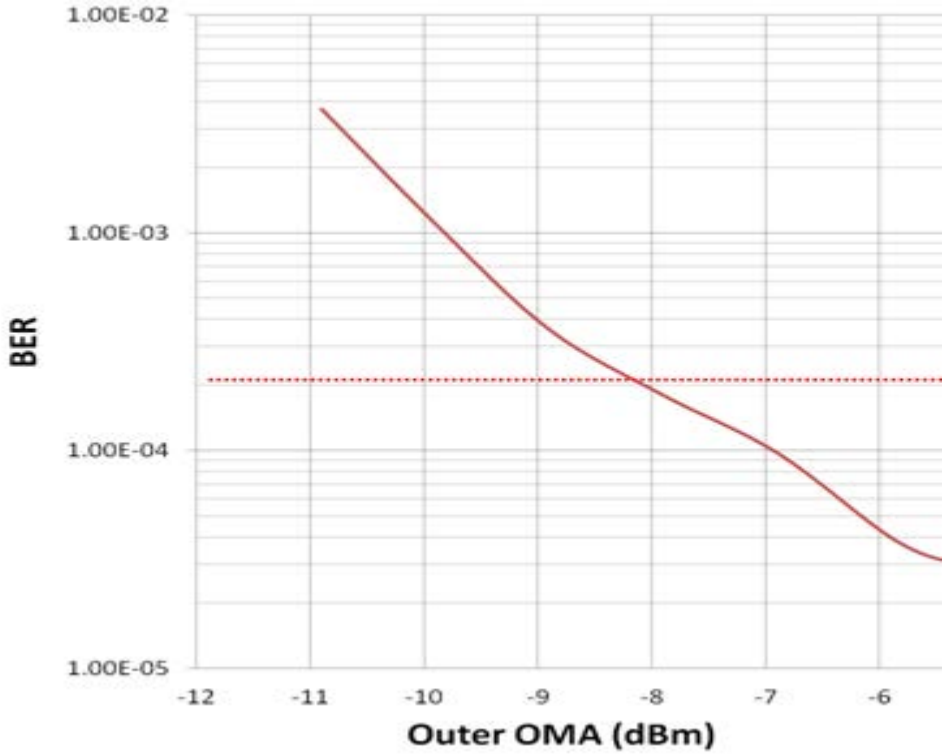
Equalizer Output



MACOM Integrated Optical Development Platform:

MACOM PAM-4 DSP (Narva), MACOM 6417 linear Driver, MACOM TIA Fujitsu FTM7938 MZI

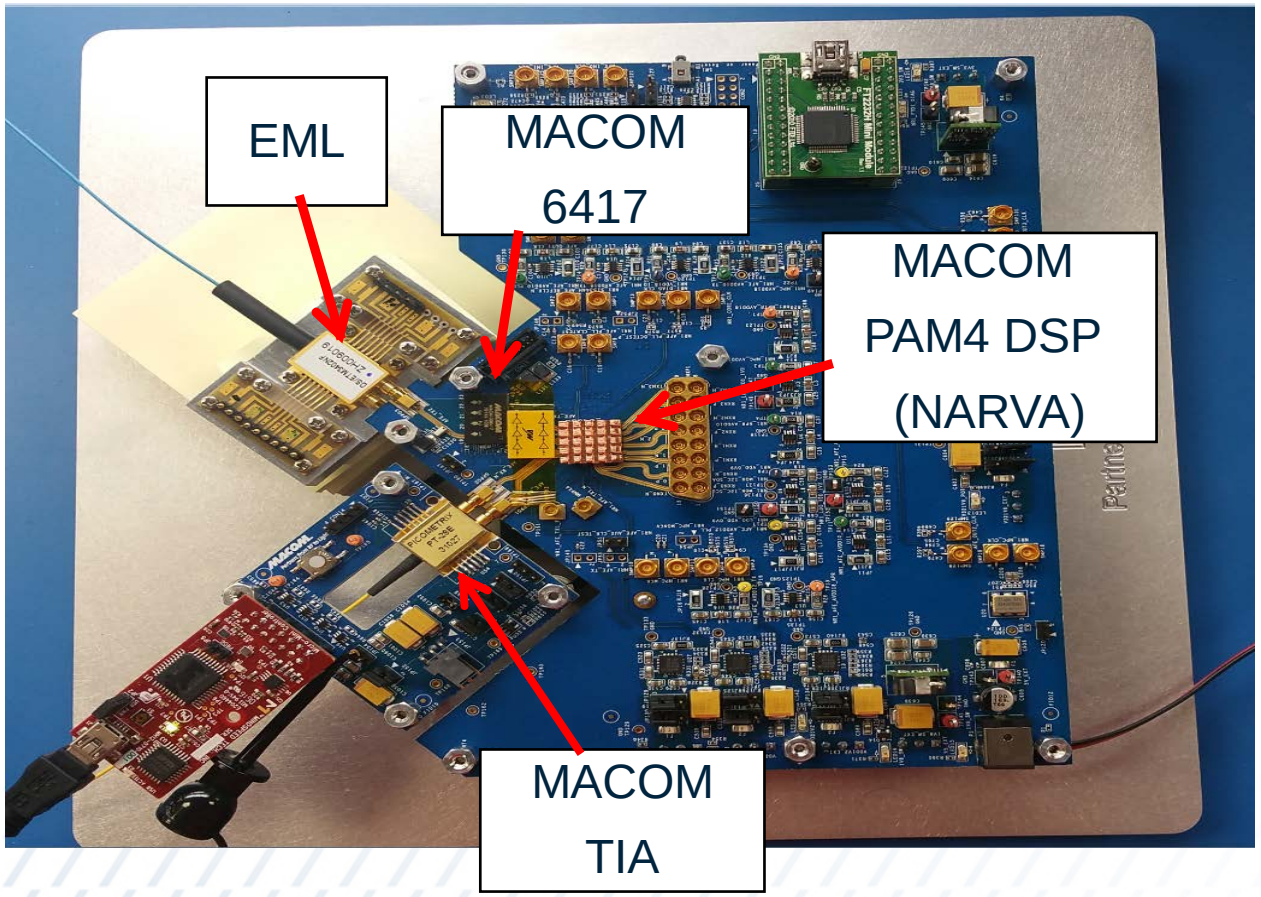




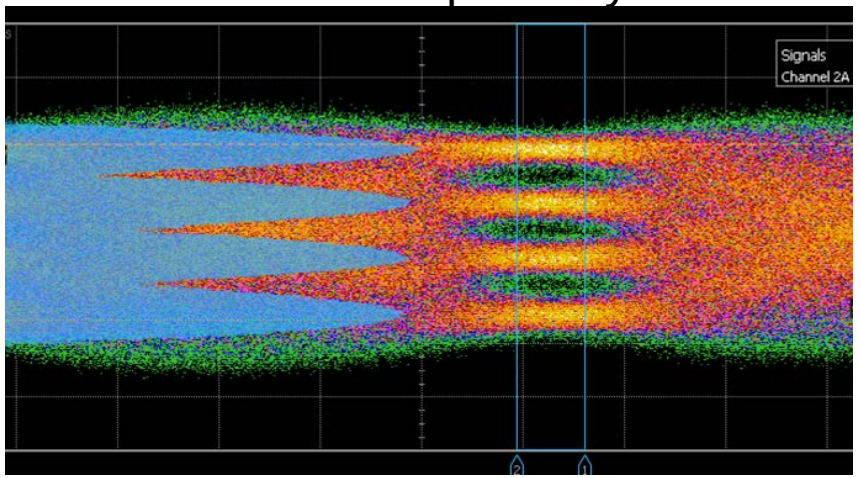
- 1550nm with patch fiber connected to VOA
- Rx Sensitivity ~-8 dBm Outer OMA for KP4-FEC threshold

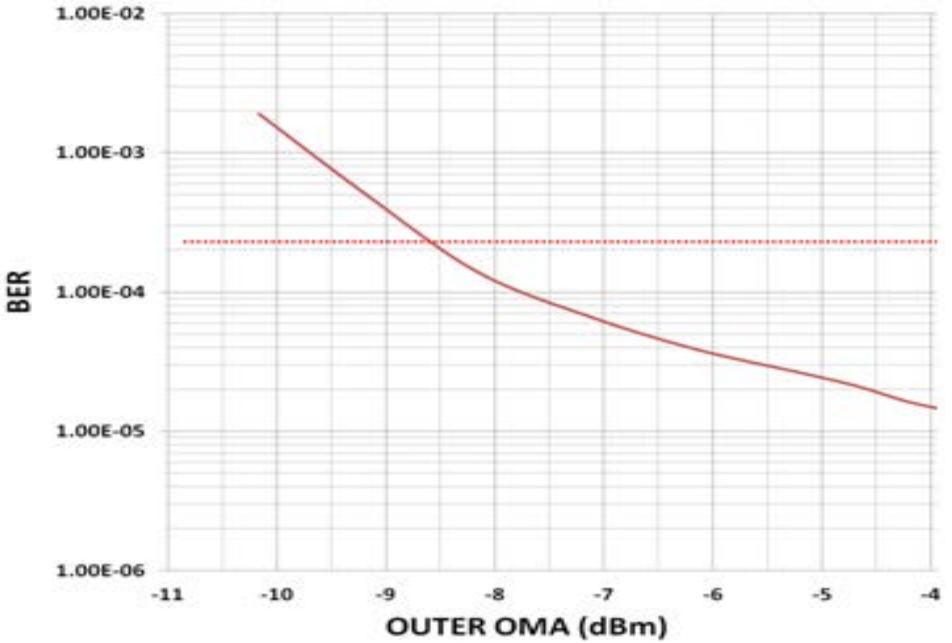
MACOM Integrated Optical Development Platform:

MACOM PAM-4 DSP (Narva), MACOM 6417 linear Driver, MACOM TIA, EML



PAM-4 Optical Eye

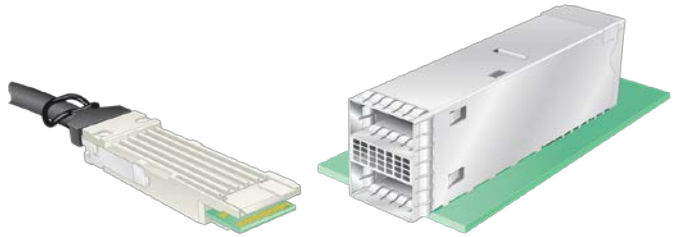




- 1310nm with patch fiber connected to VOA
- Rx Sensitivity ~-8.5 dBm Outer OMA for KP4-FEC threshold

100GE Single Lambda demonstrated

- 100GE single λ links demonstrated
- Applications:
  - 100GE single λ solutions in QSFP28
    - 1x100GE single λ
  - 400GE QSFP-DD and OSFP modules
    - 4x100GE single λ optical interface
    - CEI-56G VSR PAM-4 host interface
  - Next Generation OSFP modules intend to target 800Gbps
    - 8 bi-directional differential pairs comprise the host interface
      - CEI-112G-VSR is required to enable this solution
- Performance demonstrated for 100GE single λ support use in 100GE and 400GE modules
  - Preliminary results show Rx Sensitivity sufficient for 2km
  - Potential exists to extend reach further



QSFP-DD

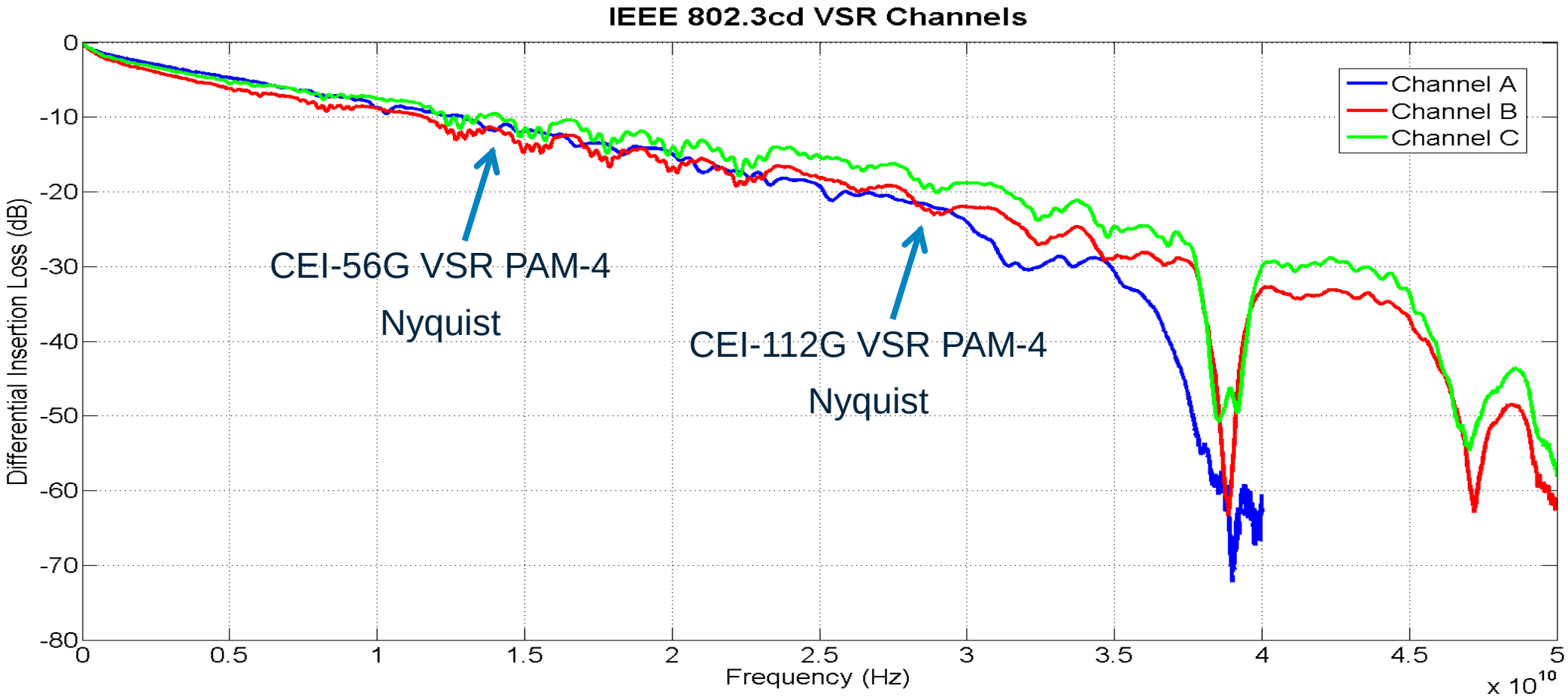
http://www.qsfp-dd.com/

CEI-112G VSR PAM-4

CEI-112G VSR PAM-4

- Preliminary CEI-112G VSR PAM-4 system analysis
  - System Assumptions
  - Analysis performed on existing CEI-56G VSR channels
  - Measurements
  - Considerations

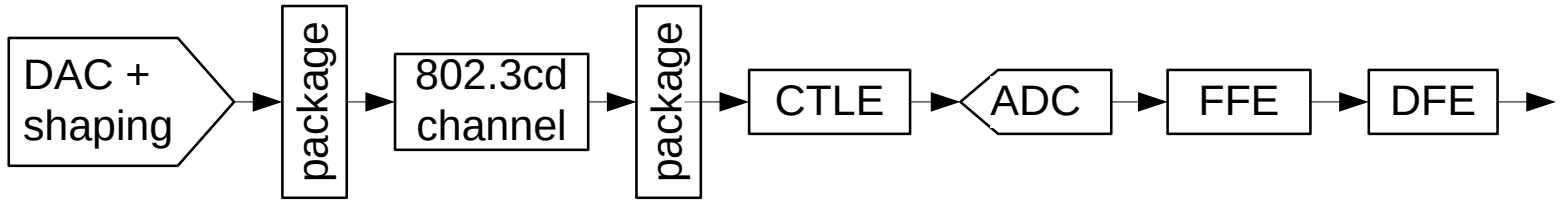
CEI-56G-VSR compliant channels



- Insertion Loss roughly doubles at Nyquist
- Insertion Loss deviation (ILD) increases
  - For VSR, ILD can significantly impact the equalization requirements

[1] IEEE 802.3cd Channel Data http://www.ieee802.org/3/cd/public/channel/index.html

System Assumptions for analysis



- 56GBaud PAM4
- Tx/Rx BW = 28GHz
- Transmit shaping 3-tap FIR (pre, post, main)
- 1dB-1.5dB package IL at 28GHz
- High-Frequency CTLE with 12dB peaking
- Low-Frequency CTLE
- ADC ENOB > 5 (5.5 in the following analysis)
- Crosstalk noise rms = 2.5mV
- 8/16/32/64/128 FFE taps + 1/3/5/15 DFE tap

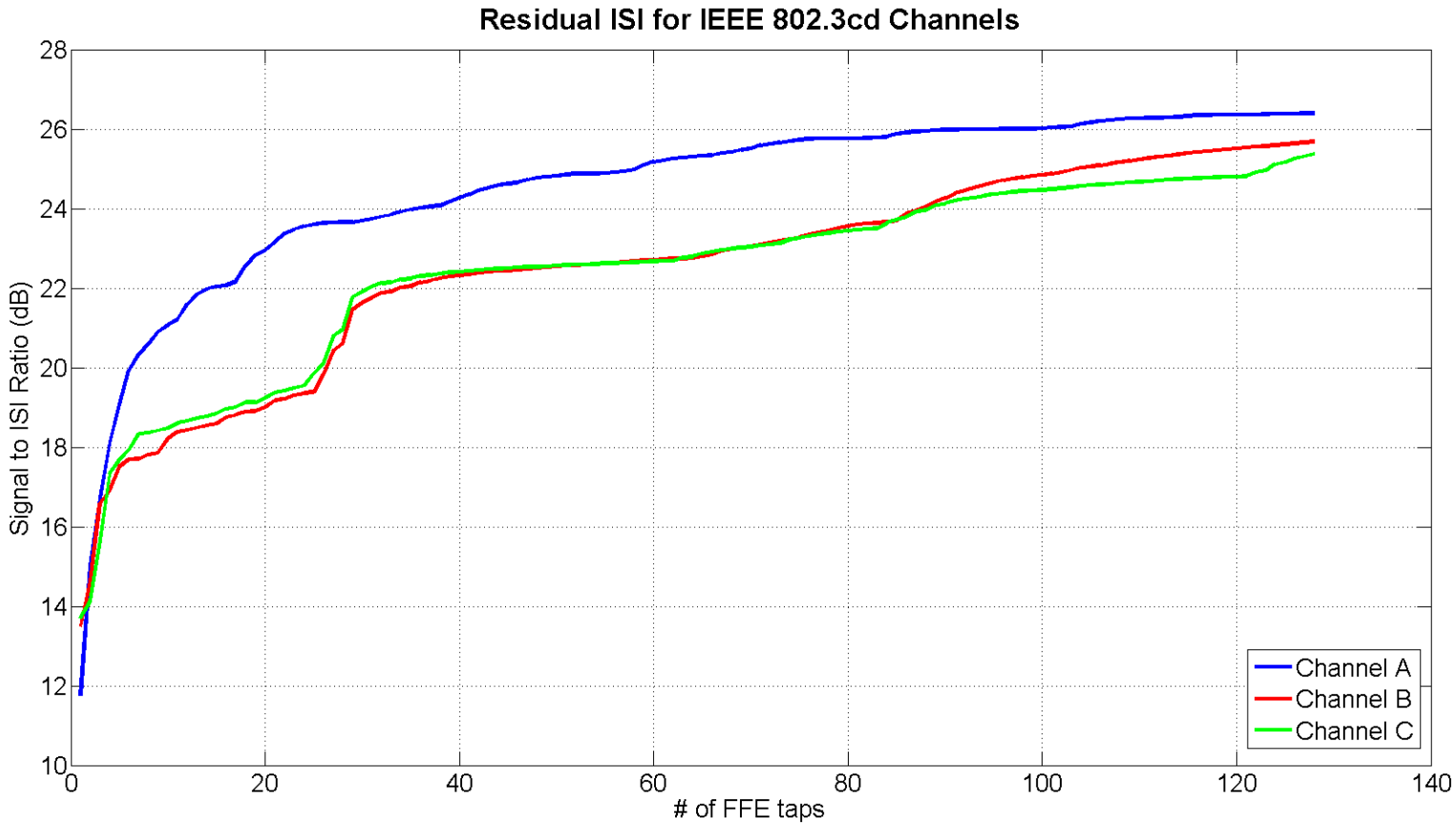
112G VSR PAM4 System Performance Analysis

- SNR margin with respect to BER target of 1e-6 shown in table (SNR target = 20.4 dB).
  - Ideally achieve 3dB SNR margin (23.4 dB)

SNR margin (1 DFE tap)	Channel A	Channel B	Channel C
8 FFE taps	-0.4dB	-2.9dB	-2.3dB
16 FFE taps	0.7dB	-2.0dB	-1.7dB
32 FFE taps	2.2dB	0.6dB	1.1dB
64 FFE taps	3.2dB	1.3dB	1.7dB
128 FFE taps	3.8dB	3.3dB	3.7dB

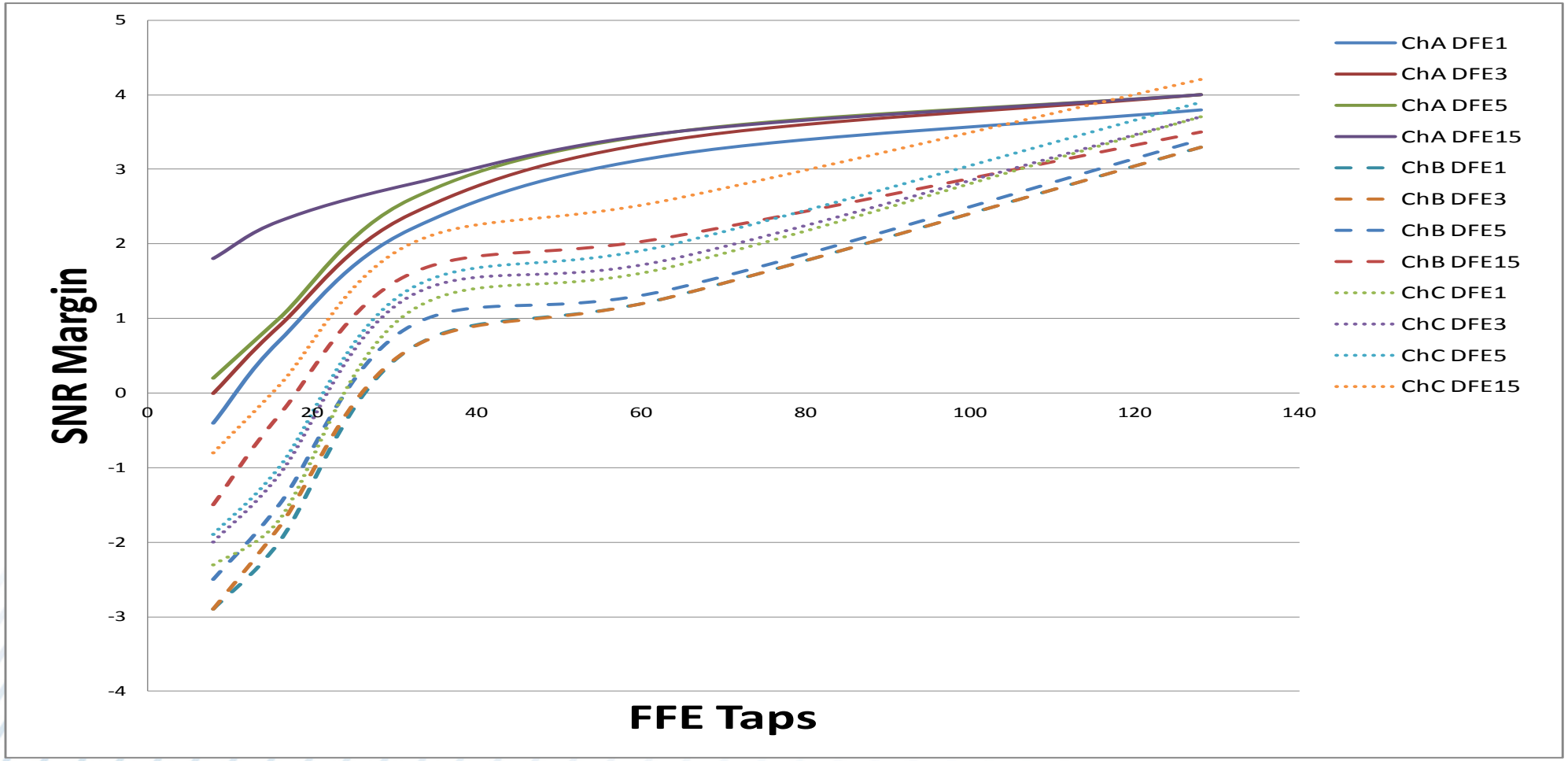
- 3dB margin only obtained with impractically long equalizer.
  - Primarily due to ILD
- Better performance for smoother TE channel, which was designed for improved ILD, RL and noise.

Residual ISI for 802.3cd channels vs. FFE taps with 1-tap DFE



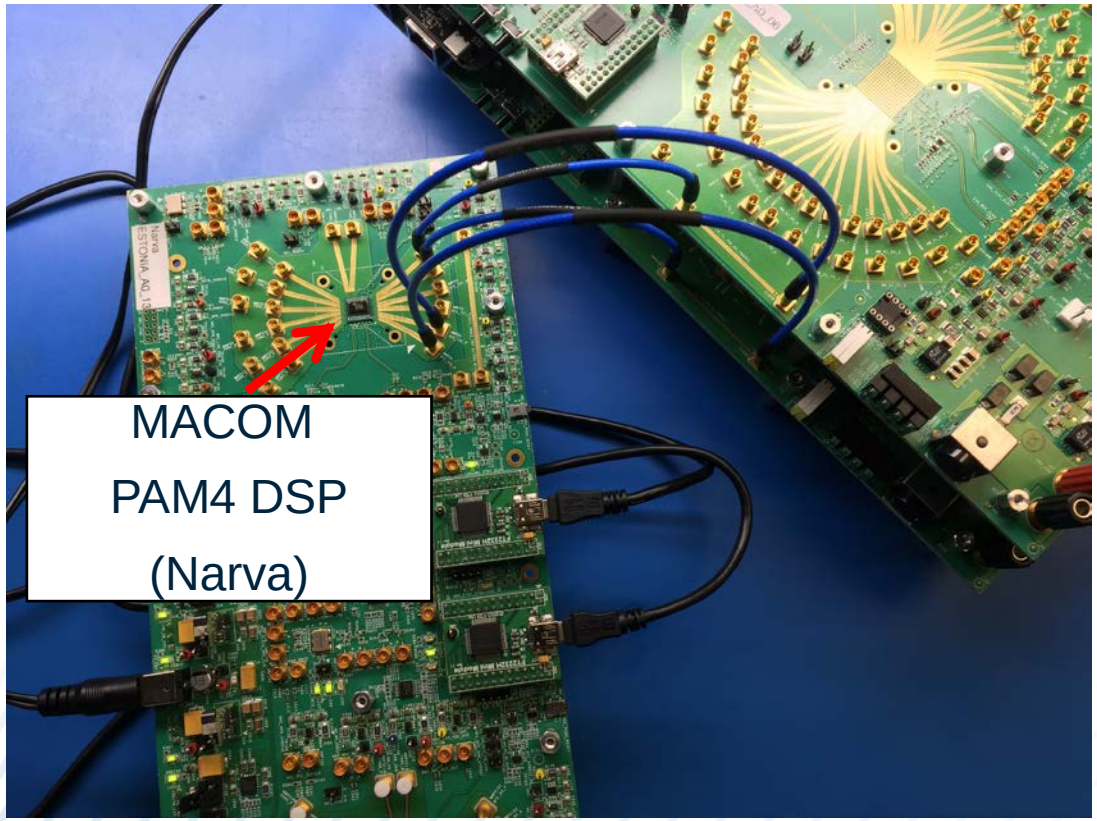
- Plot residual ISI of the end-to-end responses as a function of the number of FFE taps
  - includes packages at both ends of the link, AFE responses, CTLE
- Ch. A which was designed to improve ILD, RL and noise
  - Reduces equalization complexity

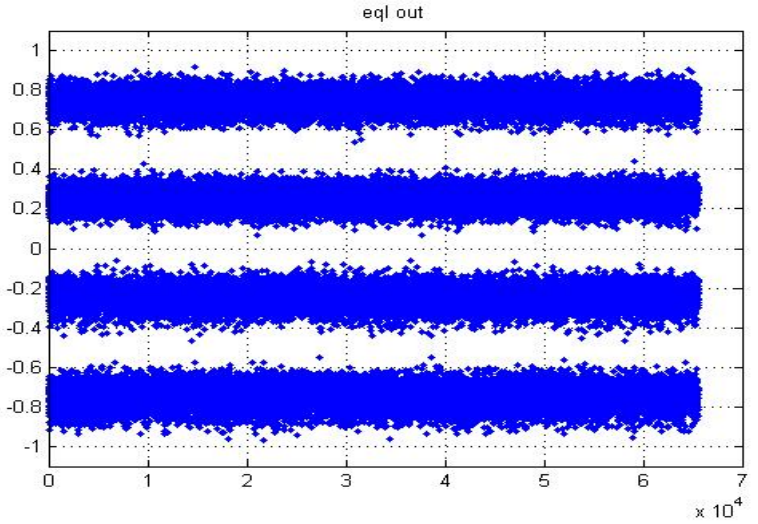
SNR Margin for BER 1E-6
FFE taps and DFE taps for 802.3cd channels

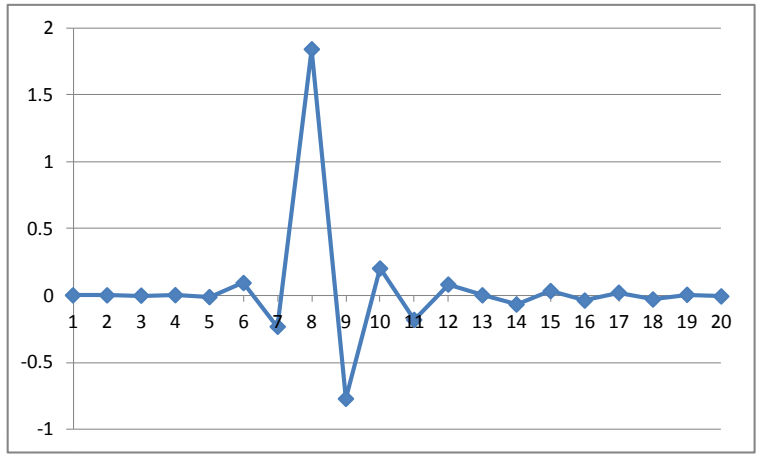


- Increasing DFE taps doesn't significantly reduce FFE taps in Ch.B and Ch. C.
  - Ripple in IL for Ch. B and C requires long FFE

Narva
100GE PAM-4 Measurement @53.125GBaud



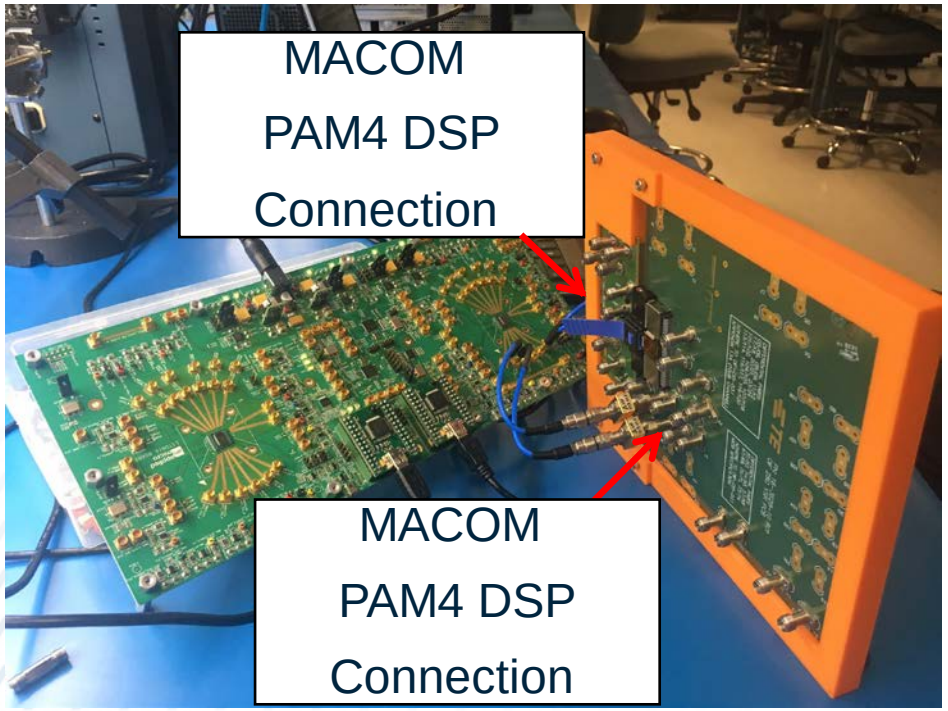




BER < 7E-7

Narva with TE sliver Connector
100GE PAM-4 Measurement @53.125GBaud

- 53.125 GBaud PAM 4 transmit performance evaluated with MACOM Narva, connector and trace board using the TE sliver connector recently selected for use in the COBO MSA.
- BER < 6e-7



Preliminary Power Considerations for CEI-112G VSR

- Target Power for CEI-112G VSR:
  - Should be < 2*CEI-56G-VSR PAM-4
    - CEI-56G-VSR PAM-4 tentatively in the range of 170-300mW/lane (~3-5pJ/bit)
    - Target *350mW* for CEI-112G VSR PAM-4
- CEI-112G VSR PAM-4 Power
  - ADC – Current designs operating at > 10GS/s trending towards ~3-10pJ/sample

    Source: B. Murmann, "ADC Performance Survey 1997-2016," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.
  - FFE - Simplified Complexity model, treat each tap as a Multiply-accumulate (MAC) operation
    - 32-tap FFE * 56GBaud = 1.79 trillion MAC operations per second
      - Assuming 5 trillion MACs/W => 1.79E12 / 5E12 = *360mW* , 10 trillion MACs/W = *180mW*
  - DFE – power does not scale linearly with # of taps due to high operating rate, single tap typically consumes the same power as several FFE taps.
  - 4-level driver + Tx Equalization (pre, post) – power consumed is not negligible, however the channel characteristics are not anticipated to impact transmit requirements.

CEI-112G VSR SERDES Considerations

> CEI-112G VSR Considerations

- Performance
  - Operating at 112Gbps on current CEI-56G VSR channels is challenging
    - Analysis presented here shows need for CTLE, FFE, and DFE
  - Desirable to optimize channels to improve operating margin and simplify equalization requirements
    - Prior VSR links required only CTLE and possibly DFE.
- Power is a critical concern for CEI-112G VSR
  - The receiver complexity required for CEI-112G VSR **MUST** be considered when defining the channel specification.
  - ILD and RL critically impact the power of the system.
- BER
  - Relaxing to 2.2E-4 (KP4-FEC used in 100GE) provides up to 2.7dB SNR improvement
  - If used in a module supporting 100GE, relaxing to 2.2E-4 likely requires FEC termination and regeneration on each SERDES interface (must consider power/latency overhead)

Conclusions

- MACOM has demonstrated lab measurements using Narva for:
  - Optical links supporting 100GE single λ
  - VSR Links supporting 53.125GBaud PAM-4

- 112Gbps VSR is a challenging problem with a limited power budget.
- Need to improve ILD, RL and noise characteristics of channels.
- Improved channels will allow vendors to design power-efficient solutions.

Acknowledgements

- Special thanks to: Georgios Takos, Yehuda Azenkot, Saman Behtash, Aravind Ramachandran, Dean Truong, Rohan Gandhi, Chris Collins and Bhaskarareddy Avula.