Comments on PTP Timestamping Clarifications

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Background

- **IEEE P802.3-2015/Cor 1 (IEEE 802.3ce) Multilane Timestamping Task Force**
  - Generated 802.3-2015-Cor1-2017.pdf (March 2017)
    - This document has since been superseded by 802.3-2018
  - Contains updates to Clause 90
    - Clarifying text for the transmit path delay and receive path delay (i.e. SFD at the MDI)
    - New paragraph indicating that for multilane PHYs to use the arrival of the SFD on the lane with the least-skewed buffer
- **IEEE 802.3 Working Group received ITU_SG15-LS-72_to_IEEE_802d3.pdf liaison from ITU-T SG15 (October 2017)**
  - Requesting advice on the sources of timestamping error in PHYs that contain FEC, use codeword markers, and/or use alignment markers
- **IEEE 802.3 Working Group sent IEEE_802d3_to_SG15_timing_0118.pdf liaison to ITU-T SG15 (January 2018)**
  - Indicated that Ethernet FEC streams are bit transparent through the FEC layer such that the delay variation in the Tx path is matched by opposite variation in the Rx path
  - Indicated that some implementation introduce no timestamping accuracy due to markers
- **IEEE P802.3 Revision to IEEE Std 802.3-2015 (IEEE 802.3cj) Maintenance #12 Task Force**
  - Comment #i-52 of P8023-D3p0-Comments-Final-byCls.pdf revised the previous Clause 90 to provide guidance for Tx and Rx path delay measurements in the presence of FEC (January 2018)
    - Report the delays as if the SFD is at the start of the FEC block

Recent Discussions

- **802.3 Maintenance Task Force gorshe_1_0718.pdf sought clarity in PTP timestamping in the presence of alignment markers (July 2018)**
  - Highlighted differences between IEEE 802.3 Clause 90 (i.e. beginning of SFD) and the IEEE 1588-2018 (i.e. beginning of the first symbol after the SFD) message timestamp point
    - Location of alignment markers thus impacts correctness of the timestamp
  - Suggested clarifying text for the timestamp value in the presence of alignment markers and/or rate adaptation (idle insert/delete)
- **802.3 Maintenance Task Force gorshe_1_0119.pdf again sought clarity (January 2019)**
  - Re-iterated the above two points
  - Highlighted a new point about the lane distribution/multiplexing impact on the timestamp
    - Suggested two possible methods of calculating an accurate timestamp

Open Questions

- **Three previous questions from Gorshe, et. al:**
  - Clarify Tx and Rx Path Data Delay
  - Clearly specify how AM and Idle insertion/deletion affect PTP timestamps
  - Clarify how to account for the lane distribution impact on the latency difference between the MII and the PHY of each lane
- **This presentation provides a response to these three questions**

Tx and Rx Path Data Delay

- **Current Standards References**
  - IEEE 1588-2008 reads:
    - 7.3.4.1 Event message timestamp point
      - Unless otherwise specified in a transport-specific annex to this standard, the message timestamp point for an event message shall be the beginning of the first symbol after the Start of Frame (SOF) delimiter.
  - IEEE 802.1AS-2011 reads:
    - 11.3.9 Event message timestamp point
      - The message timestamp point for a PTP event message shall be the beginning of the first symbol following the start of frame delimiter.
  - IEEE 802.3-2018 Clause 90.7 reads:
    - 90.7 Data delay measurement
      - The TimeSync capability requires measurement of data delay in the transmit and receive paths, as shown in Figure 90–3. The transmit path data delay is measured from the beginning of the SFD at the xMII input to the beginning of the SFD at the MDI output. The receive path data delay is measured from the beginning of the SFD at the MDI input to the beginning of the SFD at the xMII output.
- **Agree with gorshe_1_0119.pdf that IEEE 802.3 Clause 90 should use the same timestamp reference point as IEEE 1588-2018 and IEEE 802.1AS-2011**
  - Should use the beginning of the first symbol after the SFD

Proposed Text to Clarify Tx and Rx Path Data Delay (1 of 3)

- **IEEE 802.3-2018 Clause 90.7 current text:**
  - The transmit path data delay is measured from the beginning of the SFD at the xMII input to the beginning of the SFD at the MDI output. The receive path data delay is measured from the beginning of the SFD at the MDI input to the beginning of the SFD at the xMII output.
- **Clause 90.7 proposed text:**
  - The transmit path data delay is measured from the beginning of the first symbol after the SFD at the xMII input to the beginning of the first symbol after the SFD at the MDI output. The receive path data delay is measured from the beginning of the first symbol after the SFD at the MDI input to the beginning of the first symbol after the SFD at the xMII output.

Proposed Text to Clarify Tx and Rx Path Data Delay (2 of 3)

- **IEEE 802.3-2018 Clause 90.7 current text:**
  - For a PHY that includes an FEC function, the transmit and receive path data delays may show significant variation depending upon the position of the SFD within the FEC block. However, since the variation due to this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays be reported as if the SFD is at the start of the FEC block.
- **Clause 90.7 proposed text:**
  - For a PHY that includes an FEC function, the transmit and receive path data delays may show significant variation depending upon the position of the beginning of the first symbol after the SFD within the FEC block. However, since the variation due to this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays be reported as if the beginning of the first symbol after the SFD is at the start of the FEC block.

Proposed Text to Clarify Tx and Rx Path Data Delay (3 of 3)

- **IEEE 802.3-2018 Clause 90.7 current text:**
  - The receiver of a multi-lane PHY is expected to include a buffer to compensate for skew between the lanes. This buffer selectively delays each lane such that the lanes are aligned at the buffer output. The earliest arriving lane experiences the most delay through the buffer and the latest arriving lane experiences the least delay through the buffer. The receive path data delay for a multi-lane PHY is reported as if the beginning of the SFD arrived at the MDI input on the lane with the smallest buffer delay.
- **Clause 90.7 proposed text:**
  - The receiver of a multi-lane PHY is expected to include a buffer to compensate for skew between the lanes. This buffer selectively delays each lane such that the lanes are aligned at the buffer output. The earliest arriving lane experiences the most delay through the buffer and the latest arriving lane experiences the least delay through the buffer. The receive path data delay for a multi-lane PHY is reported as if the beginning of the first symbol after the SFD arrived at the MDI input on the lane with the smallest buffer delay.

AM Insert/Delete and Rate Adaptation

- **According to IEEE 802.3-2018 Clause 90.7, MII is the start point for transmit path data delay and MII is the end point for receive path data delay**
  - Alignment markers may be inserted/removed “beneath” the MII
  - Rate adaptation (i.e. idle insertion/removal) may occur “beneath” the MII
  - Unless taken into consideration, these factors can introduce inaccuracy in the timestamp
- **In gorshe_1_0119.pdf clarifying text was proposed:**
  - “If the insertion or removal of AMs and/or Idles in these PCSs affects the transmit or receive data path delay, this effect must be accounted for in the timestamp. In this way, the timestamp operation is performed as if alignment markers are present at the xMII (i.e., as if AM insertion and Idle insertion/removal is performed ahead of the Tx xMII and AM deletion and Idle insertion/removal is performed after the Rx xMII).”
- **Agree with the above clarifying text and propose similar text on next slide**

Proposed Text to Clarify Effect of AM insert/delete and rate adaptation

- **Clause 90.7 current text:**
  - None
- **Clause 90.7 proposed text to add after existing 90.7 paragraph 2:**
  - For a PHY that inserts alignment markers or performs rate adaptation, the transmit path data delay measurement starting point (the beginning of the first symbol after the SFD at the xMII input) should be adjusted to account for alignment marker insertion or rate adaptation that occurs in the PHY (between the xMII input and the MDI output) which impacts the relative location of the beginning of the first symbol after the SFD. Based on this adjustment, the result is a transmit path data delay measurement that appears as if the alignment marker insertion or rate adaptation had been performed before the Tx xMII. Similarly, the receive path data delay measurement ending point (the beginning of the first symbol after the SFD at the xMII input) should be adjusted to account for any alignment markers or rate adaptation that occurred in the PHY (between the MDI input and xMII output) which impacts the relative location of the beginning of the first symbol after the SFD. Based on this adjustment, the result is a receive path data delay measurement that appears as if the alignment marker insertion or rate adaptation had been performed after the xMII.

Impact of Lane Distribution

- **On transmit the distribution of data to multiple lanes results in delay variation as symbols/blocks are intended to leave the transmitter logically aligned**
  - And thus, early-arriving symbols/blocks experience greater delay than late-arriving blocks, until each lane is filled with a symbol/block
- **On receive, the multiplexing of the data from multiple lanes back into a single stream result in similar delay variation**
- **In gorshe_1_0119.pdf two methods were proposed:**
  - Method1) Take the distribution and multiplexing into account
  - Method2) Ignore the impact of distribution and multiplexing since they cancel each other out
- **Agree with Method 2 of above and propose text on next slide**
  - In applications where PHY and 1588 Timestamping Logic are separated, Method 2 allows identical timestamping with different PHYs

Proposed Text to Clarify Impact of Lane Distribution

- **Clause 90.7 current text:**
  - None
- **Clause 90.7 proposed text to add after 90.7 paragraph 3:**
  - For a multi-lane PHY the transmit and receive path data delays may show some variation depending upon the lane which contains the beginning of the first symbol after the SFD. However, since the variation due to this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays exclude consideration of this effect.

Summary

- **Discussed three previous questions from Gorshe, et. al:**
  - Clarify Tx and Rx Path Data Delay
  - Clearly specify how AM and Idle insertion/deletion affect PTP timestamps
  - Clarify how to account for the lane distribution impact on the latency difference between the MII and the PHY of each lane
- **Provided a response to these three questions**
- **Proposed text to amend 802.3-2018**

Thank You!