Thoughts on electrical interfaces beyond 100 Gb/s

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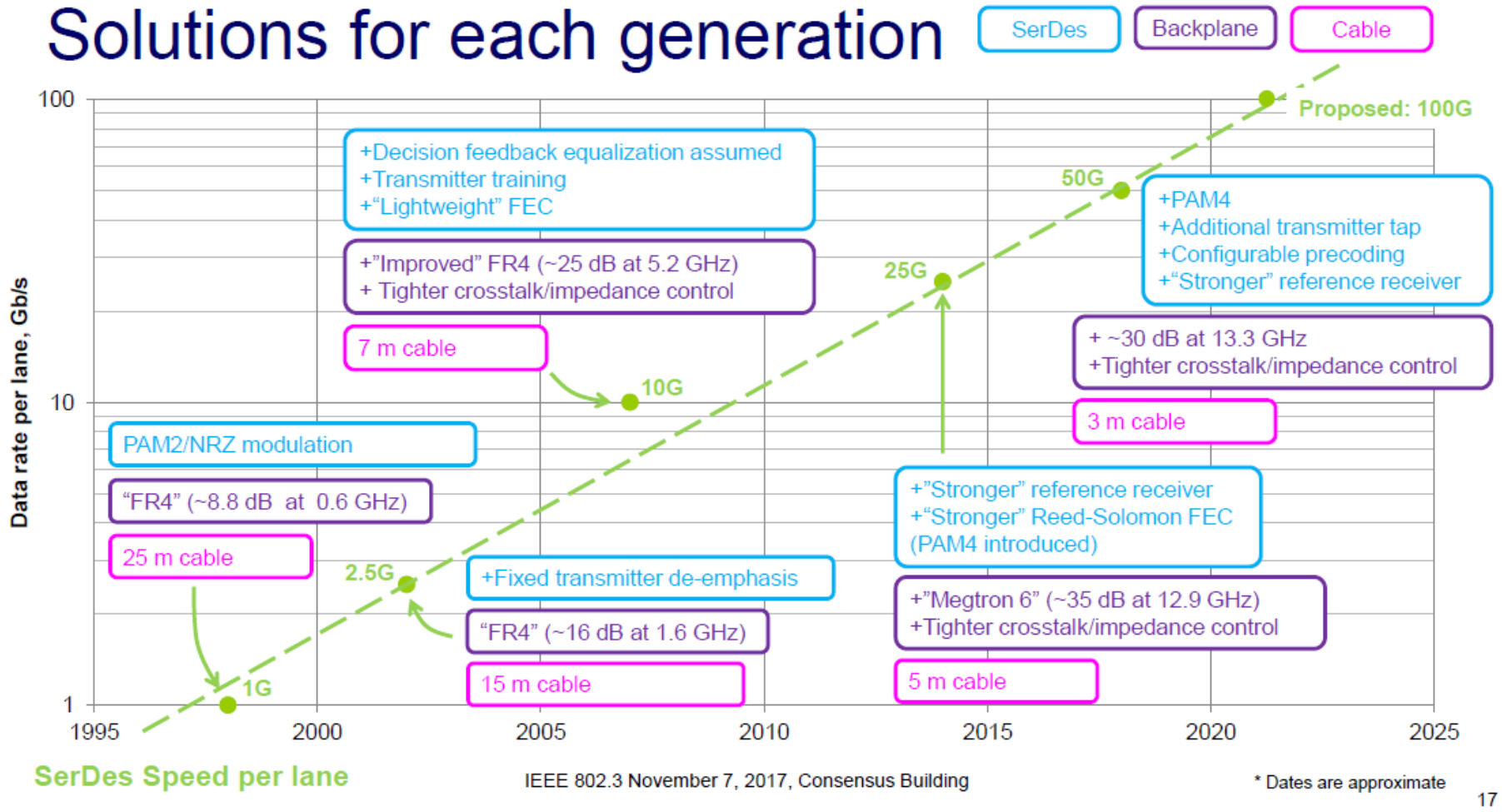
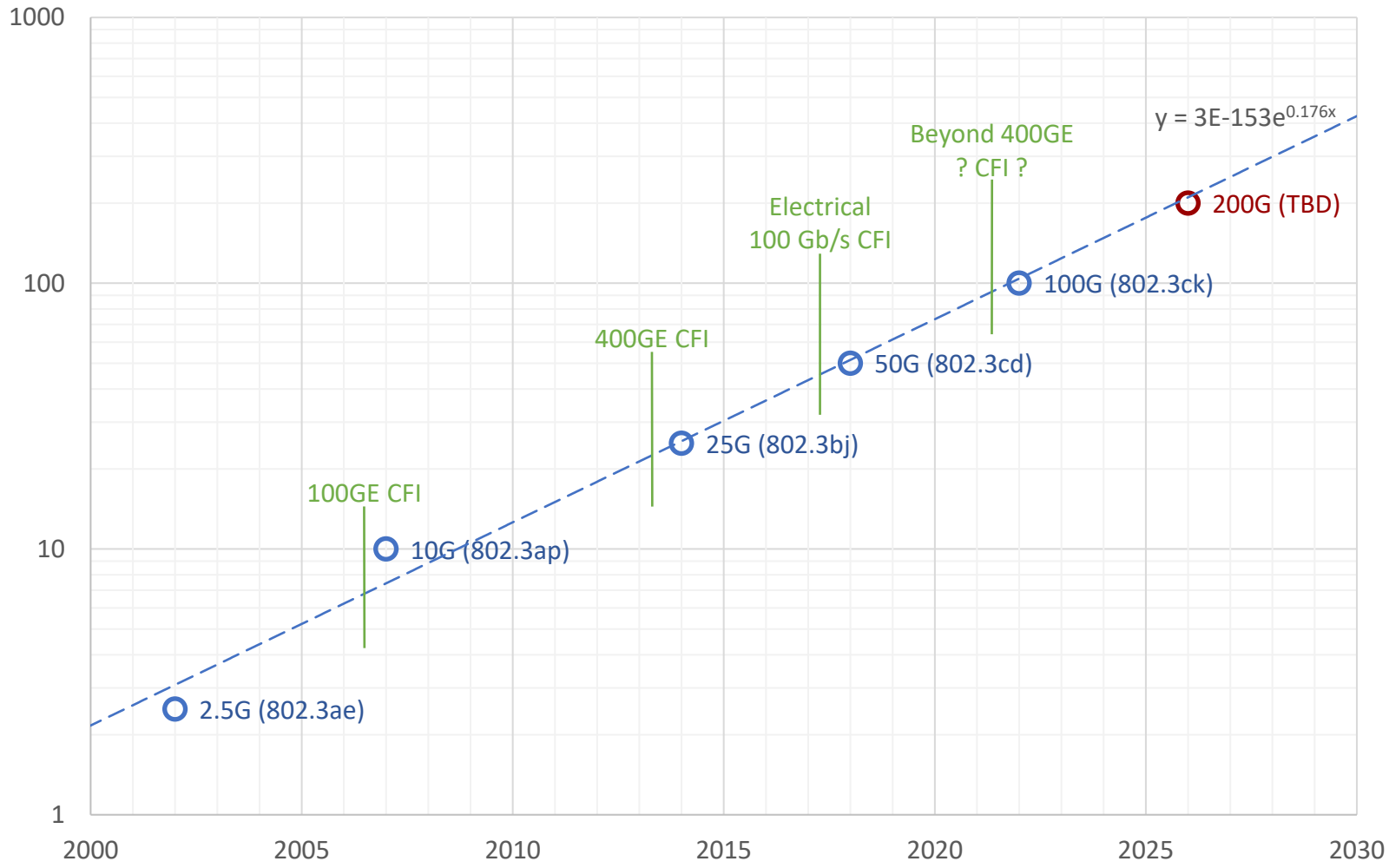
Introduction

- For any high-volume package, connector, and medium there are a limited number of physical “wires” available.
- For the next Ethernet rate, data rate per electrical lane must increase.
- Consider historical trend of data rate per electrical lane.
- Consider potential paths to higher data rate per electrical lane.
- Looking only at longer reach interconnect such as copper cable and backplane.
  - Will consider chip-to-chip and chip-to-module later.
- Not proposing any specific solutions.

802.3ck CFI slide 17



Electrical lane rate history, timeline



Assuming we have a successful CFI in March 2021 and the resulting project completes in 4 years, 200 Gb/s electrical interfaces will be on track with the historical trend.

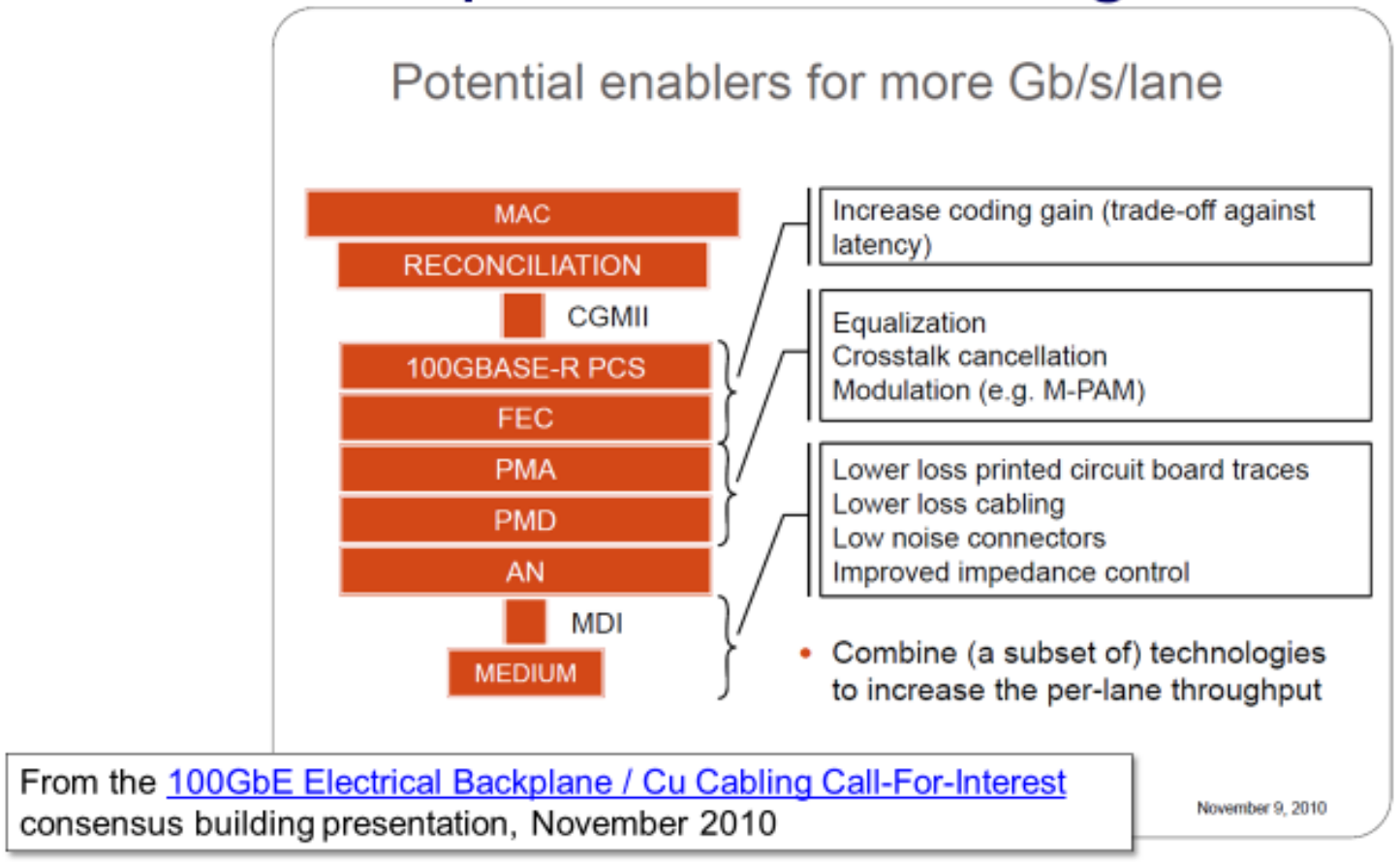
Trendline indicates doubling of lane rate every 3.9 years.

Electrical lane rate history, solutions

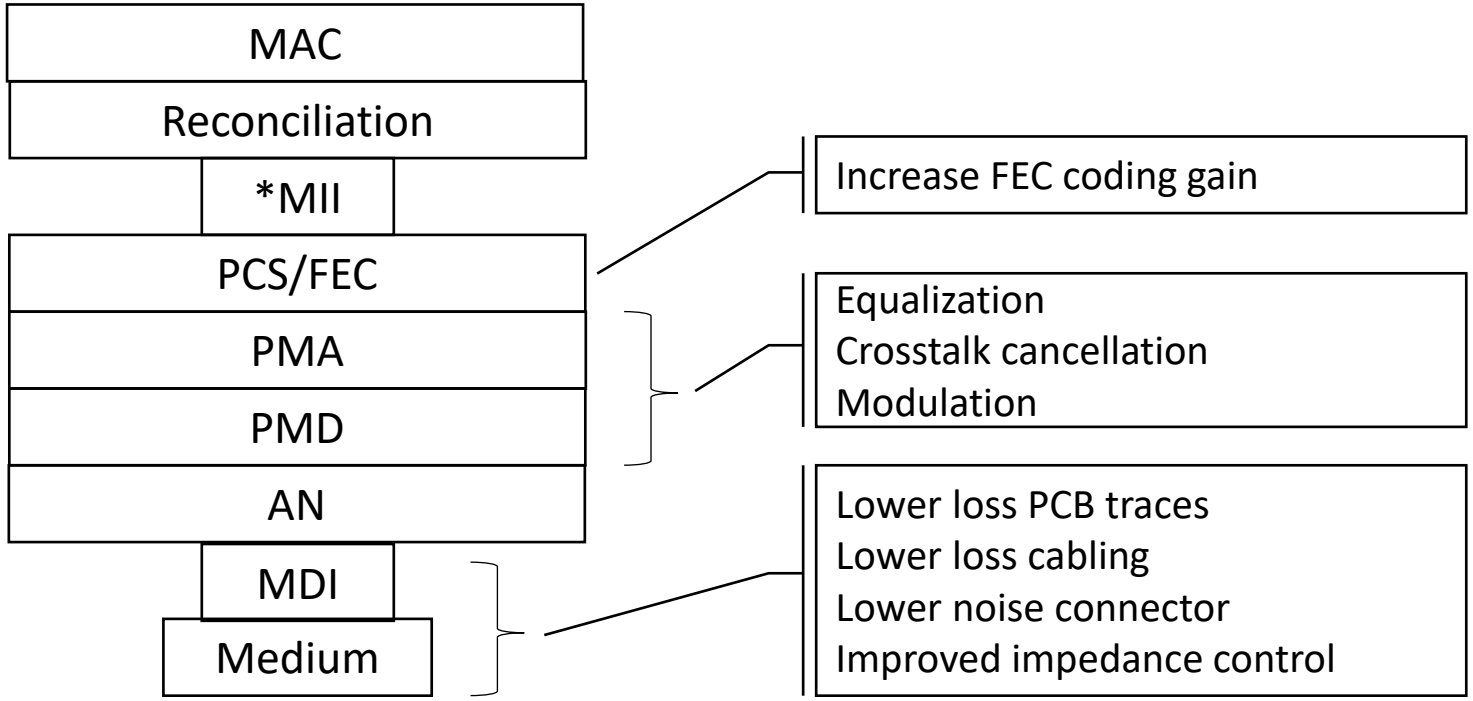
Lane rate (Gb/s)	Year	SERDES	Backplane	Cable
1	1998	PAM2/NRZ modulation	FR4 PCB (~8.8 dB @ 0.6 GHz)	25 m cable
2.5	2002	Fixed TX de-emphasis	FR4 PCB (~16 dB at 1.6 GHz)	15 m cable
10	2007	RX DFE assumed TX equalization training Light-weight FEC	“Improved” FR4 (~25 dB at 5.2 GHz) Tighter crosstalk/impedance control	7 m cable
25	2014	Stronger reference receiver Stronger FEC (Reed-Solomon) PAM4 introduced	Megtron 6 (~35 dB at 12.9 GHz) Tighter crosstalk/impedance control	5 m cable
50	2018	PAM4 universal Additional transmitter tap Configurable precoding Stronger reference receiver	~30 dB at 13.3 GHz Tighter crosstalk/impedance control	3 m cable
100	2021?	Additional transmitter tap Stronger reference receiver	~28.5 dB @ 26.6 GHz Tighter crosstalk/impedance control	2 m cable
200	2026?	?	?	?

802.3ck CFI slide 16

It's time to open the toolbox again…



Tool box for higher data rate per lane



Avenues to higher data rate per lane

- Higher order modulation
  - e.g., PAM16, QAM16
- Increase # of electrical lanes per physical lane (wire/trace)
  - e.g., bidirectional
- No package
  - e.g., die on substrate, OIF XSR
- Not quite double the bit rate per lane
  - e.g., 5 * 160 Gb/s, 6 * 133 Gb/s
- Stronger FEC
- Lower loss interconnect

Conclusion

- The timing is right to start thinking about the next lane rate.
- There are paths to achieving higher lane rates.

Thanks