

IEEE 802.3 Ethernet Working Group
DRAFT Liaison Communication

Source: IEEE 802.3 Working Group¹

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Subject: Liaison reply to Impact on timing performance due to Ethernet PHY – October 2017 communication

Approval: **To be approved** at IEEE 802.3 Interim meeting, Geneva, Switzerland, 25th January 2018

Dear Mr. Ruffini,

Thank you for your liaison letter concerning the impact on timing performance due to Ethernet PHY.

We recognize the importance of controlling delay asymmetry and variability for time synchronization. To that end, Clause 90 of IEEE Std 802.3-2015 deals with methods for reporting the minimum and maximum values of transmitter and receiver path data delays separately.

Following your liaison letter, an ad hoc was formed to address the concerns that were raised and recommend further action. The outcome of this activity is reported below.

1. As noted in your letter, FEC encoding includes periodic insertion of parity blocks, which creates variability in the delay of frames in the transmitter and in the receiver. This is characteristic of multiple FEC schemes specified in IEEE Std 802.3-2015 and

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its amendments, including Clause 108. For the RS(528,514) used in Clause 108, the delay variability is up to 5.43 ns in both transmitter and receiver. However, in all FEC schemes, the total delay through the FEC encode and decode functions is constant, so time synchronization accuracy should not be affected. This fact is not currently addressed by Clause 90.

To address the variability in path data delay due to the FEC function, a comment has been submitted to the IEEE P802.3 (IEEE 802.3cj) Revision task force, suggesting a recommendation of a specific path data delay reporting method that would eliminate this source of variability. Please note that at the IEEE P802.3 (IEEE 802.3cj) Revision is currently in Sponsor Ballot and comments may or may not be accepted.

2. Another possible source of delay variability is the periodic insertion and deletion of markers by the PCS/FEC (e.g., codeword markers in Clause 108, or alignment markers in Clause 82). This functionality may introduce delay variability of up to 12.8 ns for the 100GBASE-R PCS, in both transmitter and receiver. However, we would like to note that there are compliant implementation methods that create no timestamping inaccuracy due to markers.
3. Your letter also listed rate adaptation as a possible concern. Note that rate adaptation is specified as a function of the Reconciliation Sublayer (RS), and implementation within the RS does not affect timing at the xMII reference point. While some PCS specifications include optional capability of rate adaptation, implementations are possible without this capability, if minimizing delay variability is a goal.
4. The reference points of path data delay reporting are specified in Clause 90 as the xMII and the MDI. This enables assessment of the delays from MDI to MDI even with asymmetry in PHY delays. Since the xMII is the only reference point that is defined for all PHYs, it is the only point that enables a generic definition of delays. As noted above, accurate timing is achievable in practice, even with the marker insertion functionality, and with the proposed specification of path data delay reporting with FEC. Therefore, changing the reference point for path data delay reporting is not considered necessary.

We would like to note that the Ethernet standard does not enforce limits on delay variations in Ethernet PHYs, nor does it dictate specific implementation methods. We would also note that it may not be possible to eliminate all timing errors when certain optional internal interfaces are physically instantiated (e.g., XGXS/XAUI or 25GAUI). Products may or may not be optimized for minimum delay variation.

In summary, the action following your letter is a proposed recommendation for specific path data delay reporting that would eliminate variability due to FEC encoding and decoding, which will be processed in the IEEE P802.3 (IEEE 802.3cj) revision project. We would like to thank you for bringing forward your concerns. We look forward to continuing our cooperation with ITU-T SG15.

Sincerely,

David Law

Chair, IEEE 802.3 Ethernet Working Group