

## IEEE P802.3 Timing Performance Ad Hoc meeting – November 29, 2017

Prepared by Kent Lusted

### Proposed Agenda:

- Approval of the Agenda
- IEEE patent policy reminder:
  - <http://www.ieee802.org/3/patent.html>
- IEEE Participation Requirements reminder
- Ad Hoc Topics –
  - Approval of the November 15<sup>th</sup> [minutes](#)
  - Next ad hoc teleconference announcement
  - Ethernet Time Synchronization accuracy – ad hoc report (Adee Ran, Intel)

Presentations posted at: [http://www.ieee802.org/3/ad\\_hoc/timing\\_perf/index.html](http://www.ieee802.org/3/ad_hoc/timing_perf/index.html)

Meeting began at ~12:05 p.m. Pacific by Adee Ran.

Adee Ran appointed Kent Lusted as the recording secretary for the call.

Meeting began with the agenda presentation:

[http://www.ieee802.org/3/ad\\_hoc/timing\\_perf/agenda\\_tp\\_2017\\_11\\_29.pdf](http://www.ieee802.org/3/ad_hoc/timing_perf/agenda_tp_2017_11_29.pdf)

The ad hoc chair reminded participants to indicate full names and employer/affiliation correctly for the meeting minutes. He reminded participants to mute lines when not speaking and reviewed the steps to unmute.

Showed the links to the ad hoc page and the email reflector.

Reminded participants of the IEEE Participation Requirements and showed the slide with the Participation requirements. He asked if anyone was unfamiliar with the IEEE Participation Requirements. No one responded.

Presented the proposed agenda and asked if there was objection as written. The agenda was approved by the ad hoc.

Reminded participants of the IEEE patent policy. He asked if anyone was unfamiliar with the IEEE patent policy. No one responded.

Asked if there were comments regarding the posted minutes of the last ad hoc meeting. No one responded.

## Agenda Items

Adee announced the next ad hoc teleconference meeting as December 13, 2017. It will be announced over the DIALOG reflector.

Adee Ran asked Kent Lusted to moderate the discussion during his presentation.

### Presentation #1:

“Ethernet Timing performance ad hoc report”, Adee Ran

See: [http://www.ieee802.org/3/ad\\_hoc/timing\\_perf/ran\\_tp\\_01\\_2017\\_11\\_29.pdf](http://www.ieee802.org/3/ad_hoc/timing_perf/ran_tp_01_2017_11_29.pdf)

- On slide 3, false accuracy is meant to be the difference between the min and the max delay in the Clause 90 registers due to FEC encoding and decoding (since the sum of the delays of encoding on one end and decoding on the other end is constant).
- Adee asked if there were any other sources that should be listed. No other sources were added after discussion.
- Regarding implementation-dependent methods, the Standard defines externally visible behavior, not the way to implement it.
- There was a request to rephrase the sub-bullet of the first major bullet on slide 5. It was recommended to avoid referencing the implementation.
- Discussed the proposed changes to Clause 90 shown on slide 7. It was noted that the variability in the TX is nearly always compensated by the RX. A common location, such as a specific SFD in a FEC block, in the TX and RX should be specified. There was a recommendation to move the text location to the register section as a summary statement. There should be no variation in the delay register due to the position of the frame in the FEC block; it may come from other sources. The added text should be a recommendation, not a requirement, in order to exempt existing implementations.
- It was noted that PON could use the same delay measurement as proposed. EPOC should be checked. It was recommended to add an exclusion for PHY types that are no longer available.
- Discussed different phrasing for the proposed text on slide 8. It will be considered offline. Use caution with the item related to the comment; it is not implied that the comment's remedy will be adopted.

David Law thanked Adee for his work on this topic.

The ad hoc meeting ended at ~1 p.m. Pacific.

## List of attendees (captured from Webex tool)

	Name	Affiliation
1	Adee Ran	Intel
2	Steve Trowbridge	Nokia
3	stefano ruffini	Ericsson
4	Kent Lusted	Intel
5	Silvana Rodrigues	IDT
6	Steve Carlson	High Speed Design
7	Amit Oren	Broadcom
8	Mark Gustlin	Xilinx
9	Omer Sella	University of Cambridge
10	George Zimmerman	Analog Devices, APL Group, Aquantia, BMW, Cisco Systems, Commscope
11	David Chalupsky	Intel
12	Peter Anslow	Ciena
13	Marek Hajduczenia	Charter
14	David Law	HPE
15	Kamatchi	Juniper
16	Bill Powell	Nokia
17	Phil Sun	Credo
18	Rodney Cummings	NI