IEEE P802.3 Timing Performance Ad Hoc meeting – December 13, 2017

Prepared by Kent Lusted

Proposed Agenda:

- Approval of the Agenda
- Ad Hoc Topics –
  - Approval of the November 29th minutes
  - Comment for submission to 802.3cj (Adee Ran, Intel)
  - Proposed draft liaison response (Adee Ran, Intel)

Presentations posted at: http://www.ieee802.org/3/ad_hoc/timing_perf/index.html

Meeting began at ~12:05 p.m. Pacific by Adee Ran.

Adee Ran appointed Kent Lusted as the recording secretary for the call.

Meeting began with the agenda presentation:

http://www.ieee802.org/3/ad_hoc/timing_perf/agenda_tp_2017_12_13.pdf

The ad hoc chair reminded participants to indicate full names and employer/affiliation correctly for the meeting minutes. He reminded participants to mute lines when not speaking and reviewed the steps to unmute.

Showed the links to the ad hoc page and the email reflector.

Reminded participants of the IEEE Participation Requirements and showed the slide with the Participation requirements. He asked if anyone was unfamiliar with the IEEE Participation Requirements. No one responded.

Presented the proposed agenda and asked if there was objection as written. The agenda was approved by the ad hoc.

Reminded participants of the IEEE patent policy. He asked if anyone was unfamiliar with the IEEE patent policy. No one responded.

Asked if there were comments regarding the posted minutes of the last ad hoc meeting. No one responded.

Agenda Items

Presentation #1:
"Proposed comment for P802.3cj", Adee Ran
See: http://www.ieee802.org/3/ad_hoc/timing_perf/ran_tp_01a_2017_12_13.pdf

- Reviewed proposed text. Minor changes were made to the text.
- Reviewed the change with the context (slide 6). The comment has already been submitted at the time of review.
- An observation was made on the proposed Note 3: a PHY built out of components and has a FEC delay in the PCS and the PMD, may have more than 2 parties involved. Consider the implication of "not in both" in which more than 2 parties are involved.
- A real measurement on silicon is not expected to be made. However, it is expected that a design would be analyzed to determine what value should be placed into the delay register, assuming the SFD was at the start of the FEC block.
- The multi-lane case accounts for the deskew buffer delay in the data.
- A change was made to the first paragraphs proposed text on slide 6.
- Changed the proposed text in Note 3 on slide 6. "For PHYs that are specified with a FEC sublayer separate from the PCS…." Discussed the impact of FEC bypass or no FEC case and determine no further change to the text is required.

Adee Ran reviewed the proposed liaison communication text in IEEE_802p3_ITU-T_SG15_0118_DRAFT.doc. Changes were made and saved as IEEE_802p3_to_ITU-T_SG15_0118_DRAFT_2017_12_13.doc.

- Discussed different ways to create compliant implementations referenced in list item #2.
- Discussed rate adaption as it related to list item #3.
- It was noted that a 25G PCS is connected to a 25G FEC via a 25GAUI interface, there is no viable solution for eliminating frame jitter. There may be specific optional physical implementations of internal interfaces that may prevent accurate time error reporting.

The ad hoc meeting ended at ~1:15 p.m. Pacific.

List of attendees (captured from Webex tool)

	Name	Affiliation
1.	Adee Ran	Intel
2.	Yong Kim	Broadcom
3.	Adrian Butter	Global Foundries
4.	David Law	HPE
5.	Duane Remein	Huawei
6.	Kapil Shrikhande	Innovium
7.	Steve Trowbridge	Nokia
8.	Kent Lusted	Intel
9.	George Zimmerman	Analog Devices, APL Group, Aquantia, BMW, Cisco Systems, Commscope