*Cl* **00**     *SC* **Table 51-12**          *P* **444**          *L* **6**          # **99200**

Geoffrey Garner                    Lucent Technologies

*Comment Type* **TR**     *Comment Status* **R**                    *D4.2 #96*

Comments #99046 and #99048 of D4.1 (formerly comments #11 and #12, respectively, of D4.0) state that the +/- 100 ppm clock tolerance currently specified for the 10GBASE-LW and 10GBASE-EW receivers (in Tables 52-14 and 52-18, respectively) is more than is required in relation to the transmitter specification and any possible transport network such as SDH/SONET, OTN, and also old legacy 10 G WDM transponder equipment. Both comments indicate that, as such, the specification is internally inconsistent and also inconsistent with respect to transport equipment.  There is no reason to require the receiver to have a tolerance of +/- 100 ppm because no received signal will ever have a frequency offset greater than +/- 20 ppm.  The comments state that the receiver specification should be changed to what is required in line with the transmitter and transport network specification.

The response to these comments was REJECT, with a reference to the comment #93 response; this response simply indicated that this is consistent with clauses 46-51, and would be a flip-flop after much discussion to set the receiver tolerance to +/- 100 ppm.

This response does not address the technical issue raised in the comments.  The fact is that the +/- 100 ppm receiver tolerance is much more stringent than is needed for the +/- 20 ppm transmit tolerance spec.

The suggested remedy in both comments #99046 and #99048, to change the required receiver tolerance to +/- 20 ppm, would result in a less costly receiver design that would work with the transmitter specification.  The design would be less costly because the receiver clock tolerance is essentially a spec on the receiver phase-locked loop pull-in range; making the pull-in range unnecessarily large results in the design being more costly than it needs to be.

This issue was discussed in the March 26, 2002 serial PMD call.  The commenter raised the issue there because the comments were against clause 52, and they were against clause 52 because the relevant tables that contain the receiver clock tolerance (Tables 52-14 and 52-18) are in clause 52.  Nonetheless, the members of the serial PMD group on the call said that the optics group does not really have the expertise or the strong opinions on this matter, and this would be better raised as a comment against "clause 00" for discussion in the larger group. Therefore, the present comment is against "clause 00".

It also was stated in the March 26, 2002 seial PMD call that changing the receiver clock tolerance to +/- 20 ppm would also require changes to clause 51. Examination of clause 51 does indicate that receiver clock tolerance is also given in Table 51-12.  The present comment indicates that the entry for 10GBASE-W in Table 51-12 on Line 6, p. 444, should be changed from 622.08 MHz+/-100ppm to 622.08 MHz+/-20ppm.

This is in addition to the changes to Clause 52, Tables 52-14 and 52-18 already indicated in Comments #99046 and #99048.  Finally, note that the original comment that gave rise to the change to the WAN PHY transmit clock tolerance, comment #661 of D3.0, indicated that the 622.08 MHz+/-100ppm in what was then Table 51.6 of D3.0 should be changed to 622.08 MHz+/-20ppm, and that analogous changes should be made to Tables 52-7, 52-9, 52-12, 52-14, 52-17, and 52-18.  The clause 52 tables include the transmit and receive specs.  The clause 51 table pertains only to the transmit spec; however, D3.0 did not have a clause analogous to Clause 51.7.2 in D4.2, nor a Table analogous to Table 51-12 in D4.2.  The statements in Comment #661 of D3.0 at least indicate that the intent of this comment was to change both the 10GBASE-W transmitter and receiver clock tolerances from +/-100ppm to +/-20ppm.  The response to this comment indicates ACCEPT, with the comment re-issued as #44000 and 44001 to permit clause 51 and 52 editors to track closure of the comment.

*SuggestedRemedy*

Make the changes to Tables 52-14 and 52-18 already indicated in Comments #99046 and #99048, to change the 10GBASE-LW and EW receiver specs to +/-20ppm.  Change 622.08 MHz+/-100ppm to 622.08 MHz+/-20ppm in Table 51-12.

*Response*                    *Response Status* **U**

REJECT.

This comment has been ruled as not a new comment.  This comment was submitted against Clause 52 in D4.0 by the commenter, and the comment was rejected.  The comment was recirculated and the draft has remained approved through the D4.1 and D4.2 recirculations.

Input from other PLL designers is that +/- 100 ppm doesn't impact the cost of the PLL design.  The assumption that +/- 20 ppm would always occur at the receiver is invalid. One possible application for increased receive clock tolerance is the mapping and demapping of 10GBASE-W into a SONET/SDH payload.

Historically, Ethernet has been liberal on what they receive and conservative on what they transmit.  The support for the current tolerances is indicative of support for this philosophy.

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*Cl* **47**     *SC* **3.4.5**          *P* **292**          *L* **40**          # **99017**

Gaither, Justin                    Xilinx

*Comment Type* **TR**     *Comment Status* **R**                    *D4.0 #4*

Input impedance should be specified the same as the output impedance.

*SuggestedRemedy*

Change text similar to the way output impedance is specified.

*Response*                    *Response Status* **U**

REJECT.

Input impedance spec is not considered to be a problem according to test data (working receivers were tested and met spec) supplied that did indicate a valid spec problem with output impedance. Recevier test data indicates that a flat 10 dB input return loss was achievable.

The impact of loosening transmitter return loss as agreed to for D4.0 comment resolutions results in an increase in return loss contribution to deterministic jitter from 0.03 UI to 0.049 UI. The additional impact of loosening receiver return loss as requested by this comment would result in a return loss contribution of 0.072 UI of deterministic jitter. This amount of additional jitter is excessive (blows the jitter budget) in light of the absence of proof of an existing problem with the current input impedance spec.

If evidence is received indicating that the current receiver return loss spec is not acheivable, then other driver and/or receiver parameters must be adjusted in order to maintain a working jitter budget.

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TYPE: TR/technical required  T/technical  E/editorial    COMMENT STATUS: D/dispatched  A/accepted  R/rejected    SORT ORDER:  Clause, Page, Line, Subclause

RESPONSE STATUS: O/open  W/written  C/closed  U/unsatisfied  Z/withdrawn

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*Cl* **47**     *SC* **3.4.5**

*Cl* **51**       *SC* **4**                    *P* **427**           *L*              **#** **99019**

Gaither, Justin                                    Xilinx

*Comment Type*   **TR**       *Comment Status*   **R**                          *D4.0 #3*

As stated in the Note on page 421. XSBI is based on the OIF SFI-4 specification. The OIF specification includes the optional use of a Dual Data Rate clock which the XSBI implementation is missing.

An optional Dual Data Rate clock should be included in the standard as part of the XSBI interface for the following reasons:
1. Maintain continuity between OIF interface and XSBI
2. Broad market availability of LVDS IO at <400 Mhz (FPGA & ASIC)
3. >600 Mhz LVDS IO requires higher cost. (ASIC only, higher license fee)
4. lower EMI radiation.

*SuggestedRemedy*

The following changes will be required:
1. pg. 422 Table 51-1: add "SDR Mode defined as Single data rate clock mode of operation in which data is latched on the rising edge of the clock signal"
2. pg 422 Table 51-1: add "DDR Mode defined as Optional Dual Data Rate clock operation in which data is latched on both the rising and falling edge of the clock signal."
3. pg. 423 line 4: add text to read "...edge of the PMA_TX_CLK for SDR mode or the corresponding edge for DDR mode."
4. pg. 423 line 10 and 11.  removed ", PMA_RX_CLK, which is at 1/16 the bit rate,"
5. pg 423 Table 51-4: Change active level for PMA_TX_CLK and PMA_RX_CLK to indicate rising edge for SDR Mode and both edges for DDR Mode.
6. pg 424 line 45: add text to read "rising edge of PMA_TX_CLK is used to latch data into the PMA in SDR mode and both edges of PMA_TX_CLK are used to latch data into the the PMA in DDR mode."
7. pg 425 line 11: add text to read "presented to the PMA client on the rising edge of PMA _RX_CLK in SDR Mode or both edges of PMA_RX_CLK in DDR Mode.
8. pg 427 line 10: add text to read "positioning clocks relative to the data in SDR mode."
9. pg 427 line 16: Change title of 51.6.1 to read "XSBI transmit interface timing for SDR mode" Similarly add for SDR mode to subclause titles as needed.
10. Insert new subclause 51.6.2 containing content similar to 51.6.1 except referenced to DDR mode. (I will gladly create the figures and text). specifications should be similar to OIF standard.
11. pg 429 line 50: add text to read "positioning clocks relative to the data in SDR mode"
12. pg 430 line 1: Change the title of 51.7.1 to read "XSBI receive interface timing for SDR Mode" Similarly add for SDR mode to subclause titles as needed.
13. Insert new subclause 51.7.2 containing content similar to 51.7.1 except referenced to DDR mode. (I will gladly create the figures and text). specifications should be similar to OIF standard.
14. pg 429 Table 51-8: existing spec should be specified for SDR mode.  Add another row specifing DDR mode frequency.
15. pg 432 Table 51-12: existing spec should be specified for SDR mode.  Add another row specifing DDR mode frequency.

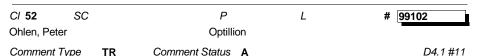*Response*                   *Response Status*   **U**

REJECT.

The DDR option was discussed extensively but voted out over one year ago in working group.

This feature last appeared in draft 1.1(Oct 2000). Since draft 2.0 (Dec 2000) this option is no longer in XSBI. There was consensus in the working group that there was no extensive usage of this mode in the industry.

[Note: Prior vote to remove the 3xx MHz mode.
"Move to accept resolution.
Vote: For: 12 Against: 2 Abstain: 6 (motion carries)"]

The XSBI is an optional interface.  If the working group accepted the commenter's suggested remedy, there would be two non-interoperable version of the XSBI.  The commenter is free to implement a proprietary interface if desired.

Including different options for the same interface is highly deprecated as it tends to split the market and create interoperability problems between components.

*Cl* **52**     *SC*       *P*      *L*      **#** **99102**

Ohlen, Peter        Optillion

*Comment Type*  **TR**     *Comment Status*  **A**        *D4.1 #11*

The receiver sensitivity is currently specified using the stressed sensitivity, measured with a conditioned input signal to which both jitter and ISI has been added. Although the method has been simplified, it still has a limited track record. There are a few parameters which can put you in different corners of a multi-dimensional "stress space". Different receivers designs have different strong and weak points, and depending on which corner you choose, you punish or favor different devices. For some, the nominal sensitivity is more critical, for others, SJ stress is most difficult. For yet another rx, DCD is more difficult.What do we really want to to? We want to find a set of parameters for the stressed eye such that the subsets (1)[passes_test & not_working] and (2)[fails_test & works] are both minimized. This calls for extensive testing and development of test procedures.At the time we want to make products that we can sell to the market-place without revising the spec numbers every other month.These two things don't go along very well, and we might need to give up one of the two options.

*SuggestedRemedy*

Settle on something that we think works today, with numbers that can easily be validated. Do one or several of the following:

1. Make the currently informative receiver sensitivity normative. This measurement is easier to calibrate but does not test jitter.

Separate the jitter and the ISI in the RX stress tests:

2. Remove the jitter from the stressed eye, only use a low-pass filter. Thi s would guard against low-bandwidth signals caused by TX and/or fiber impairments.

3. Introduce a SONET-style jitter tolerance test to ensure that the receiver can cope with a jittered input signal.

Other things we could do:

4. Keep the stressed eye, but follow the precedent of 1GbE and take out the margin for the stressed sensitivity because of the large uncertainty in how the actual penalty and stress (VECP measured on the oscilloscope) correlate.

5. Recognize that we have gathered enough measurement data to say that the stressed eye methodology is well understood and the we have confidence in the chosen numbers and know their significance to ""mission mode"" performance.

*Response*        *Response Status*  **U**

ACCEPT IN PRINCIPLE.

Specifications were refined and reflected in D4.2 & D4.3.

The stressed eye test procedures have been modified and we are now in a position where we believe the following:
- subset 1 (passes test and not working) has been minimized
- subset 2 (fails test and works) has been reduced

by the changes in the specification within D4.2 & D4.3 described below.

We limited the amount of sinsoidal amplitude interferer, thereby narrowing the 3D stress space. We introduced histogram definitions of VECP and jitter to make the calibration more accurate. We strengthened the spec to describe a low noise stressed eye generator. We tightened the TDP spec and added .05 UI offset to ensure that receivers that pass the stressed eye test would interoperate with the specified transmitters. By applying a variable amount of sinusoidal jitter, we now achieve the correct total jitter.

Measurements have been made which support the current specification. The committee believes the current specifications will produce interoperability with conformant products.

11:0:1

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*Cl* **52**     *SC* **52.6.2**       *P* **450**      *L* **14**      **#** **99033**

Juergen Rahn        Lucent Technologies

*Comment Type*  **TR**     *Comment Status*  **R**        *D4.0 #93 clock tolerance*

For the 10GBASE-LW receive optical specifications a clock tolerance of +/-100ppm is specified in table 52-14. This is more than is required in relation to the transmitter specification and any possible transport network such as SDH/SONET, OTN, and also old legacy 10 G WDM transponder equipment. As such, the specification is internally inconsistent and also inconsistent with respect to transport equipment. There is no reason to require the receiver to have a tolerance of +/- 100 ppm because no received signal will ever have a frequency offset greater than +/- 20 ppm. The receiver specification should be changed to what is required in line with the transmitter and transport network specification.

*SuggestedRemedy*

Add an extra column for 10GBASE-LW in table 52-14 with 9.95328 GBd as rate and +/-20ppm as clock tolerance in the same way as it is in Table 52-12.
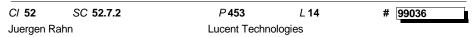
*Response*        *Response Status*  **U**

REJECT. This is consistent with Clauses 46-51. This would be a flip-flop of a previous decision after much discussion to set the receiver frequency tolerance to +/- 100 ppm (the suggested change was rejected once)

6:1:3

See response to comment 96 of D4.2 (or #99200) for an updated explanation.

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TYPE: TR/technical required  T/technical  E/editorial    COMMENT STATUS: D/dispatched  A/accepted  R/rejected    SORT ORDER:  Clause, Page, Line, Subclause     Page 3 of 5

RESPONSE STATUS: O/open   W/written  C/closed   U/unsatisfied  Z/withdrawn         *Cl* **52**     *SC* **52.6.2**

*Cl* **52**    *SC* **52.7.2**    *P* **453**    *L* **14**    **#** **99036**

Juergen Rahn    Lucent Technologies

*Comment Type* **TR**    *Comment Status* **R**    *D4.0 #92 clock tolerance*

For the 10GBASE-EW receive optical specifications a clock tolerance of +/-100ppm is specified in table 52-18. This is more than is required in relation to the transmitter specification and any possible transport network such as SDH/SONET, OTN, and also old legacy 10 G WDM transponder equipment. As such, the specification is internally inconsistent and also inconsistent with respect to transport equipment. There is no reason to require the receiver to have a tolerance of +/- 100 ppm because no received signal will ever have a frequency offset greater than +/- 20 ppm. Thereceiver specification should be changed to what is required in line with the transmitter and transport network specification.

*SuggestedRemedy*

Add an extra column for 10GBASE-LW in table 52-18 with 9.95328 GBd as rate and +/-20ppm as clock tolerance in the same way as it is in Table 52-17.

*Response*    *Response Status* **U**

REJECT.

See response to comment 96 of D4.2 (or #99200) for an updated explanation.

*Cl* **52**    *SC* **6.2**    *P* **450**    *L* **14**    **#** **99045**

Rick Townsend    Lucent Technologies

*Comment Type* **TR**    *Comment Status* **R**    *D4.0 #35 clock tolerance*

For the 10GBASE-LW receive optical specifications a clock toleranceof +/-100ppm is specified in table 52-14. This is more than is required inrelation to the transmitter specification and any possible transport network suchas SDH/SONET, OTN, and also old legacy 10 G WDM transponder equipment. As such,the specification is internally inconsistent and also inconsistent with respect totransport equipment. There is no reason to require the receiver to have a tolerance of+/- 100 ppm because no received signal will ever have a frequency offset greater than+/- 20 ppm. Thereceiver specification should be changed to what is required in line with thetransmitter and transport network specification.

*SuggestedRemedy*

Add an extra column for 10GBASE-LW with 139.95328 GBd as rate and +/-20ppm as clock tolerance in the same way as it isin Table 52-12.

*Response*    *Response Status* **U**

REJECT.

See response to comment 96 of D4.2 (or #99200) for an updated explanation.

*Cl* **52**    *SC* **6.2**    *P* **450**    *L* **14**    **#** **99046**

Geoffrey Garner    Lucent Technologies

*Comment Type* **TR**    *Comment Status* **R**    *D4.0 #11 clock tolerance*

For the 10GBASE-LW receive optical specifications a clock toleranceof +/-100ppm is specified in table 52-14. This is more than is required inrelation to the transmitter specification and any possible transport network suchas SDH/SONET, OTN, and also old legacy 10 G WDM transponder equipment. As such,the specification is internally inconsistent and also inconsistent with respect totransport equipment. There is no reason to require the receiver to have a tolerance of+/- 100 ppm because no received signal will ever have a frequency offset greater than+/- 20 ppm. Thereceiver specification should be changed to what is required in line with thetransmitter and transport network specification.

*SuggestedRemedy*

Add an extra column for 10GBASE-LW with 139.95328 GBd as rate and +/-20ppm as clock tolerance in the same way as it isin Table 52-12.

*Response*    *Response Status* **U**

REJECT.

See response to comment 96 of D4.2 (or #99200) for an updated explanation.

*Cl* **52**    *SC* **7.2**    *P* **453**    *L* **14**    **#** **99048**

Geoffrey Garner    Lucent Technologies

*Comment Type* **TR**    *Comment Status* **R**    *D4.0 #12 clock tolerance*

For the 10GBASE-EW receive optical specifications a clock toleranceof +/-100ppm is specified in table 52-18. This is more than is required inrelation to the transmitter specification and any possible transport network suchas SDH/SONET, OTN, and also old legacy 10 G WDM transponder equipment. As such,the specification is internally inconsistent and also inconsistent with respect totransport equipment. There is no reason to require the receiver to have a tolerance of+/- 100 ppm because no received signal will ever have a frequency offset greater than+/- 20 ppm. Thereceiver specification should be changed to what is required in line with thetransmitter and transport network specification.

*SuggestedRemedy*

Add an extra column for 10GBASE-LW with9.95328 GBd as rate and +/-20ppm as clock tolerance in the same way as it isin Table 52-17.

*Response*    *Response Status* **U**

REJECT.

See response to comment 96 of D4.2 (or #99200) for an updated explanation.

TYPE: TR/technical required  T/technical  E/editorial    COMMENT STATUS: D/dispatched  A/accepted  R/rejected    SORT ORDER:  Clause, Page, Line, Subclause
RESPONSE STATUS: O/open  W/written  C/closed   U/unsatisfied  Z/withdrawn

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*Cl* **52**    *SC* **7.2**

*Cl* **52**     *SC* **7.2**                    *P* **453**        *L* **14**            **#**  **99047**

Rick Townsend                              Lucent Technologies

*Comment Type*   **TR**        *Comment Status*   **R**              *D4.0 #34 clock tolerance*

For the 10GBASE-EW receive optical specifications a clock toleranceof +/-100ppm is specified
in table 52-18. This is more than is required inrelation to the transmitter specification and any
possible transport network suchas SDH/SONET, OTN, and also old legacy 10 G WDM
transponder equipment. As such,the specification is internally inconsistent and also inconsistent
with respect totransport equipment.  There is no reason to require the receiver to have a
tolerance of+/- 100 ppm because no received signal will ever have a frequency offset greater
than+/- 20 ppm.  Thereceiver specification should be changed to what is required in line with
thetransmitter and transport network specification.

*SuggestedRemedy*

Add an extra column for 10GBASE-LW with9.95328 GBd as rate and +/-20ppm as clock
tolerance in the same way as it isin Table 52-17.

*Response*                      *Response Status*   **U**

REJECT.

See response to comment 96 of D4.2 (or #99200) for an updated explanation.

TYPE: TR/technical required  T/technical  E/editorial    COMMENT STATUS: D/dispatched  A/accepted  R/rejected    SORT ORDER:  Clause, Page, Line, Subclause

RESPONSE STATUS: O/open   W/written  C/closed   U/unsatisfied  Z/withdrawn

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*Cl* **52**        *SC* **7.2**