Clock tolerance and insert or delete idles

Given two clocks at different frequencies, the relative error increases with time according to:

$$\Delta\phi = \int_0^{\infty} \Delta f dt$$

This value becomes unbounded as time progress.

The question is, how much mismatch between clocks can we tolerate before our FIFO's folds overflow or underflow.

1. We can only add or delete in 10 bit increments during idle.
2. A maximum packet is 9k bytes, 90k bits.
3. The bits are distributed over 4 lanes.

A maximum packet has a duration of:

$$\frac{90k\ bits}{4\ lanes} 320ps = 7.2\mu s$$

Given a +/-100ppm difference in the clocks, we can accumulate:

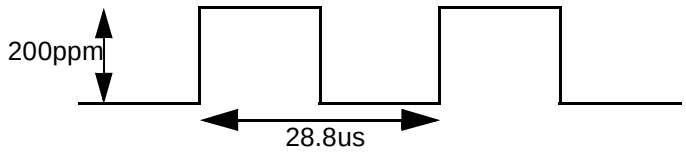
$$7.2\ .10^{-6}\left(\frac{200}{1x(10)^{-6}}\right) = 1440ps$$

$$\frac{1440ps}{320ps} = 4.5bits$$

4.5 bits is in the middle off our compensation range, we can not correct for this.

We now extend our analysis to 2 maximum length packets separated by a negligible idle. Now we accumulated 9 bits, over 14.4us.
During the next idle, we can compensate by subtracting or adding 10 bits.

The above analysis assumed a static, or "DC" offset between the clocks.
Thus it is clear that below a certain frequency of variation, the jitter specification is meaningless, because longer periods will be compensated by the elasticity buffer.
This frequency is determined as follows:



A square wave with a high period of 28.8 us is equal to the above analysis. This corresponds to a frequency of:

$$\frac{1}{28.8us} = 34.72kHz$$

For sine wave variations, there are two alternatives:

1. We can accommodate a 314ppm clock difference at 34.72kHz.
2. We can accommodate a 200ppm clock difference at 22.1kHz.