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A comparison of ITU-T and FC/GE jitter methodology applied to jitter tolerance and eye opening measurements on high-speed CDRs

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This document presents specific jitter tolerance measurement for several different GIGA Clock and Data Recovery (CDR) devices at 2.488 Gb/s, 3.125 Gb/s and 10 Gb/s.

This investigation was made due to the discussion on 10GE jitter budget specification (Austin, 7. – 8. dec. 2000), which was leveraged from the 1GE (a total jitter of 0.7 UIpp). I commented that this may be obtainable at 2.5 Gb/s but difficult to achieve at 10 Gb/s. These were the devices available at that time.

Recently, GIGA released a 3.125 Gb/s (clock reference-free) XAUI compliant CDR, which encouraged me to do more measurements for comparison.

All 3 devices is fabricated in the same bipolar Silicon process suitable for high-speed circuits. The results from this investigation is expected to be general achievable and shows the limitation of the process technology when the bit-rate increases.

One should note, that generally jitter tolerance of the 2.5 and 10 Gb/s devices are measured according to the ITU SDH/SONET specifications (measured as the sinusoidal jitter that generates a 1 dB optical receiver sensitivity penalty – i.e. a relative measurement technique that links time wise jitter to the amplitude domain.)

Actually, I do not have the optical front-end (and its impact on the signal) included in the measurements, because of several reasons. First of all I am focusing on the detailed performance of the CDR itself and do not have all the optical components required for a total system experiment. However, the electrical test set-up incorporates a white noise source, which emulated the noise of the optical front-end. The white noise is added to the differential data signal from the HP 12.5 Gb/s test-set in order to control the SNR at the input of the CDR. Additional SDH filters (1.87 GHz Bessel-Thomson) can be added in order to bandwidth limiting the 35 ps rise/fall time pulses from the test-set (i.e. close to raised cosine pulses). A second benefit is the control of the noise bandwidth. Normally, some bandwidth limitation will be the case in a well designed optical front-end. The jitter is added as sinusoidal phase modulation on to the clock of the test-set.

This experimental measurement set-up shows examples of realistic jitter tolerance limitations set by the CDR, signal quality (rise/fall, noise) and the process and package technology. When measured at the input to the device (i.e. at the equivalent TP4, though it is not a compliance point within the 10GE specification) the CDR performance sets the outmost limitation to the obtainable jitter tolerance of the module (at TP3.)

For jitter frequencies below the 3 dB bandwidth, the PLL of the CDR is able to track most of the input jitter. The important part of this investigation and comparison is the high-frequency part of the jitter spectrum, where the CDR only tracks the average line rate and does not track the incoming jitter. Bit errors start to occur when the peak to peak jitter increases and the set-up and hold time of the decision gate is violated.

As the CDR does not track the jitter, it neither cares about the frequency nor the spectral or temporal jitter distribution. With this in mind, all that matters to the CDR is the total peak-to-peak jitter (TJ) value (independent on the distribution of the individual jitter components DCD, RJ, DJ, SJ). This exploits the maximum horizontal eye opening present at the input of the decision gate and defines the on-set of bit errors when the jitter is increased.

2.5 Gb/s CDR jitter tolerance test results (SDH / SONET)

The GIGA device GD16547B is a 1:1 Clock and Data Recovery with a highly sensitive Limiting Input Amplifier (LIA). It has an absolute differential input sensitivity of less than 5 mVpp. When operated with the white noise source, a typical input swing of 2*100 mVpp is used, in order to control the external SNR.

The jitter tolerance of the CDR with different input signal conditions is shown in the figure below. The PLL bandwidth has been optimised to fulfil both the ITU jitter tolerance and transfer masks (i.e. 1 MHz and 2 MHz respectively, and max. 0.1 dB peaking).

The jitter performance of the decision gate of the CDR is around 0.68 UIpp for the three conditions:

1) A clean signal, tr/tf approximately 35 ps
2) same signal as 1) with noise added to give a 1 dB optical penalty jitter measurement.
3) same signal as 1) with SDH filters (1.87 GHz Bessel-Thomson) resulting in tr/tf = 170 ps.

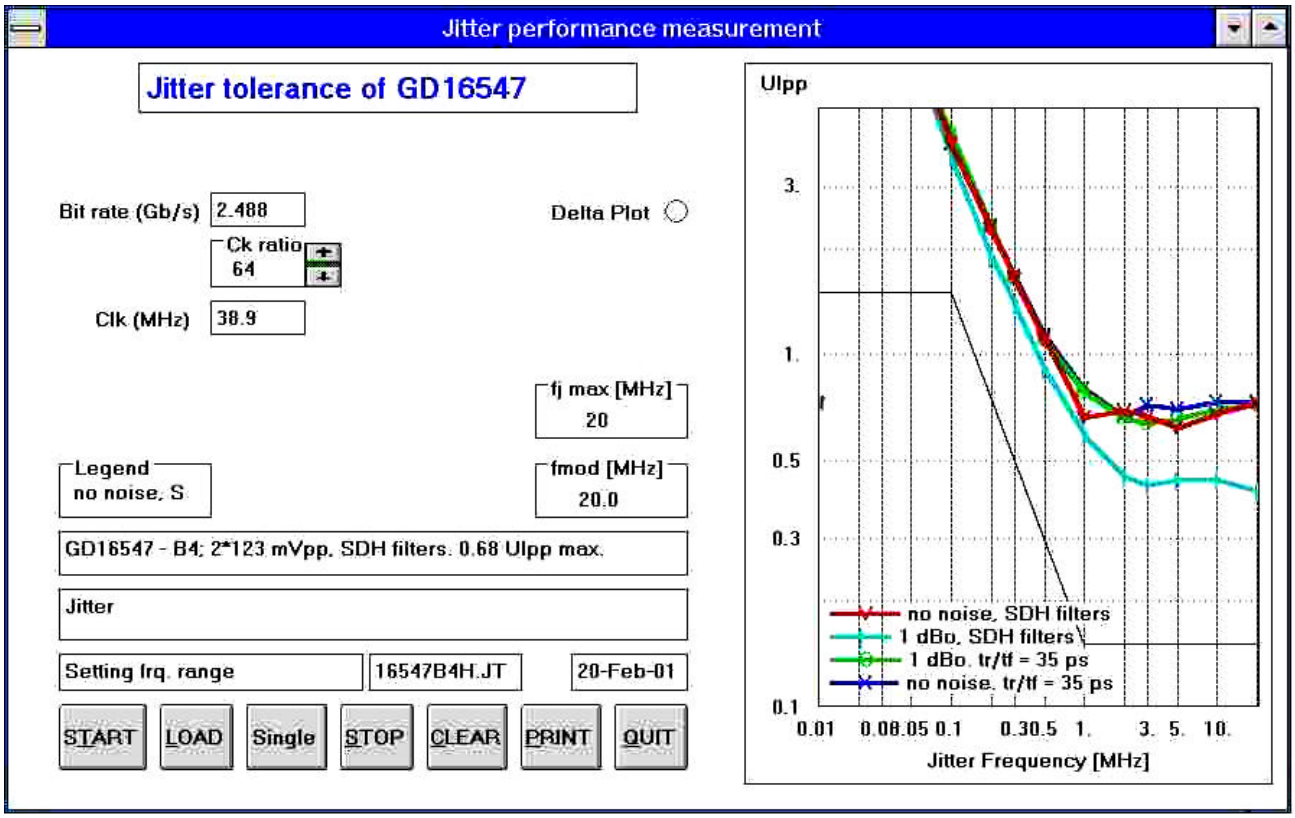

Figure 1. 2.488 Gb/s LIA CDR jitter tolerance under different input signal conditions.

This shows that neither signal bandwidth limitation nor additive white noise impact the jitter tolerance of the CDR (i.e. the horizontal eye opening at the sampling point is unchanged) because the two (separate) signal conditioning elements mainly affect the signal waveform (i.e. amplitude domain) and not (significantly) the time domain (jitter).

Also, the decision gate set-up and hold time can be calculated as (1 UI – 0.68 UI) * 400 ps/UI = 128 ps.

Only the **combined** effect of the SDH filters and the addition of white noise, lowers the jitter tolerance to around 0.4 UIpp. This is because of the AM to PM conversion of the noise, due to the finite slope of the pulses, arising from the signal bandwidth limiting SDH filters.

A similar 1 dB penalty jitter tolerance value for an optical module was verified and reported by Paul Wilson, Nortel Networks.

3.125 Gb/s lite CDR (no reference clock required).

The GIGA device, GD41644, is a low-power (290 mW), clock reference-free 1:1 Clock and Data Recovery designed for XAUI, on-board signal conditioning/regenerator and backplane applications (size: 4*4 mm leadless plastic package). It has an absolute differential input sensitivity of less than 10 mVpp.

Similar to the 2.488 Gb/s device, the highest obtainable jitter tolerance (at TP4) of the 3.125 Gb/s CDR is measured to be 0.64 UIpp for a clean input signal with fast signal edges. Decision gate set-up + hold time: (1 UI – 0.64 UI) * 320 ps/UI = 115 ps.

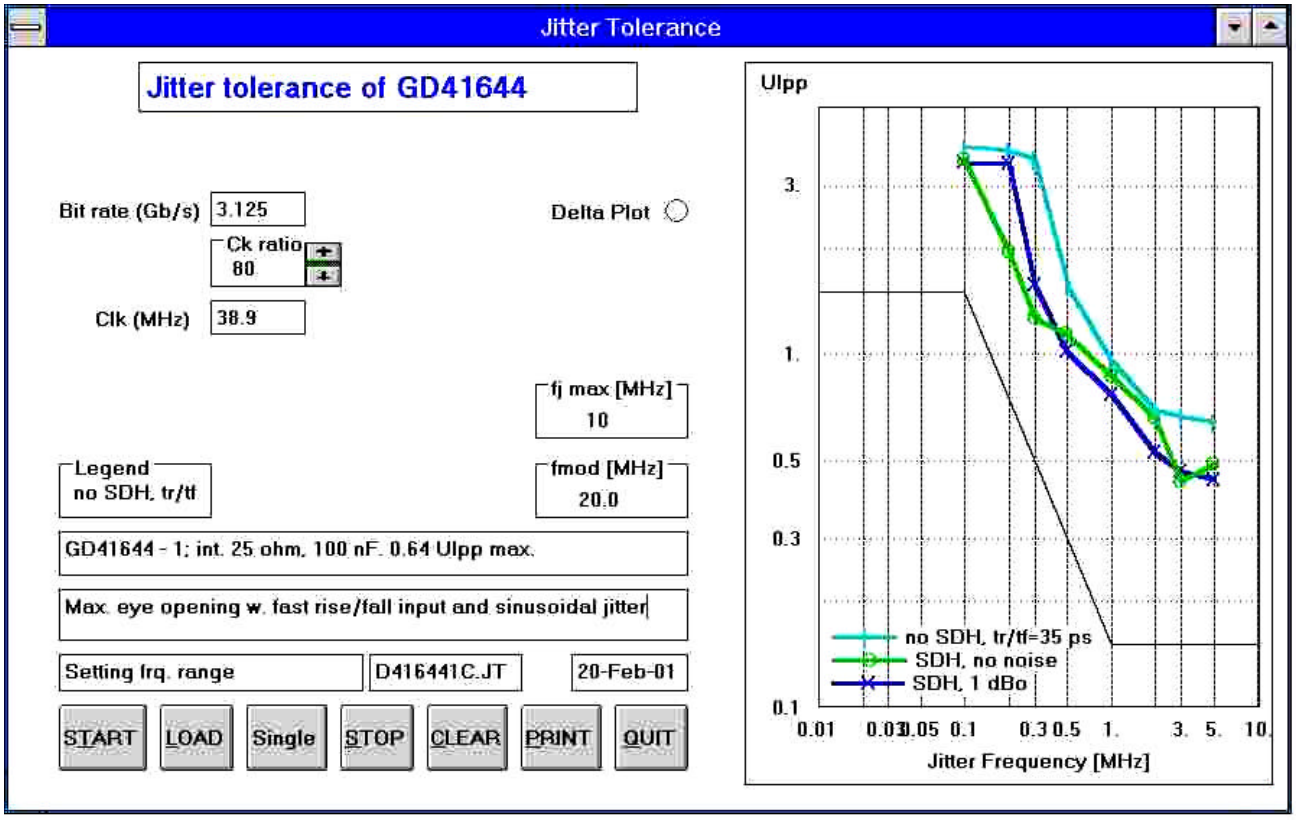

Figure 2: 3.125 Gb/s CDR jitter tolerance under different input signal conditions.

Inserting the SDH filters (though the bandwidth is a little too low and thus giving slightly more pattern jitter and amplitude reduction of single symbols. However, this is almost compensated by the relative penalty method. It implies a slightly larger overall SNR in order counteract the amplitude reduction and the fact that bit error tends to happen on the bits with the lowest amplitude), shows that the jitter tolerance has drops to 0.4 UIpp with / without white noise added to the signal. This is understood from the above-mentioned impact from the too narrow SDH filters.

The important point or conclusion from the 2.488 Gb/s and 3.125 Gb/s measurements shows consistently that the maximum jitter the CDR can handle without generating bit errors, i.e. the jitter tolerance (at TP4) is definitely less than 0.7 UI. This is a relevant comment to the recently changed jitter numbers in the 10GE XAUI specifications.

10 Gb/s CDR jitter tolerance

The GIGA device, GD16584, is a 10 Gb/s Clock and Data Recovery with a 1:16 demultiplexer. A Limiting Input Amplifier (LIA) has been added externally, as the process technology does not allow for sufficient gain-bandwidth of an integrated LIA stage. The input swing at the LIA is 2*12 mVpp with a small signal gain of 40 dB and 2*800 mVpp output swing.

The jitter tolerance of the CDR with different input signal conditions is shown in the figure below. The PLL bandwidth has been optimised to fulfil the ITU jitter tolerance masks (i.e. around 6 MHz, and max. 0.1 dB peaking).

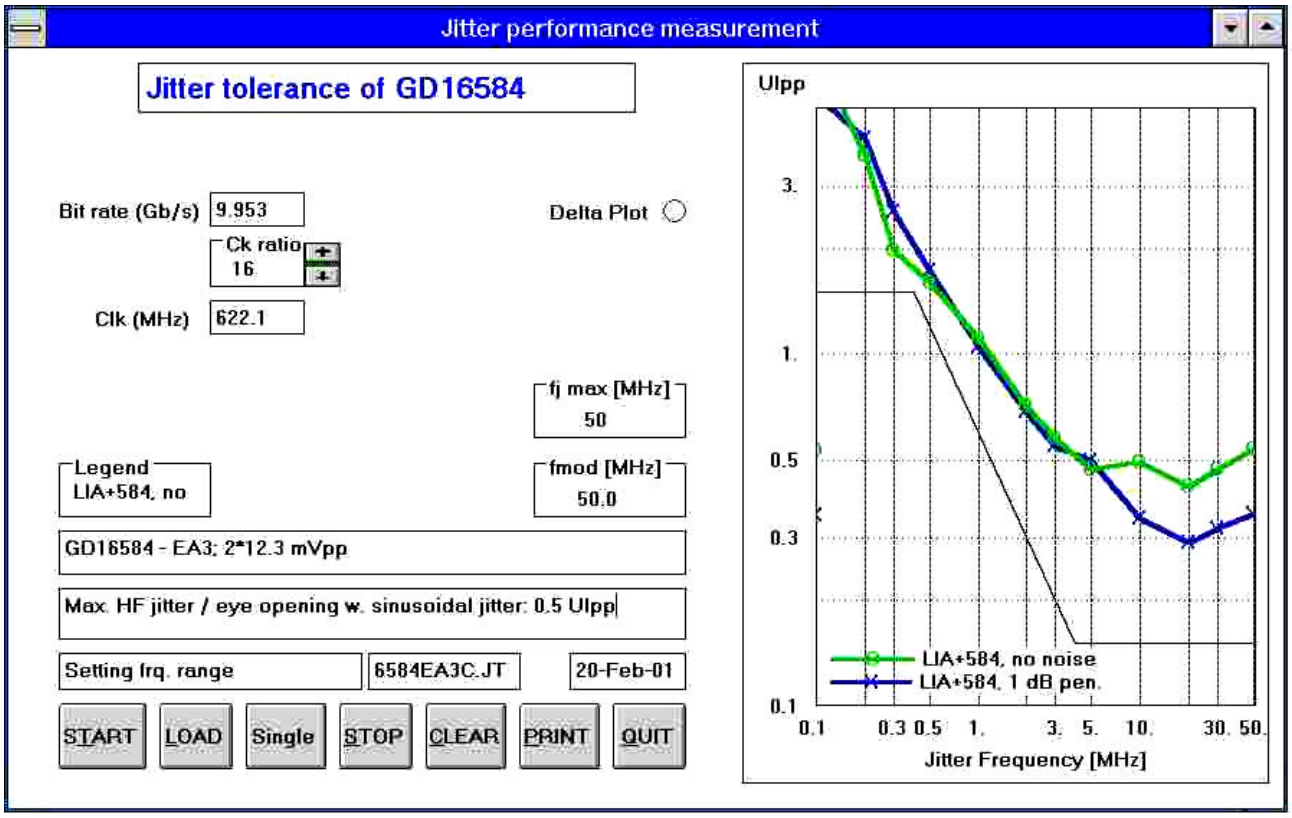

Figure 3: 9.953 Gb/s CDR jitter tolerance under different input signal conditions.

The jitter tolerance of the decision gate of the CDR with a clean input signal 0.5 UIpp, which gives a set-up + hold time of 50 ps. The reduction of jitter tolerance relative to the 2.488 Gb/s examples is due to more critical signal transmission on the FR-4 PCB and bandwidth limitations of the process technology.

When noise is added and using the ITU 1 dB optical penalty measurement method the jitter tolerance drop to 0.3 UIpp. This is again due to the AM-PM noise conversion, due to the finite 35 ps rise/fall time of the pulses.

The important result from this measurement is the maximum jitter of 0.5 UIpp that a realistic 10 Gb/s CDR can handle (at TP4) outside the PLL bandwidth.

Conclusion

The experimental jitter tolerance measurement results in this document shows the difference between ITU-T 1 dB power penalty jitter method and FC/GE when applied to realistic/physical CDR devices.

It also shows the impact of the process bandwidth limitations when the bit rate increases and the technology is pushed to its limits. At high speed, the required set-up and hold time does not scale with the bit period and therefore less time is left for the timing jitter – horizontal eye opening as measured by the noise-free jitter tolerance results.

For the current the 10GE jitter specification the total jitter seems to put more strict requirements to the jitter tolerance than what is actually required in SDH / SONET systems. The devices tested here this document is used world wide in SDH system, so the jitter performance is adequate. I think, that these CDR is close to the optimum performance given the process limitations.

It may be possible to design CDRs in advanced / sophisticated process, but this will probably not be a cheap solution, which is one of the objectives in 10GE.