XGMII: HSTL and/or SSTL2

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OUTLINE

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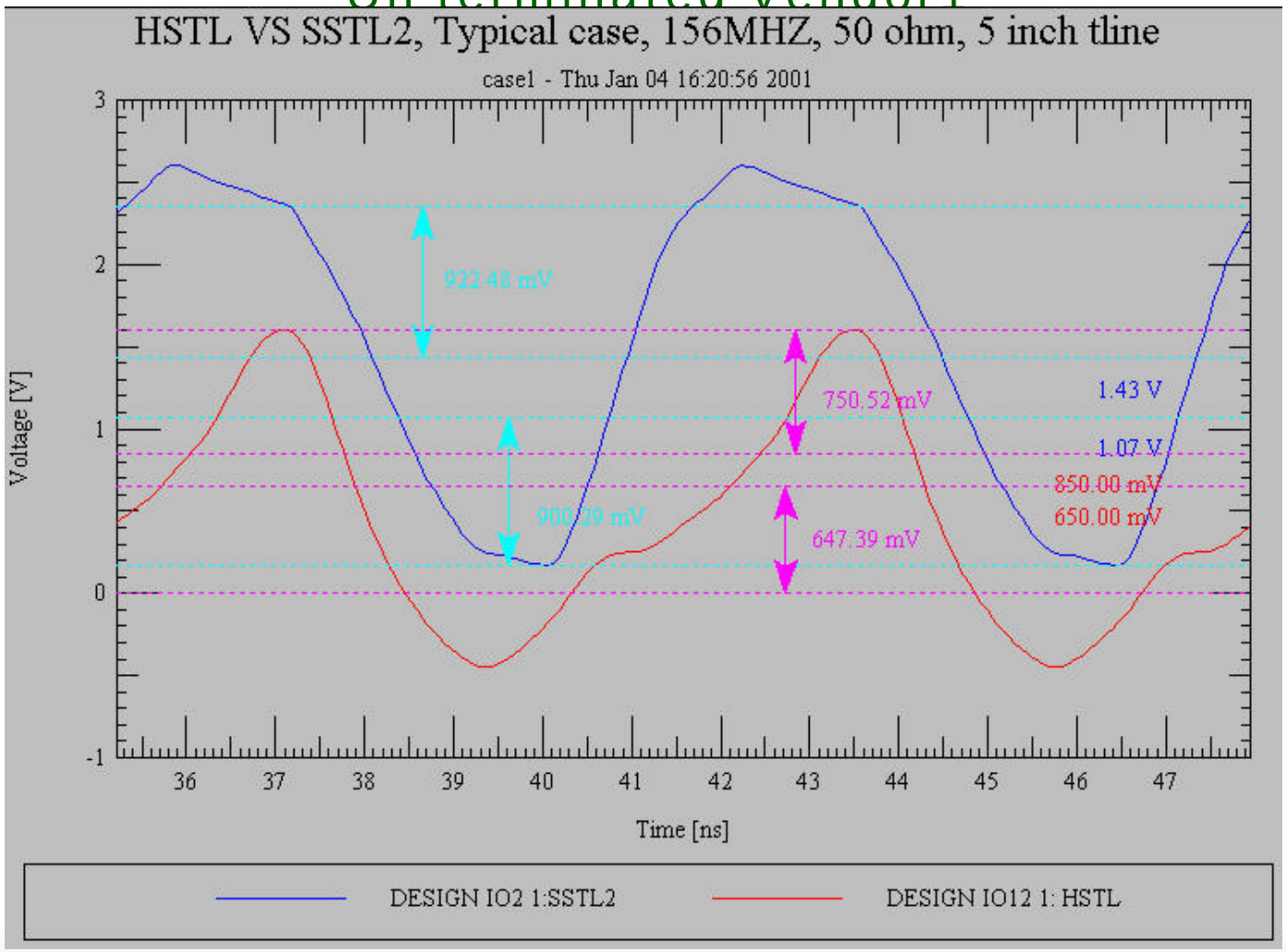
HSTL Class I Specification

- Vih vref+100mv min
- Vil vref-100mv max
- Voh vddq-400mv min
- Vol 400mv max
- 8ma Driver
- Series terminated or parallel terminated to vddq/2.

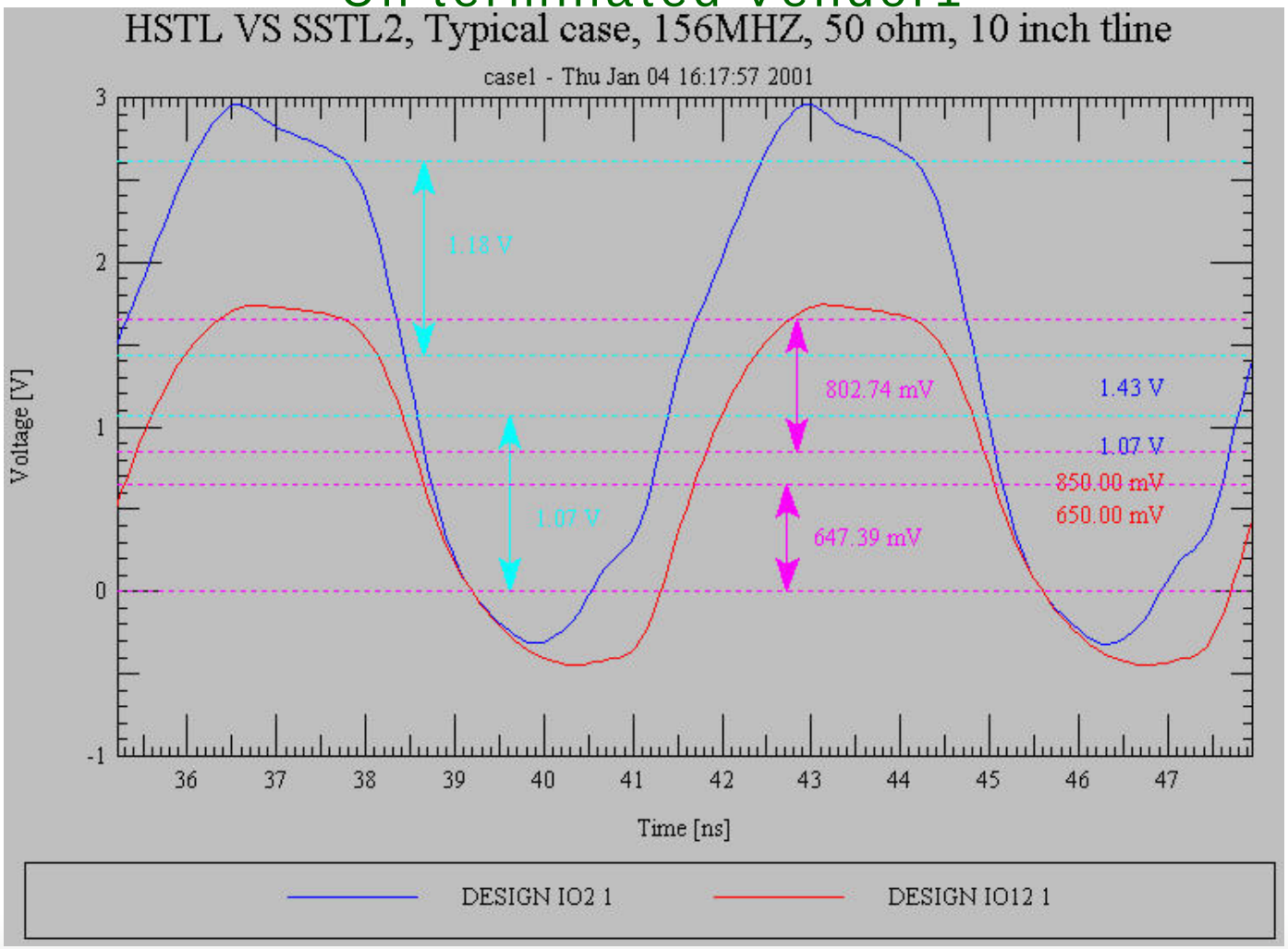
SSTL2 Class I Specification

- Vih vref+180mv min
- Vil vref-180mv max
- Voh vtt+570mv min
- Vol vtt-570mv max
- 7.6ma Driver
- Series terminated or parallel terminated to vddq/2.

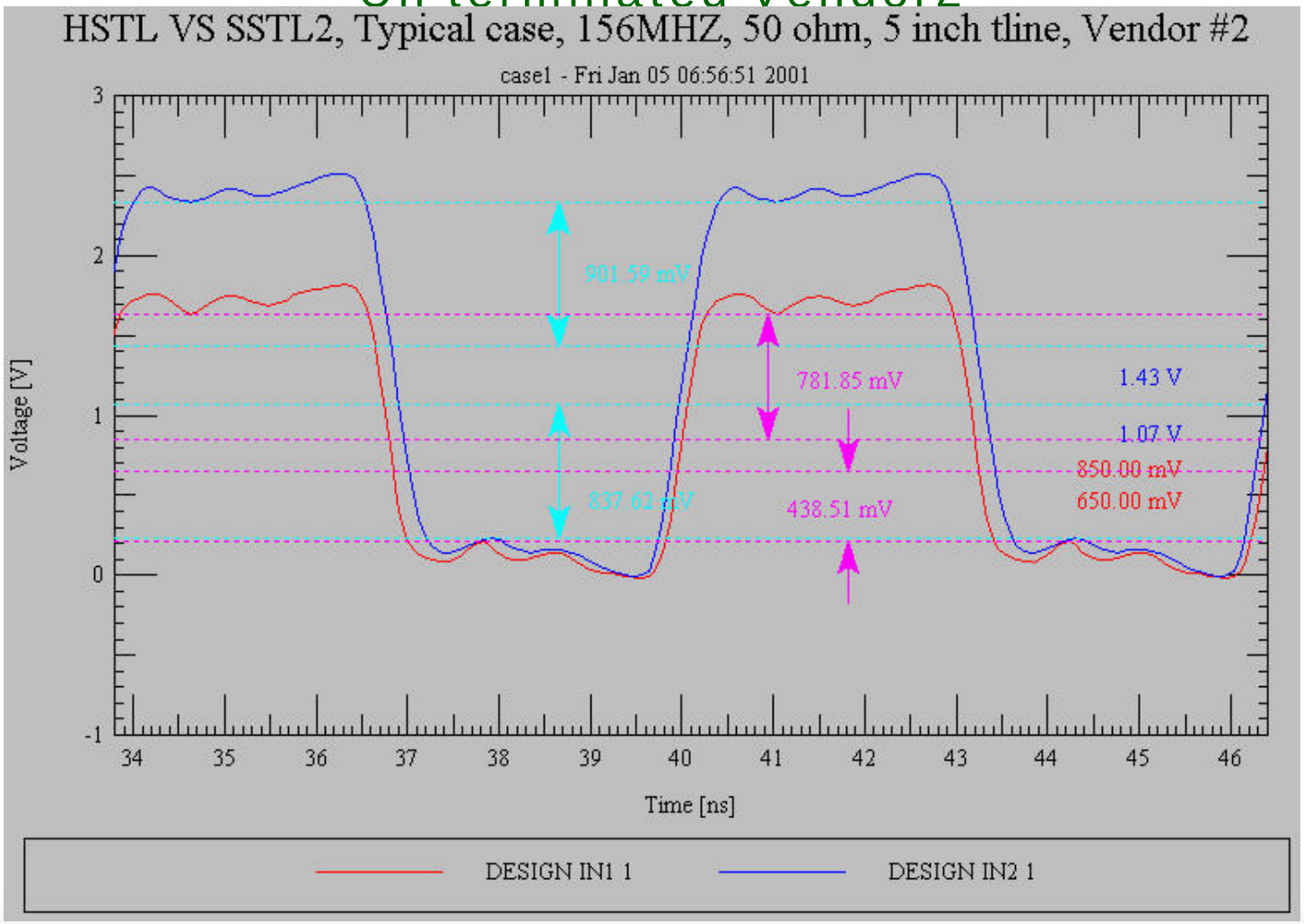
HSTL vs SSTL2 5”T-line
Un-terminated Vendor1



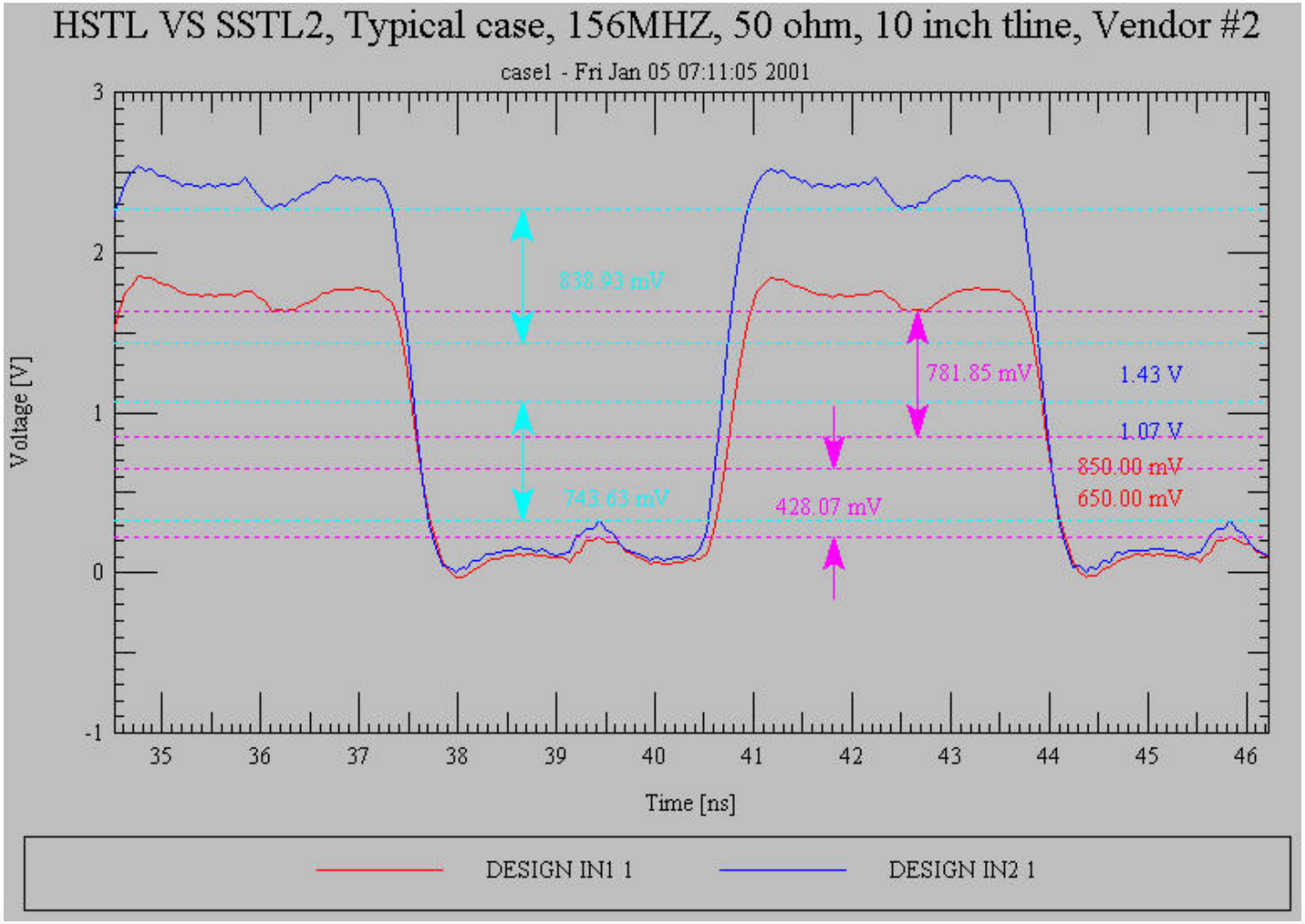
HSTL vs SSTL2 10”T-line
Un-terminated Vendor1



HSTL vs SSTL2 5”T-line
Un-terminated Vendor2



HSTL vs SSTL2 10”T-line
Un-terminated Vendor2



System Design Comparison

Advantage	HSTL	SSTL2
Slightly Lower Power consumption	X	
Slightly Higher Noise Margin		X
Termination Requirements	X	X
Routing/space for termination	X	X
Hold skew across XGMII	X	X
Drive length		X
Spice/IBIS Available	X	X

XGMII Applications

- System support
  - We can't get clock drivers for 1.8/1.5 volt parts. They are barely available for 2.5 volt components.
  - MACs using SSTL2 I/O cells already exist requiring the XGMII on the PCS side to support both HSTL and SSTL2.
- Routing layers
  - Reference oif2000.308.1 – putting multiple SERDES in a 1200pin or 1600pin ASIC to remove the XGMII will result in more layers then if the ASIC and the SERDES are kept separate.

Summary

- Both HSTL and SSTL2 I/O cells have very similar capabilities.
- I/O cells have been developed by many vendors to support both HSTL and SSTL2.
- The market is/will require SERDES vendors designing to the PCS side of the XGMII to support both HSTL and SSTL2 in an effort to satisfy both existing and emerging technologies.