IEEE P802.3ae
10 Gigabit Ethernet Task Force

XGMII Update

La Jolla, CA
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Goals and Assumptions

- Allow multiple PHY variations
- Provide a convenient partition for implementers
- Provide a standard interface between MAC and PHY
- Reference industry standard electrical specifications
10 Gigabit Media Independent Interface

- 32 data bits, 4 control bits, one clock, for transmit
- 32 data bits, 4 control bits, one clock, for receive
- Dual Data Rate (DDR) signaling, with data and control driven and sampled on both rising edge and falling edge of clock

- 32 bit data paths are divided into four 8 bit “lanes”, with one control bit for each lane
10 Gigabit Media Independent Interface - Coding

- Use embedded delimiters rather than discrete signals
- Control bit (C) is “1” for delimiter and special characters
- Control bit (C) is “0” for normal data characters
- Delimiter and special character set includes:
  - Idle, Start, Terminate, Error
- Delimiters and special characters are distinguished by the value of the 8 bit data lane when the corresponding control bit is “1”
- Data (d) symbols are striped on lane 1, lane 2, lane 3, lane 0, etc.
  - Frames (packets) may be any number of symbols in length subject to minFrameSize and maxFrameSize
10 Gigabit Media Independent Interface - Coding

- **Idle (I) is signaled**
  - during the Inter-Packet Gap
  - when there is no data to send

- **Start (S) is signaled**
  - for one byte duration at the beginning of each packet
  - always on lane 0

- **Terminate (T) is signaled**
  - for one byte duration at the end of each packet
  - may appear on any lane

- **Error (E) is signaled**
  - when an error is detected in the received signal
  - when an error needs to be forced into the transmitted signal
# 10 Gigabit Media Independent Interface - Coding

<table>
<thead>
<tr>
<th>Shorthand</th>
<th>Name</th>
<th>Code Point (Control)</th>
<th>Code Point (Data)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Idle</td>
<td>1</td>
<td>0x07</td>
</tr>
<tr>
<td>S</td>
<td>Start</td>
<td>1</td>
<td>0xFB</td>
</tr>
<tr>
<td>T</td>
<td>Terminate</td>
<td>1</td>
<td>0xFD</td>
</tr>
<tr>
<td>E</td>
<td>Error</td>
<td>1</td>
<td>0xFE</td>
</tr>
<tr>
<td>d</td>
<td>Data</td>
<td>0</td>
<td>0x00 - 0xFF</td>
</tr>
</tbody>
</table>
10 Gigabit Media Independent Interface - Example

clk
C0
D<0:7>
C1
D<8:15>
C2
D<16:23>
C3
D<24:31>

IEEE 802.3ae
10 Gigabit Ethernet
10 Gigabit Media Independent Interface -
Electrical Characteristics

- Use Stub Series Terminated Logic for 2.5 Volts
  - SSTL_2
  - EIA/JEDEC Standard EIA/JESD8-9
  - Class I (8 ma) output buffers

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDQ</td>
<td>Supply Voltage</td>
<td>2.3</td>
<td>2.5</td>
<td>2.7</td>
</tr>
<tr>
<td>VREF</td>
<td>Reference Voltage</td>
<td>1.15</td>
<td>1.25</td>
<td>1.35</td>
</tr>
<tr>
<td>VTT</td>
<td>Termination Voltage</td>
<td>VREF-0.04</td>
<td>VREF</td>
<td>VREF+0.04</td>
</tr>
<tr>
<td>VIH(dc)</td>
<td>dc input logic high</td>
<td>VREF+0.18</td>
<td></td>
<td>VDDQ+0.3</td>
</tr>
<tr>
<td>VIL(dc)</td>
<td>dc input logic low</td>
<td>-0.3</td>
<td></td>
<td>VREF-0.18</td>
</tr>
<tr>
<td>VIH(ac)</td>
<td>ac input logic high</td>
<td>VREF+0.35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL(ac)</td>
<td>ac input logic low</td>
<td></td>
<td></td>
<td>VREF-0.35</td>
</tr>
</tbody>
</table>
10 Gigabit Media Independent Interface - Circuit Topology Example

VDDQ

RS = 25 Ohms

Z=50 Ohms

VTT

50 Ohms

VREF
10 Gigabit Media Independent Interface - Timing

Clock

Data or Control

Symbol | Driver | Receiver | Units
--- | --- | --- | ---
t\_\text{setup} | 960 | 480 | ps
t\_\text{hold} | 960 | 480 | ps

\(V_{\text{IH\_AC\_min}}\) | \(V_{\text{IL\_AC\_max}}\)
\(V_{\text{IH\_AC\_min}}\) | \(V_{\text{IL\_AC\_max}}\)
Summary

- The XGMII coding proposal is stable
- The EIA/JEDEC SSTL_2 standard can be referenced for the XGMII electrical specification
- The timing proposal presented herein is a starting point for further discussion