8B/10B Idle Pattern
for
12-byte IPG

Rich Taborek, Don Alderrou nSerial

Presentation Purpose

- Modify 8B/10B Idle pattern to handle 12-byte IPG:
- Maintain all 8B/10B Idle pattern benefits

8B/10B Idle Pattern

- Current proposed 8B/10B Idle pattern
  - Fixed /A/K/R/ followed by randomized /A/ spacing and /K/R/ sequence
  - /K/ used to pad EOP column
- Problem: 12-byte IPG could compromise /R/ availability
  - Affects ability to perform clock tolerance compensation
  - Can't simply rearrange to place /R/ first:
    - Causes /A/ or /K/ starvation, and/or,
    - /R/ deletion may compromise EOP robustness
- Solution: Modify fixed /A/K/R/ to guarantee /R/
  - Start with random /A/K/ as first column following EOP
  - Second column is fixed /R/
  - Third and subsequent columns randomize /A/ spacing and /K/R/ sequence

Data Mapping Example

RS/XGMII Encoded Data

D<7:0,K0>	I	I	S	d_p	d	d	---	d	d	d_f	T	I	I	S	d_p
D<15:8,K1>	I	I	d_p	d_p	d	d	---	d	d	d_f	I	I	I	d_p	d_p
D<23:16,K2>	I	I	d_p	d_p	d	d	---	d	d	d_f	I	I	I	d_p	d_p
D<31:24,K3>	I	I	d_p	d_p	d	d	---	d	d	d_f	I	I	I	d_p	d_p

PCS Encoded Data

Lane 0	R	K	S	d_p	d	d	---	d	d	d	T	A	R	S	d_p
Lane 1	R	K	d_p	d_p	d	d	---	d	d	d_f	K	A	R	d_p	d_p
Lane 2	R	K	d_p	d_p	d	d	---	d	d	d_f	K	A	R	d_p	d_p
Lane 3	R	K	d_p	d_p	d	d	---	d	d	d_f	K	A	R	d_p	d_p

Summary

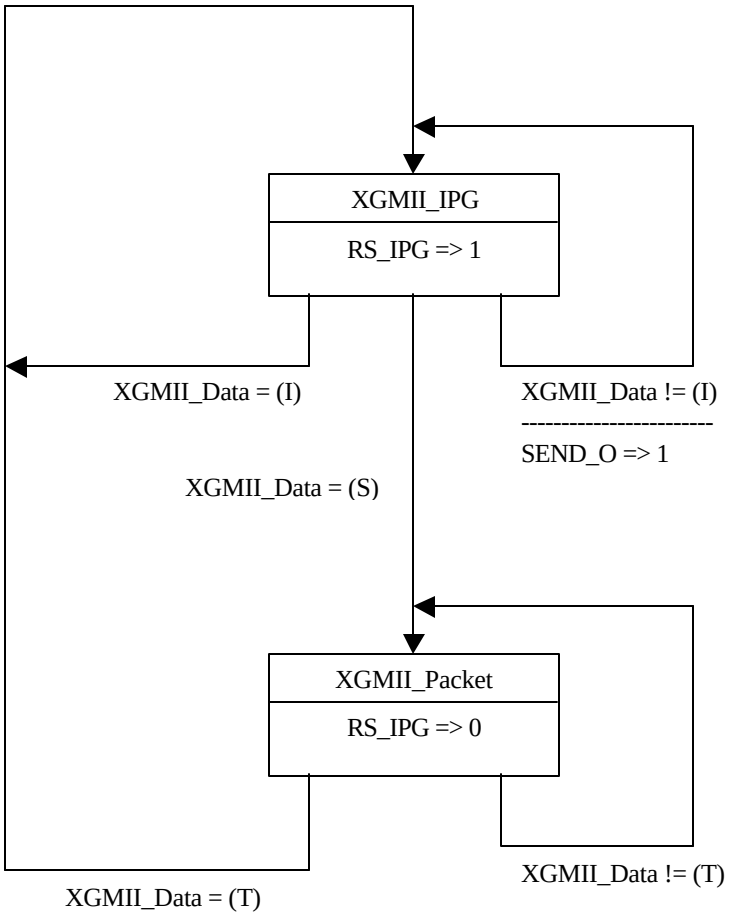
- Concerns of 8B/10B Idle pattern for 12-byte IPG addressed
- Solution is simple rearrangement of fixed Idle start pattern
- Retain all benefits of 8B/10B-based PCS and PMA
- Retain all benefits of XAUI/XGXS protocol
- No additional burden on receiver
- Retain all benefits of Idle EMI enhancements
- All benefits applicable to PCB traces & 4 Channel PMDs

Supplementary Slides

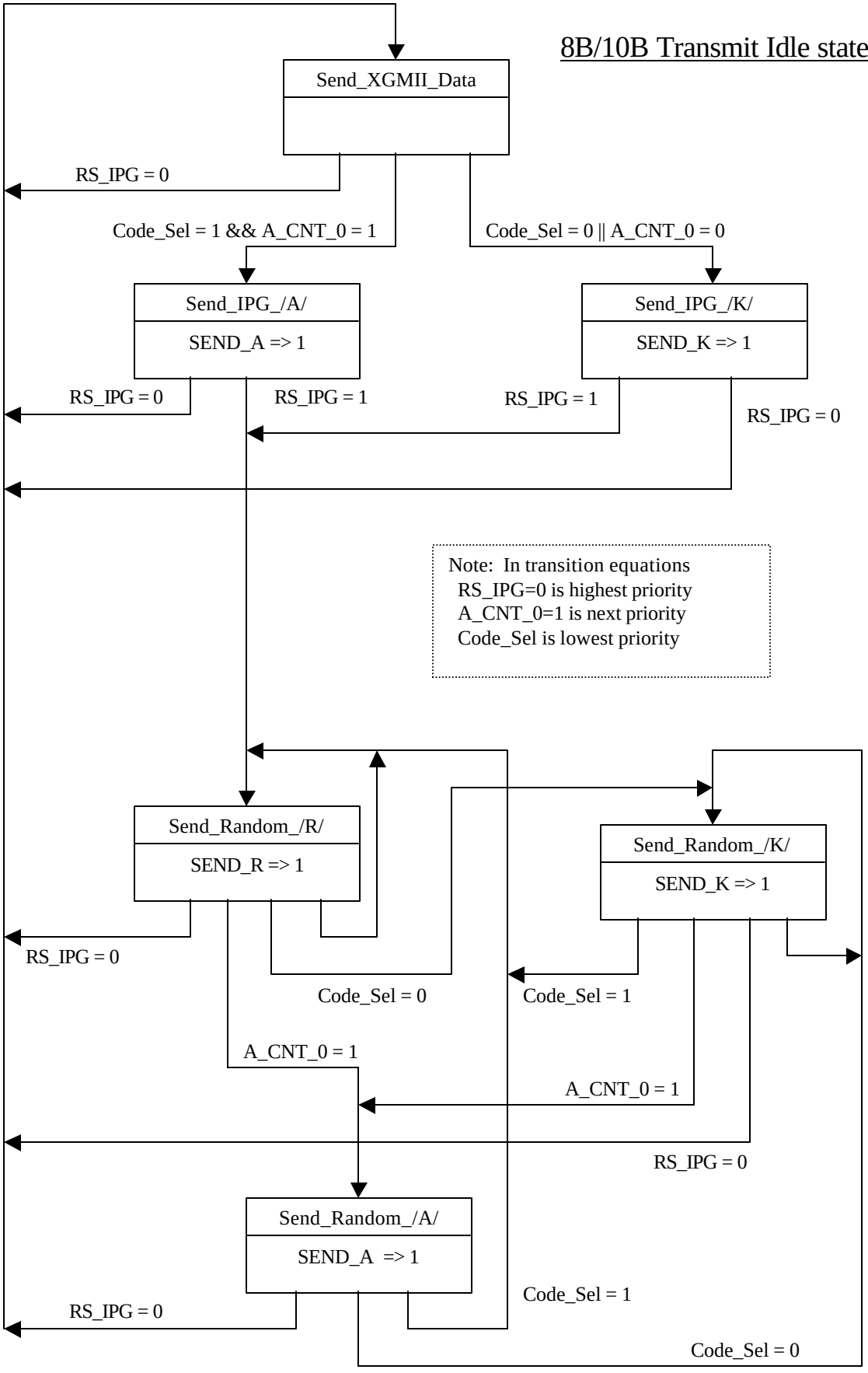
Intended for those that REALLY want to know how this stuff works

- 8B/10B Transmit state diagram
  - Transmit IPG, SOP, EOP or Other (e.g. LSS)
- 8B/10B Transmit Idle state diagram
  - Generate IPG/Random AKR Idle
- 8B/10B Transmit Idle logic diagram
  - AKR Randomizer
- 8B/10B Transmit Data multiplexer diagram
  - Multiplexing of XGMII input and Random AKR Idle

8B/10B Transmit state diagram



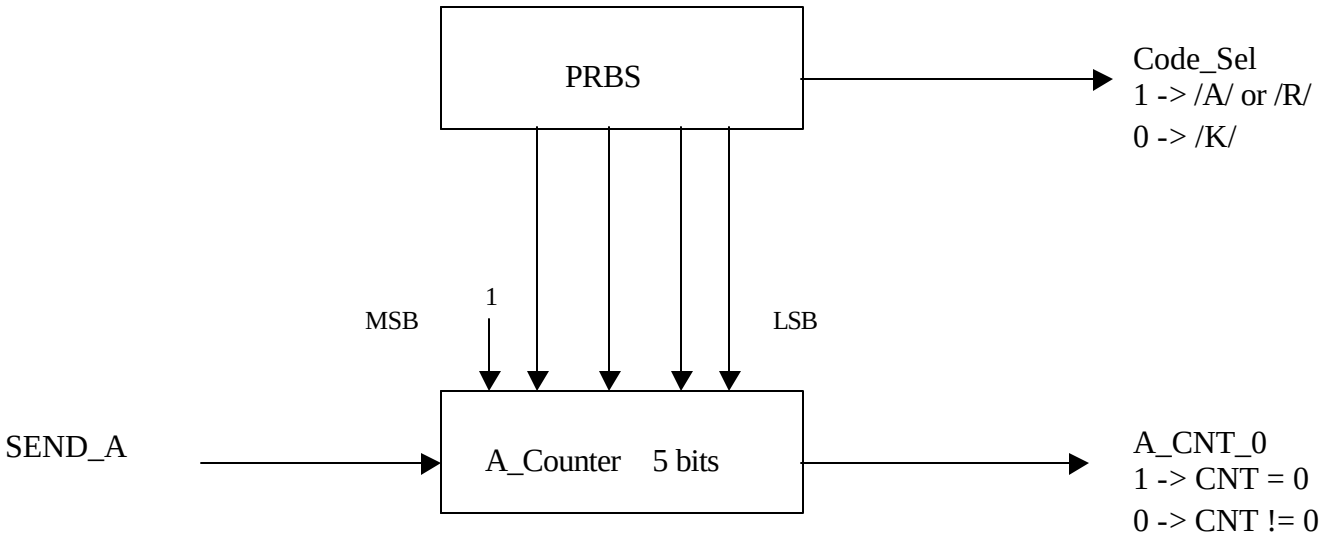
8B/10B Transmit Idle state diagram



8B/10B Transmit Idle logic diagram

The polynomial for the Pseudo-Random Bit Sequencer (PRBS) which has been simulated and tested in the lab is X^7 + X^3 + 1.

Note: it runs serially (one data bit shift per clock) at the byte clock rate.



The A_Counter counts down to zero and is parallel loaded with a random 4-bit pattern from four of the PRBS stages. The MSB is always loaded with a 1 to give the random count between /A/ codes of 16 to 31. It is loaded by the SM when an /A/ code is sent and signals a zero count back to the SM.

8B/10B Transmit Data multiplexer diagram

The data multiplexer selects either the XGMII 32-bit data & 4-bit control or one of the special codes. If none of the SEND_x signals are active, then the XGMII data & control is selected. The SEND_O signal has priority over the other SEND_x signals and will select the XGMII data & control.