

# Hierarchical Decoding of Parallel Serial Streams 

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## Levels of Decoding

F
－Bit locking
－Byte Alignment
－Clock Skew Management
－Lane Matching

Use separate control characters for each：K，S，M At most one KM at each IPG
If longer IPG needed then insert S（s）：KS．．SM Insert 3 S in IPG every 4，000 cycles or better：KSSSM
Packet bytes after every M simplifies lane matching

## Comparison

all lanes: dddddKRKRdddddddKAKRdddddd all lanes: dddddKRKRdddddddKAKdddddd ( lanes lined up \& packet is after last K or R after A ) clock skew (R) adjustment not needed at each IPG lane A: dddddKMdddddddKSSSMdddddd lane B: dddddKMdddddddKSSMdddddd
( lanes not lined up \& packet is after M )
New scheme allows for clock skew per lane and lane matching.

## Example



| clock domain A |  |  | clock domain C |
| :---: | :---: | :---: | :---: |
| MSS | clock domain B | KS | K domain D |

KSSSM
KSSM
KSM
KM

## The Journey of 10GE Data Packets



