A Unified PMD Interface for 10GigE

IEEE 802.3ae

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Agenda

- **What makes the system unified?**
- **Unification around an interface**
- **Unification of coding methods**

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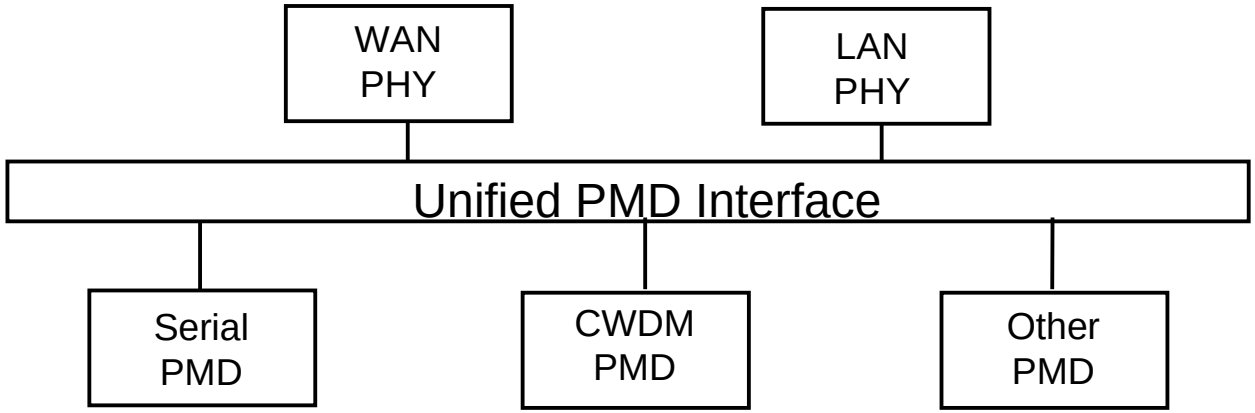
Unification Means:

- **A common PMD interface for both LAN-PHY and WAN-PHY**
- **A PMD interface which is fair to all PMD types including Serial and CWDM**
- **A low pin count interface**
- **A long reach interface (over 20 inches) to improve reach**



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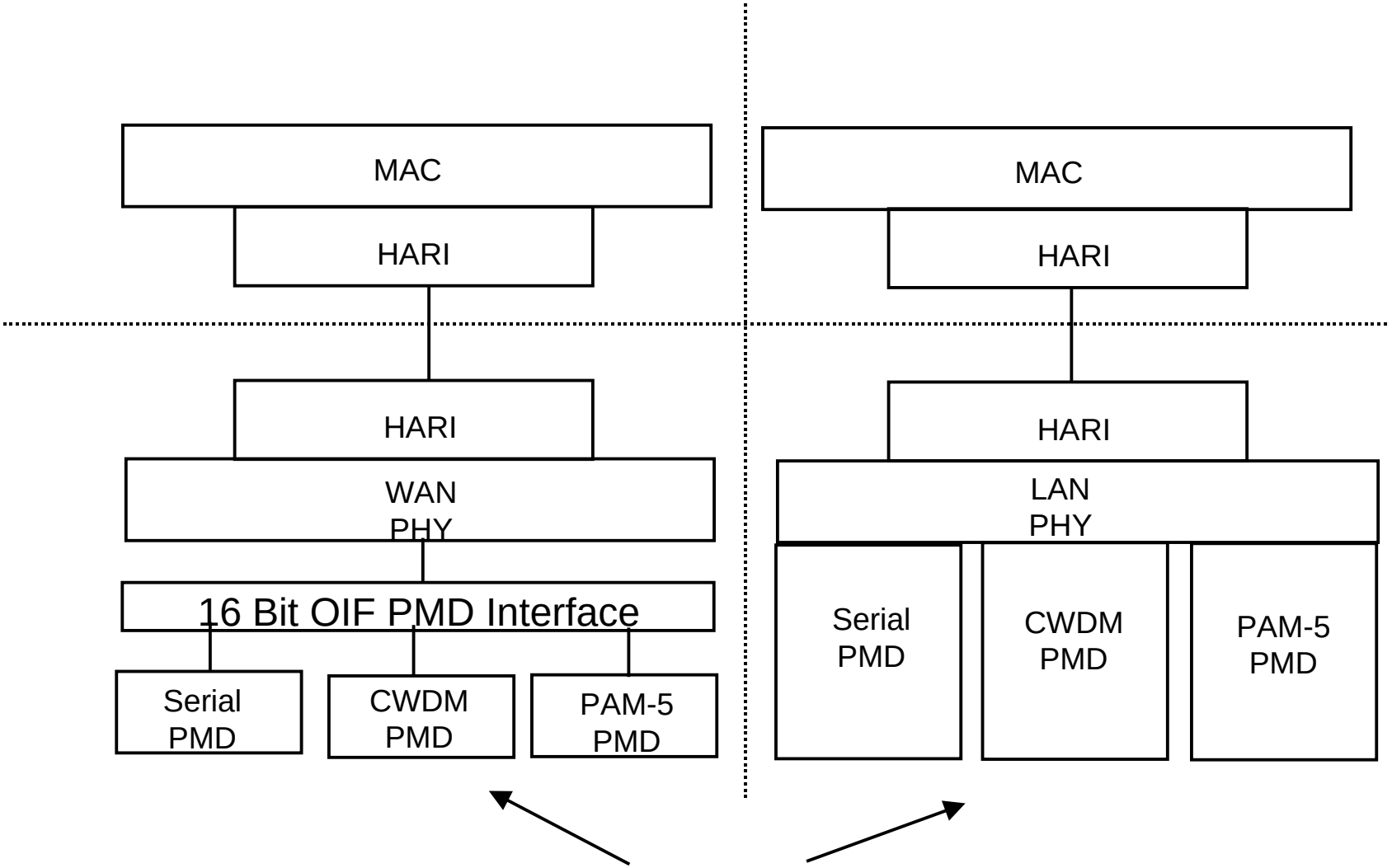
Today's Picture Splits The Market

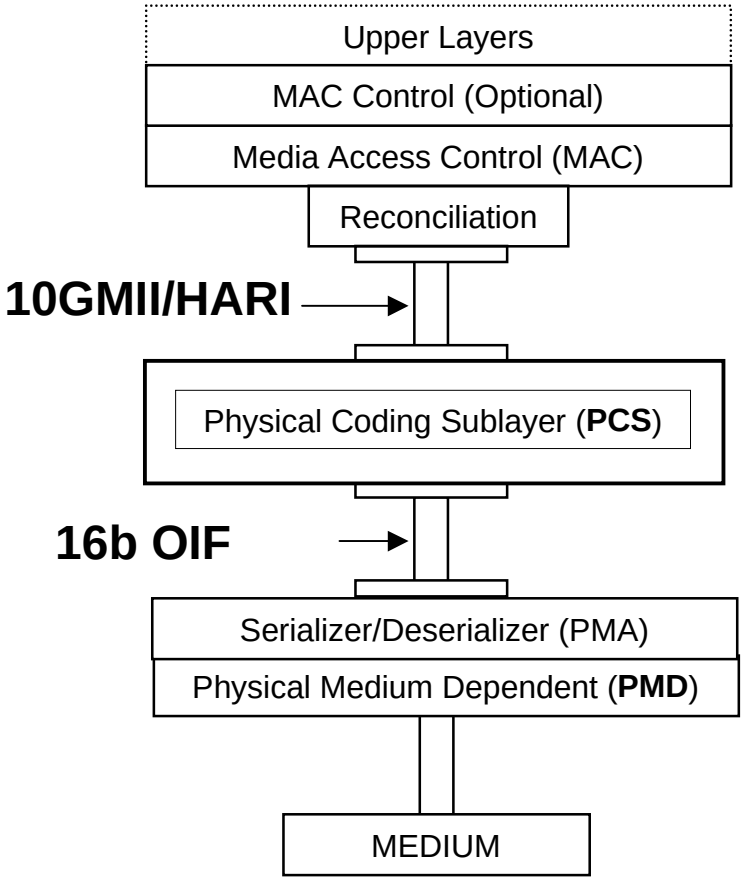


Different PMD Chips

Splitting the stack lower unifies PMDs

- **HARI splits the stack too high forcing the PCS layer into the PMD chip (PCS 64/66, length/type, etc.) layers.**
- **HARI adds unnecessary encoding and protocols**
- **HARI favors both CWDM and LAN-PHY**
- **HARI doesn't work lower in the stack**

10 Gigabit Ethernet Reference Model



The 16b OIF Interface Is Universal

- **The 16b OIF interface splits the stack between the PMA and the PCS layer**
- **It is protocol independent when using slightly different rates for LAN and WAN PCS layers**
- **It is code independent when no byte alignment is assumed over the interface**
- **It can be used for both CWDM and Serial interfaces**

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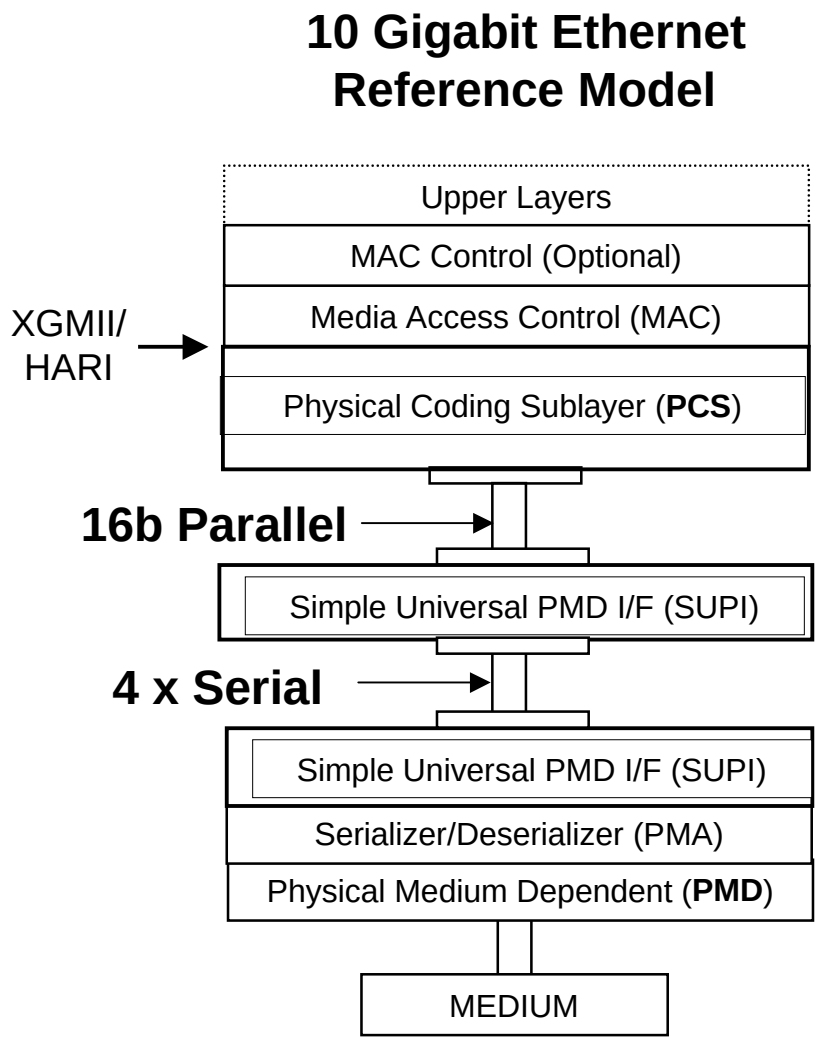
A Narrow Universal PMA Interface

- **Two issues have been mentioned about the OIF 16b interface**
  - — It takes a lot of pins
  - — It can not extend 20 inches
- **A narrow 4 lane version of the 16b interface is possible**
- **Makes the PMD independent for LAN or WAN or CWDM or Serial**



16-bit And 4x2.5 Are PMA Interfaces

- **16-bit LVDS interface**
  - — Optional parallel interface between PCS and PMA
  - — Supports both CWDM/Serial
  - — Current technology
- **4× Pseudo-Random Data (SUPI)**
  - — Optional 4x2.5 interface between PCS to PMA
  - — Supports both CWDM/Serial
  - — Each lane is lower speed than HARI (~2.5)
  - — Consistent semantics with 16-bit LVDS
  - — Future technology

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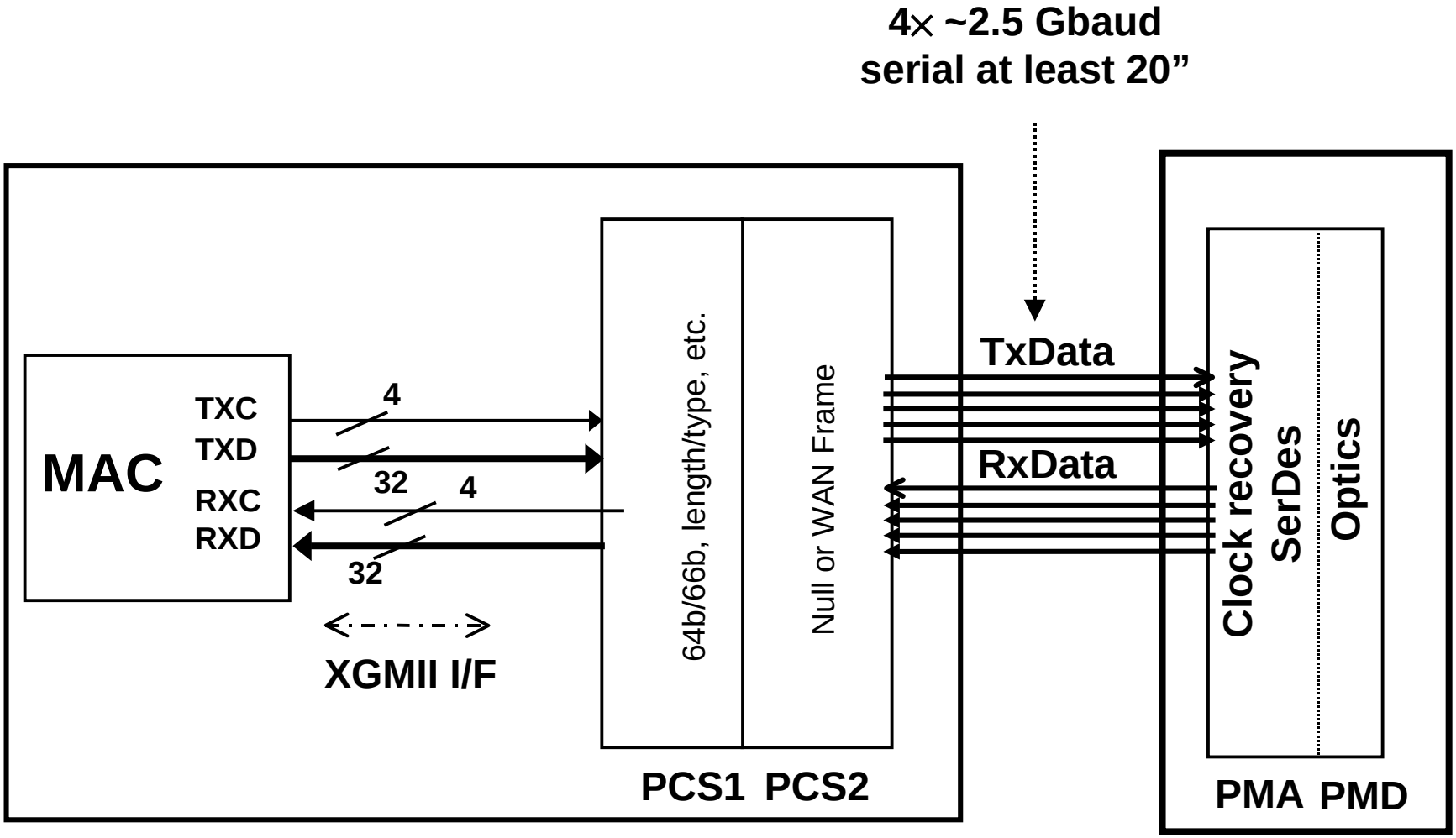
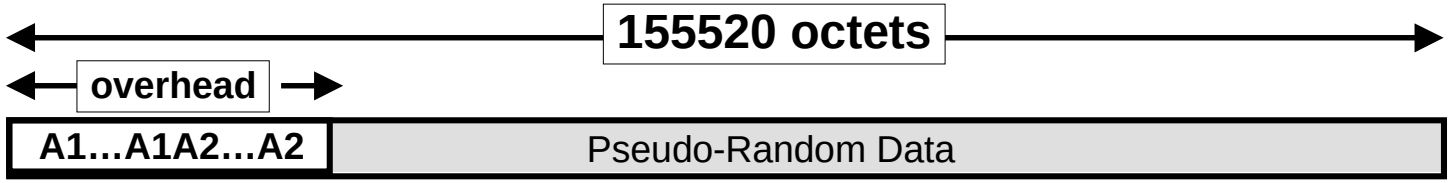
Simple Universal PMD Interface(SUPI)



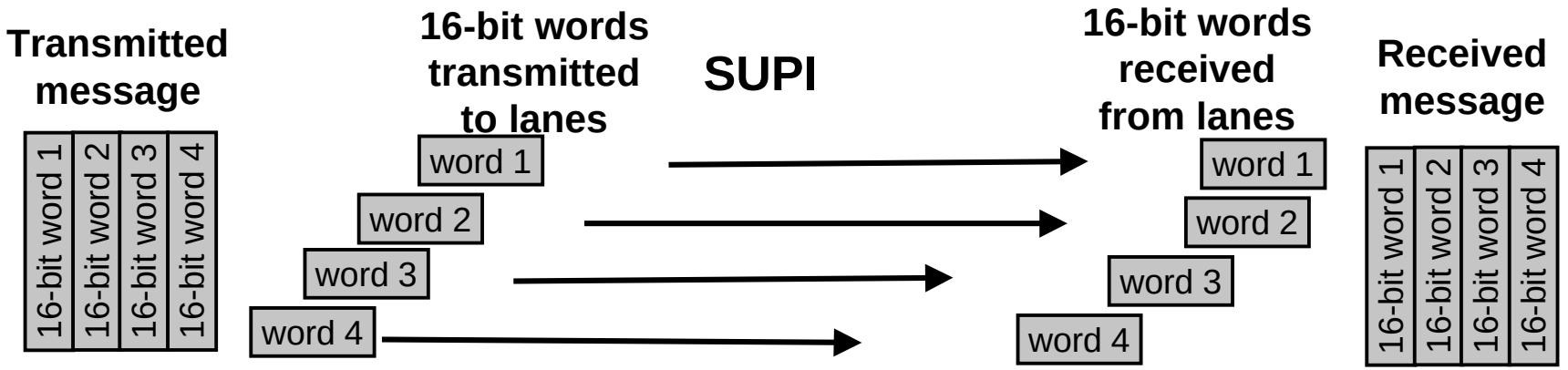
Force A1/A2s every 155520 bytes



- For LAN-PHY 48 A1 followed by 48 A2 are enough
- For WAN-PHY 192 A1s followed by 192 A2s are part of the frame structure
- For WAN-PHY 155520 octets is once every 125 usec
- A single sync algorithm can lock on either

SUPI Overview

- **4 lanes at ~2.5 Gbaud per lane**
- **16-bit word striped data transmitted on each lane**
- **Each lane has 1/4 of the A1/A2 framing bytes for lane deskew and synchronization**
- **SUPI carries any pseudo-random payload (L/HEC,64/66)**
- **Word synchronization from A1/A2 transition**
- **For fixed lane assignment skew can be large, for auto-rotation lane skew can be up to 16 bits**



SUPI Measurements

Configuration 1:

- **HP54xx scope, 20GHz RF module**
- **two 3’ RG-142 test cords**
- **450mV$_{pp}$ edge coupled 100 ohm differential**
- **backplane: 7-9-7mil stripline on Getek**
- **26” traces**
- **2.48832G SONET scrambled ($x^7 + x^6 + 1$)**
- **no de-embedding**

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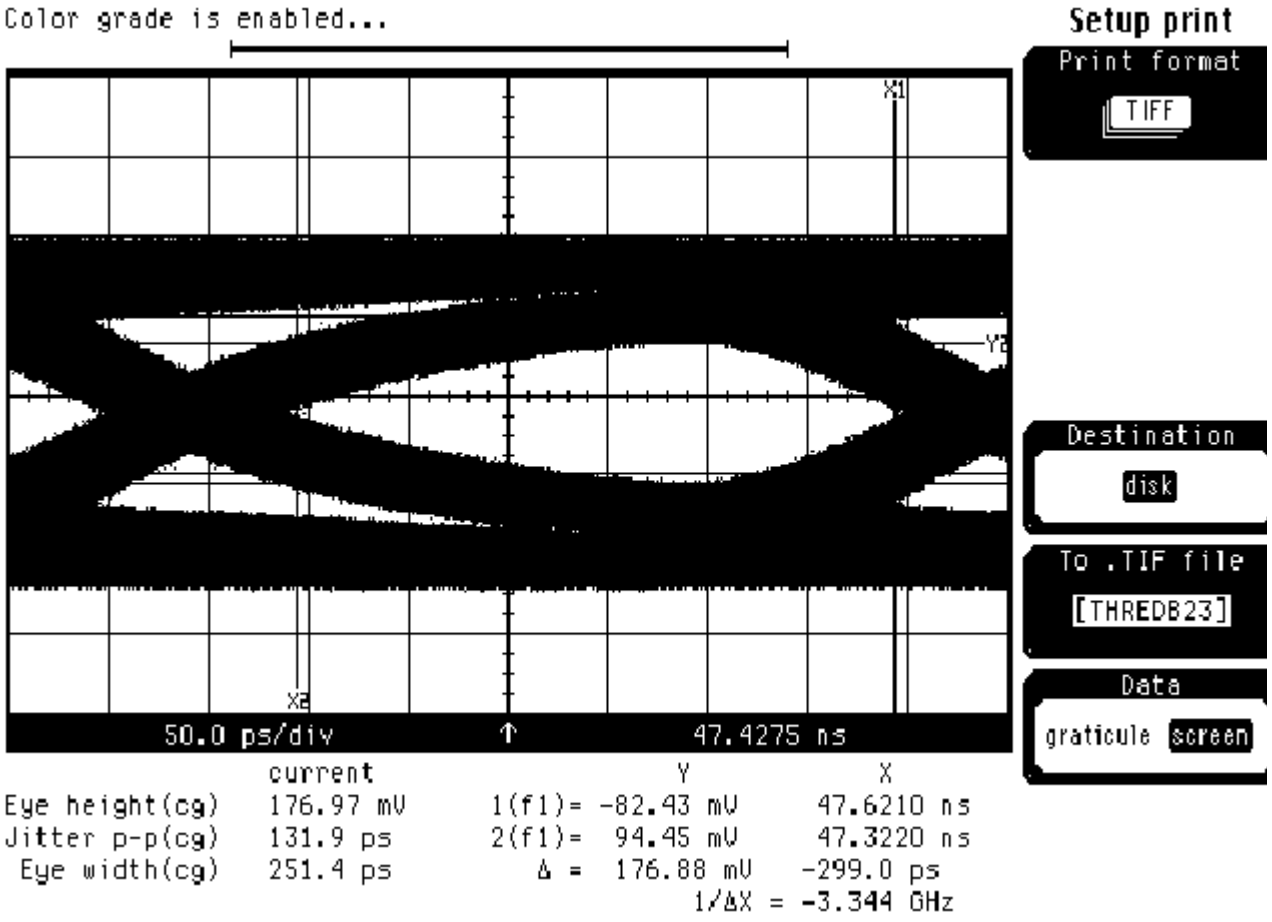
Configuration 1 Results



- **eye opening ~176mV, ~290ps (39%, 72%)**

SUPI Measurements

Configuration 2:

- **HP54xx scope, 20GHz RF module**
- **two 3’ RG-142 test cords**
- **450mV$_{pp}$ edge coupled 100 ohm differential**
- **circuit pack: 4-5-4mil stripline on Getek**
- **backplane: 7-9-7mil stripline on Getek**
- **6” - 10” - 10” traces (PCB - BP - PCB)**
- **two Teradyne VHDM pin-in-box connectors**
- **2.48832G SONET scrambled ($x^7 + x^6 + 1$)**
- **no de-embedding**

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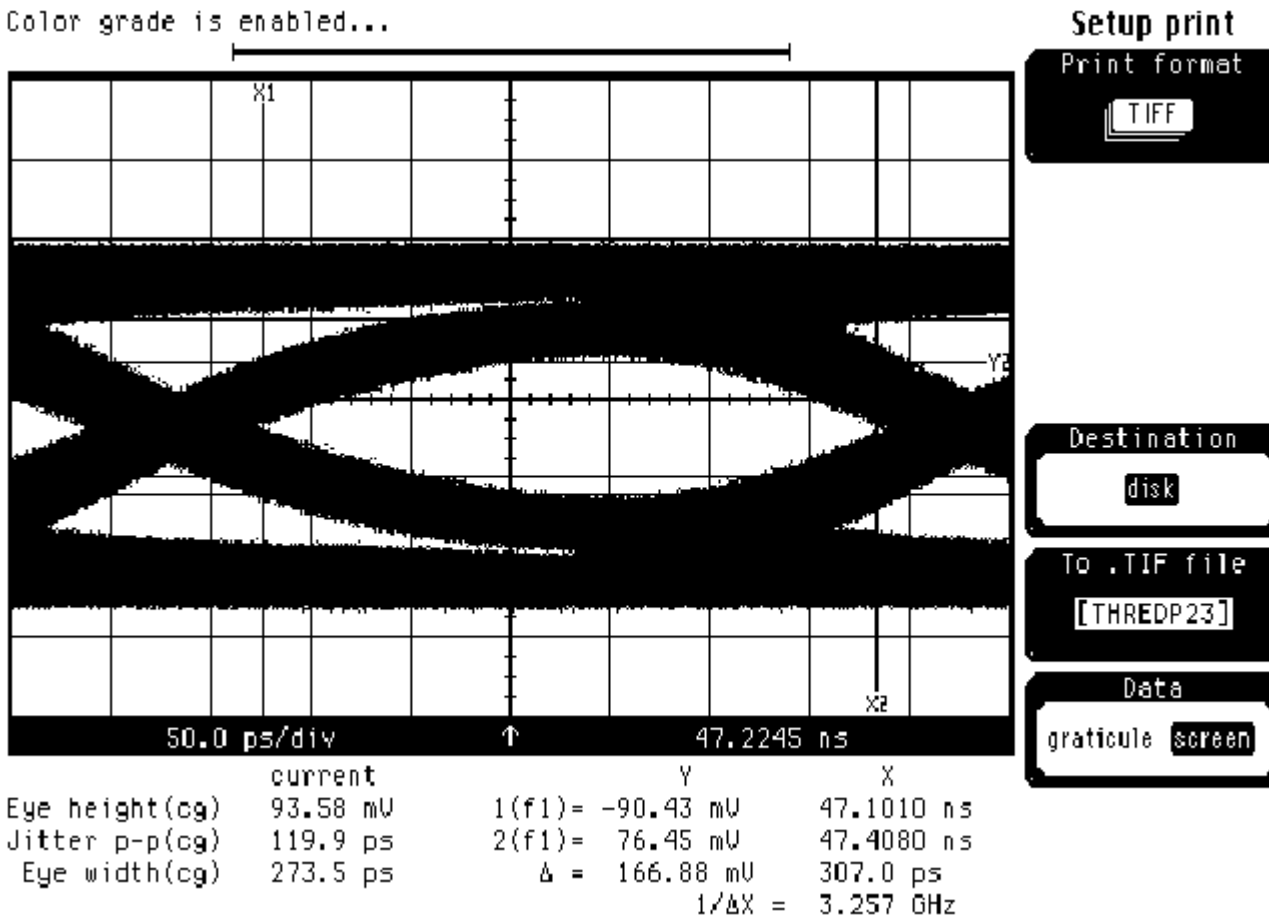
Configuration 2 Results



- **eye opening ~166mV, ~285ps (37%, 71%)**

Conclusions from Eye Diagrams

- **preliminary measurements, but encouraging**
- **negligible degradation due to connectors**
- **results for 8B/10B signal were within ~5%**

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SUPI Unifies LAN/WAN and PMDs