Hari Word Stripe Coding Issues & Status

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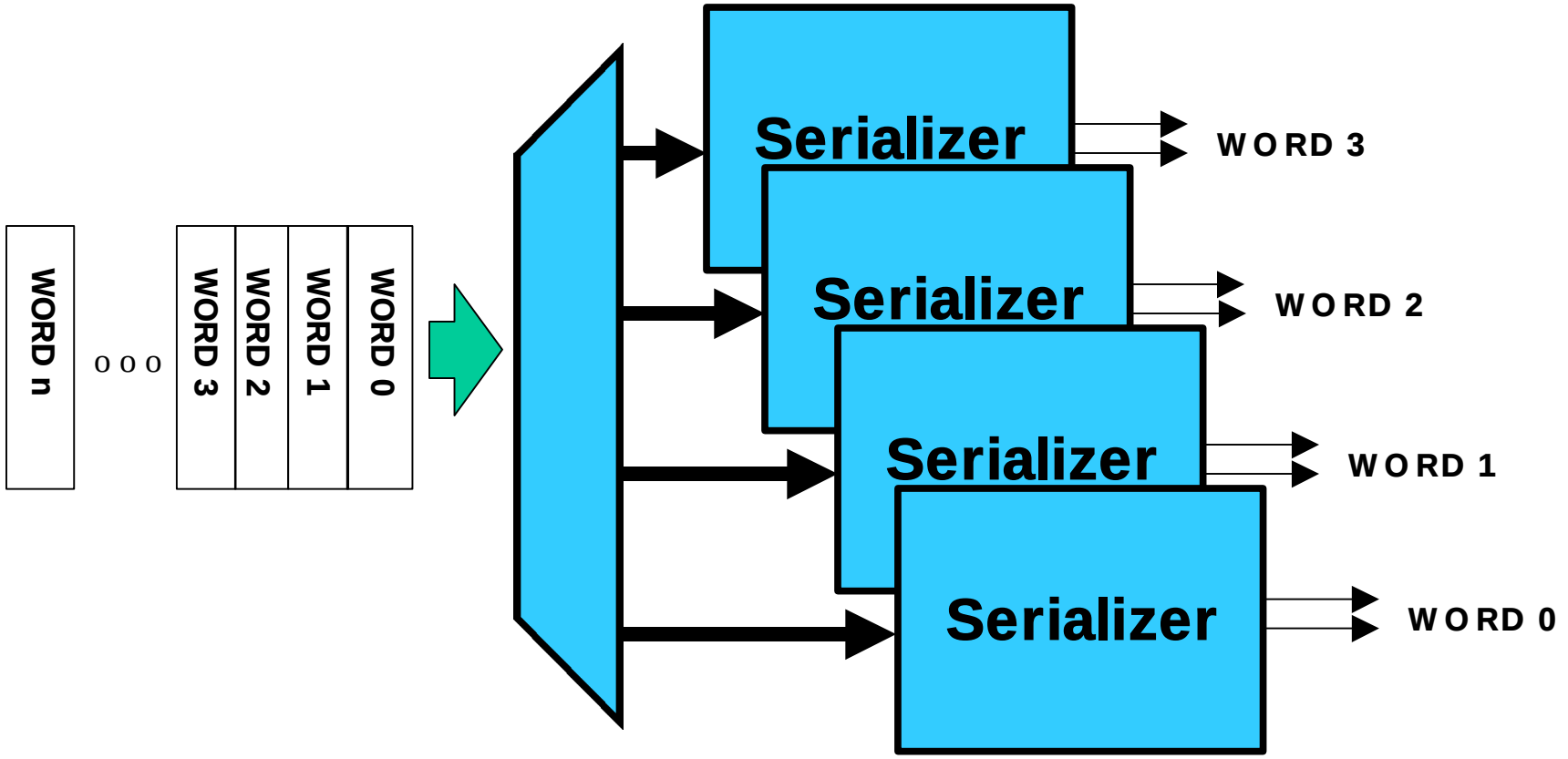
Why Word Striping instead of Byte (Column) Striping?

- *Word striping avoids need to deskew*
  - *Technical risks of byte deskew are **at least** comparable to clock-matching EFIFO design (for which several implementations suffered flaws)*
- *Word striping avoids need for high speed, byte rate (320 MHz) clocks*
- *Word striping allows more deletable characters in IPG*

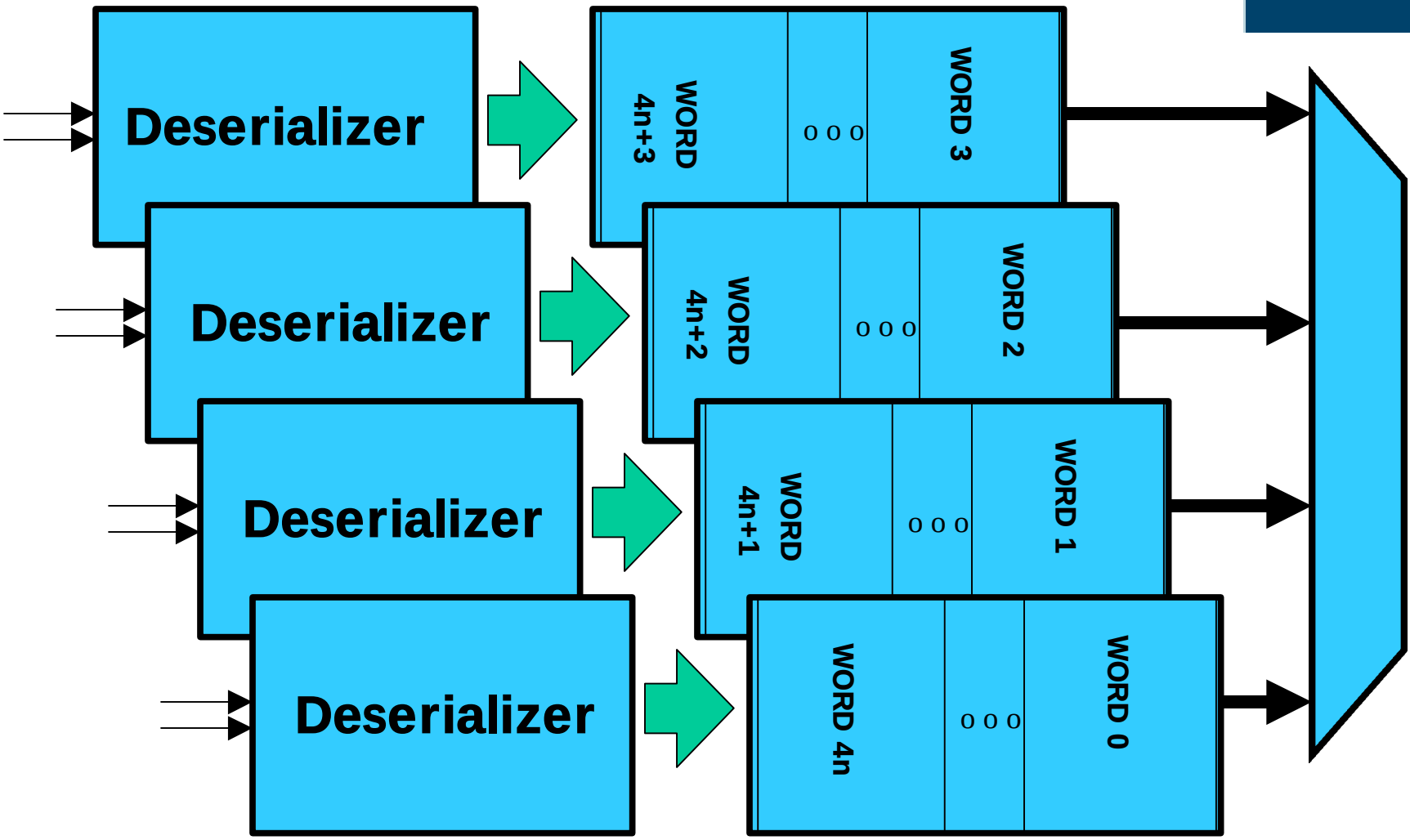
Correcting some misinformation…

- *Statement in taborek_1_0100 that "Word Striping requires commas in (WAN PHY) Preamble" is not true.*
  - *Neither striping scheme modifies packet data*
- *For either coding scheme, Hari is an "XMII extender" , so following layers (e.g., 64b/66b) are independent.*

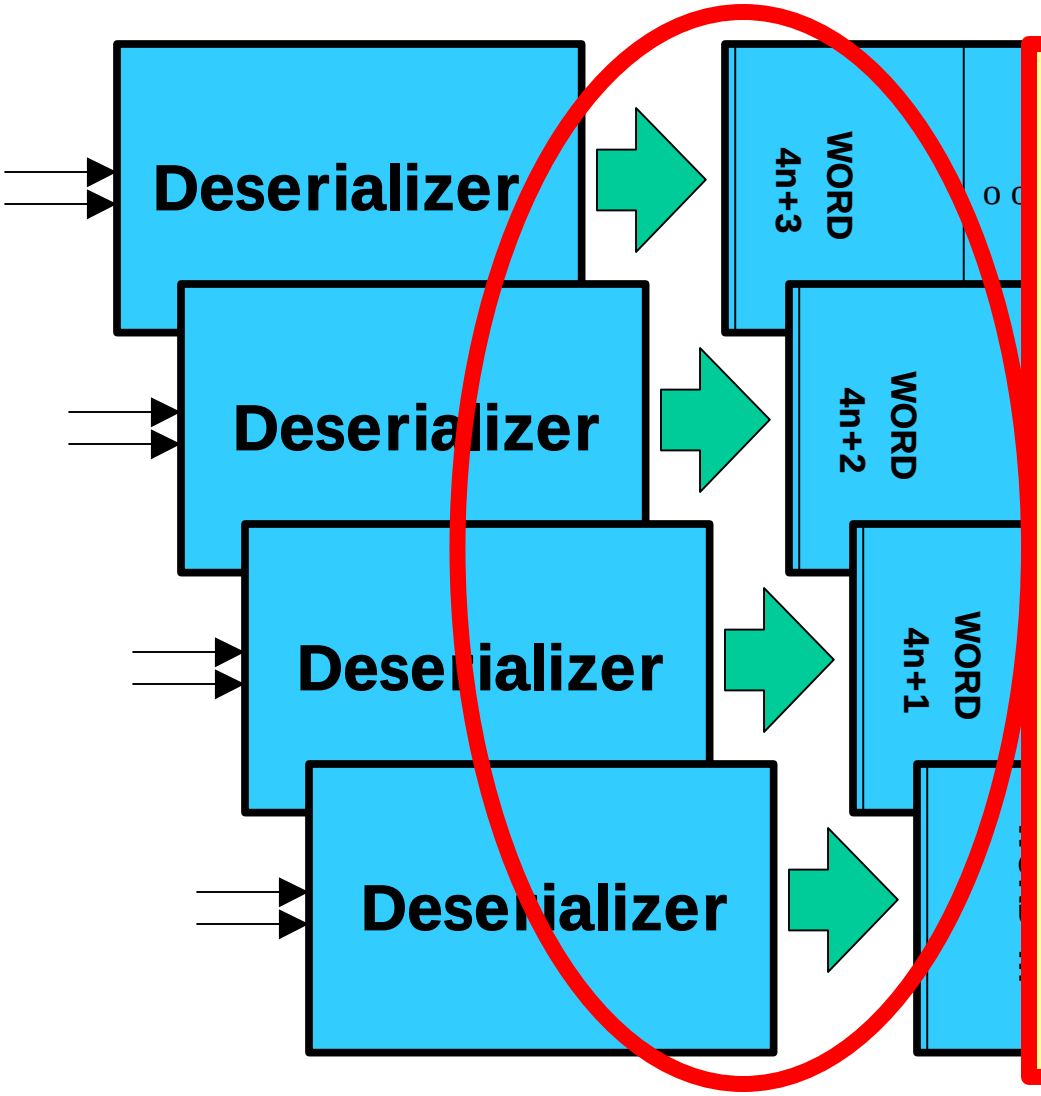
10G Architecture (Ser)



10G Architecture (Deser)



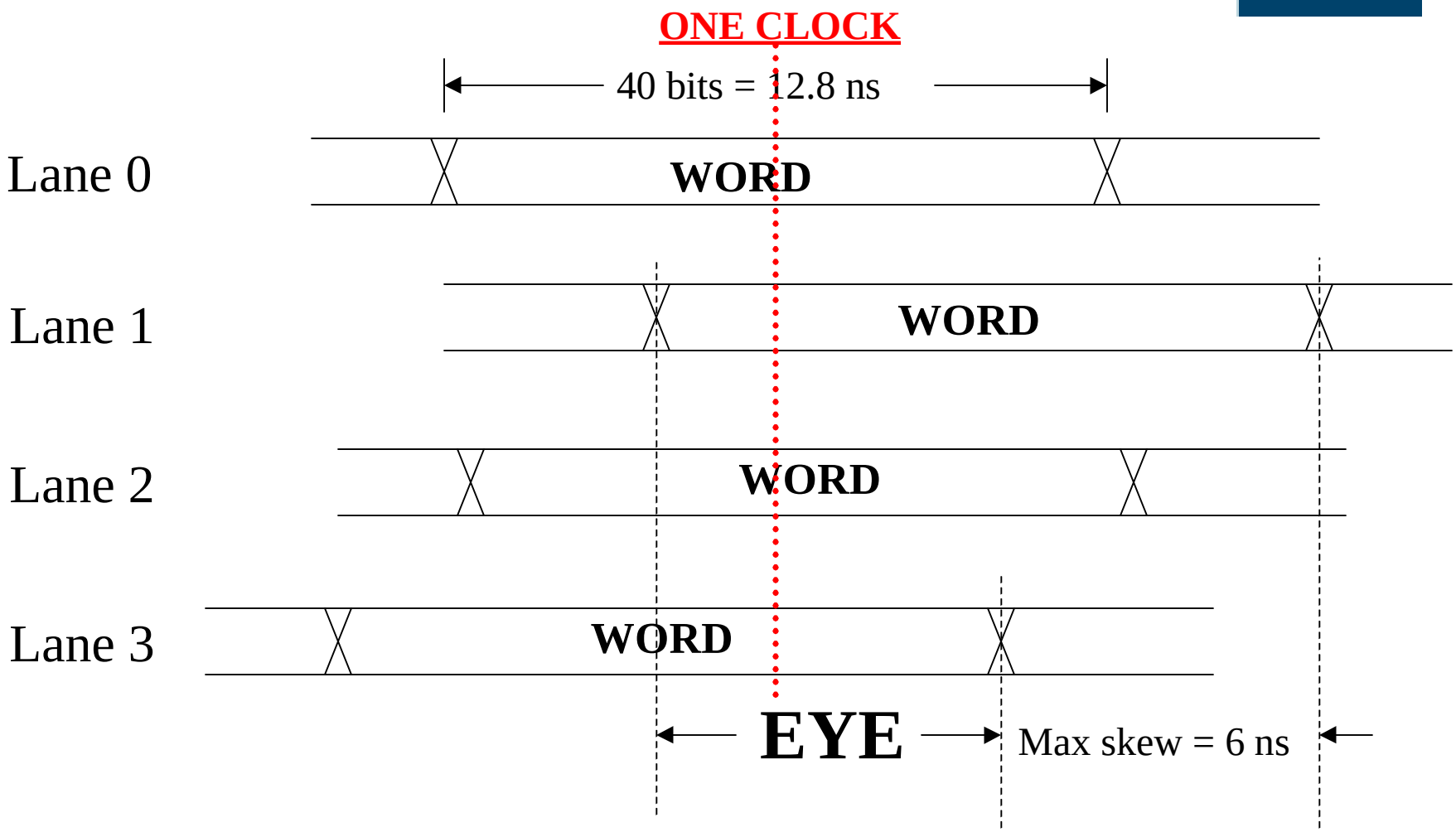
10G Architecture (Deser)



- No deskew is necessary because a word-rate clock from a single core can latch data from every deserializer into the FIFO.

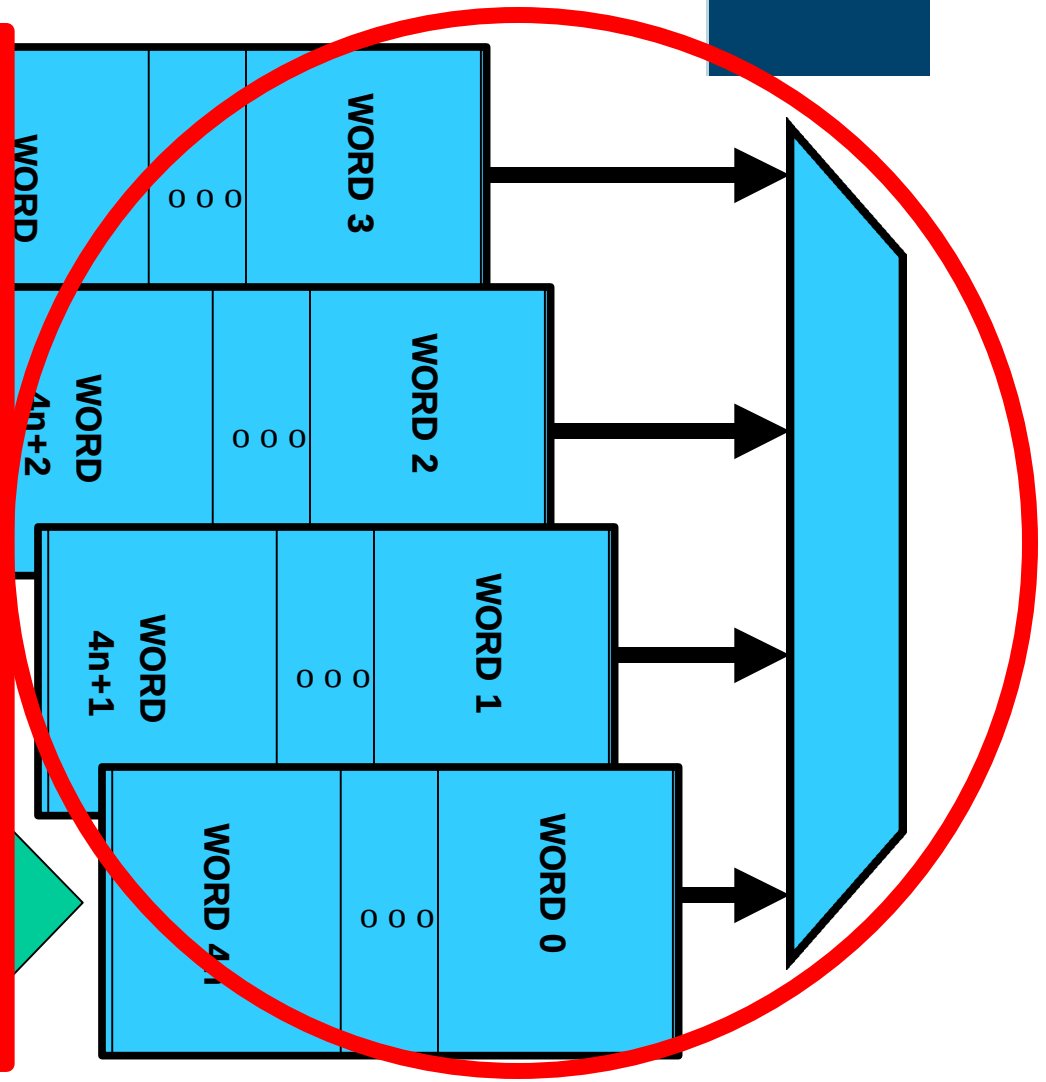
- FIFOs in each lane are loaded in correct order if this single word-rate clock (say, from lane 0) starts at recognition of defined word.

Word Striping



10G Architecture (Deser)

4 FIFOs vs. 1 FIFO is solely a matter of memory organization. That is, the four lane FIFOs can be viewed as a single FIFO, written by a single recovered clock and read by the local clock. Therefore, the exact same elasticity algorithm that was proven for 1G and 2G designs can be used for 10G designs.



Summary

- *Design work proceeding on both coding schemes (word & column striping)*
  - *Word striping extends much more directly from existing designs*
- *Recommendation: reserve judgement until thorough hardware results are available*
- *References: ritter_1_1199, jenkins_1_1199*