Analog Interface for 10-Gb/s Ethernet

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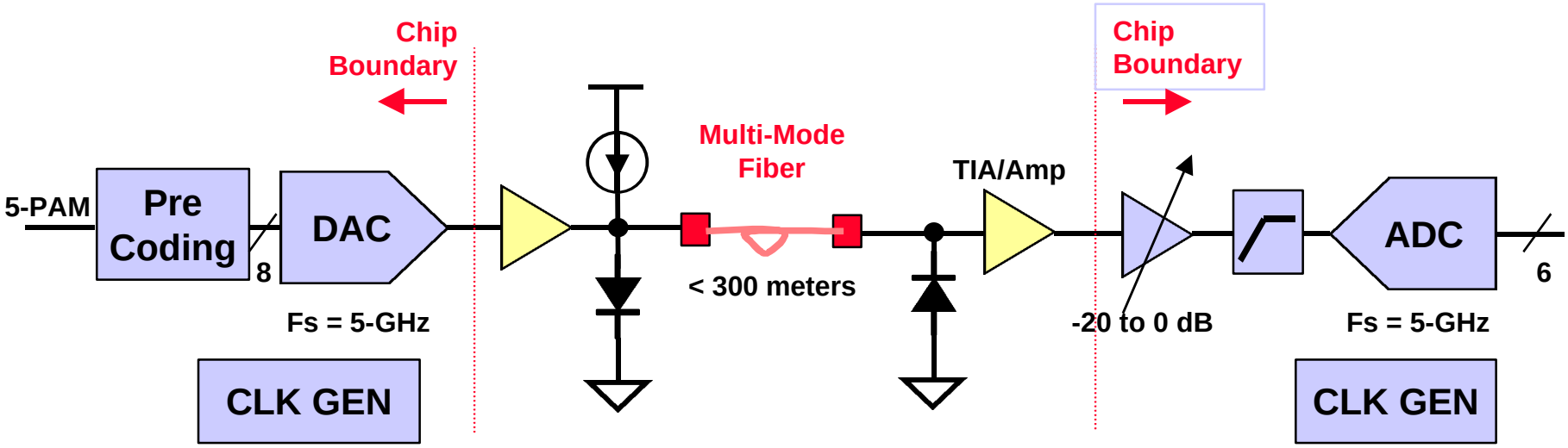
10-Gb/s Ethernet Analog Interface



- Precoding in TX requires 8-bit resolution in TX DAC
- Minimum of 6-bit ADC resolution required in RX
- RX high-pass corner @ 200-MHz
- -20 to 0 dB RX attenuator for amplitude control

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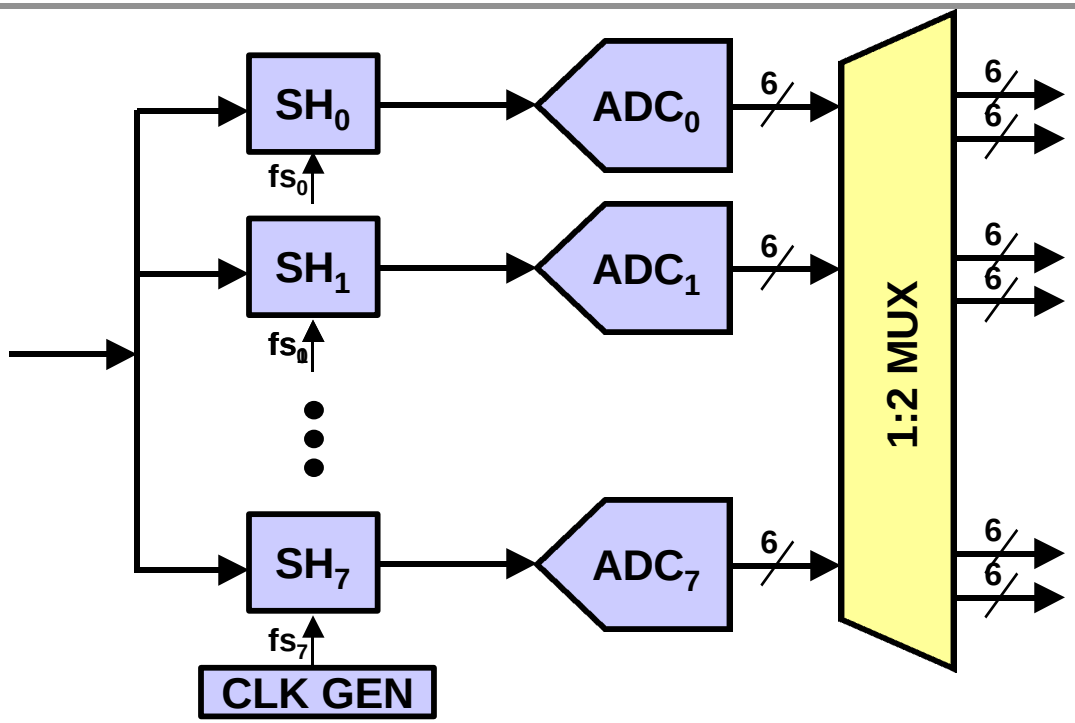
RX Using 8-Interleaved ADCs



- 8 parallel 6-bit ADCs Sampling @ 5-GHz/8 = 625-MHz
  [ISSCC2000: 6b, 800 MHz, 0.25u CMOS ADC - Matsushita]
- Sample & Hold required to eliminate jitter-induced errors (clock routing to comparators)
- Clock Generator for 8 phases timed for full-speed clock
- 1:2 Mux to Handle Digital I/O @ 312.5-MHz

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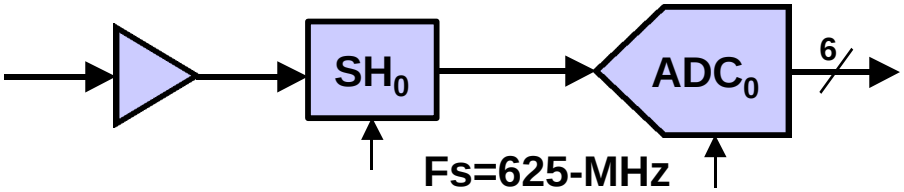
Feasability of Interleaved 625-MS/s 6-bit ADCs



• Fsample	• 625-MHz
• Resolution	• 6-bits
• Fanalog	• 0 - 2 GHz
• Vsupply	• 1.8V
• Diff Analog Input	• 1.0 Vpp Differential
• INL /DNL	• < 1.0-LSB / < 0.5-LSB
• Distortion @ 1GHz	• < -40dB
• BER	• < 10^{-15}
• Power	• 36mW @ 1.8V / slice
• Latency	• 3-4 Clock Cycles
• Clock Jitter	• < 3 ps rms

Results Based on Preliminary Simulations in 0.18mm CMOS

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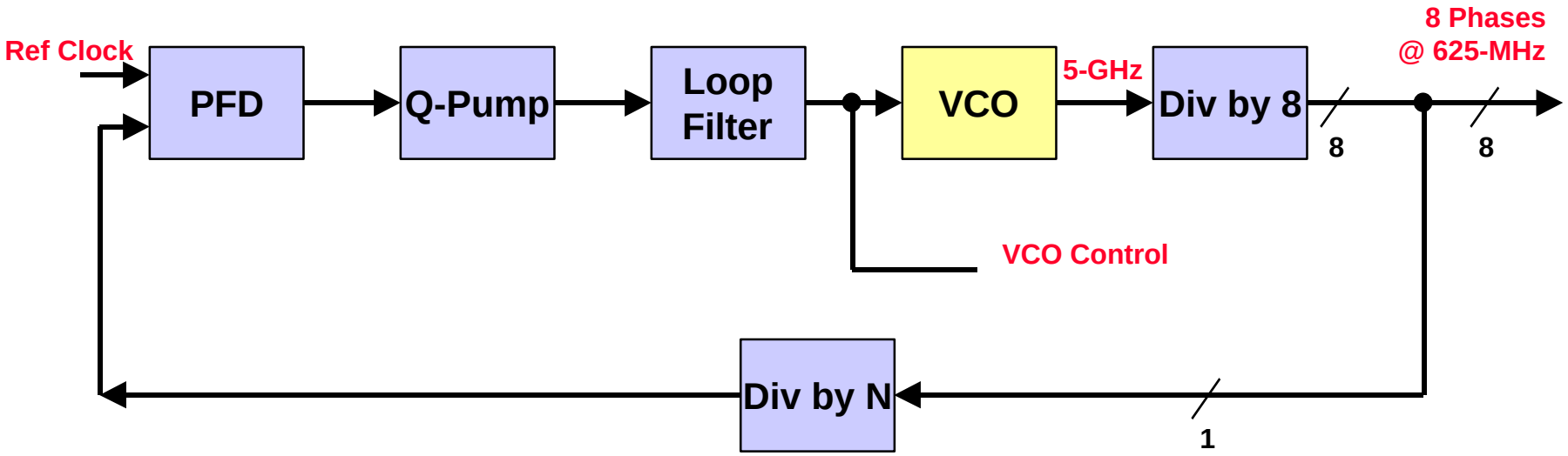
PLL Architecture with 8-phase Clocks



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3GHz PLL Jitter Measurements

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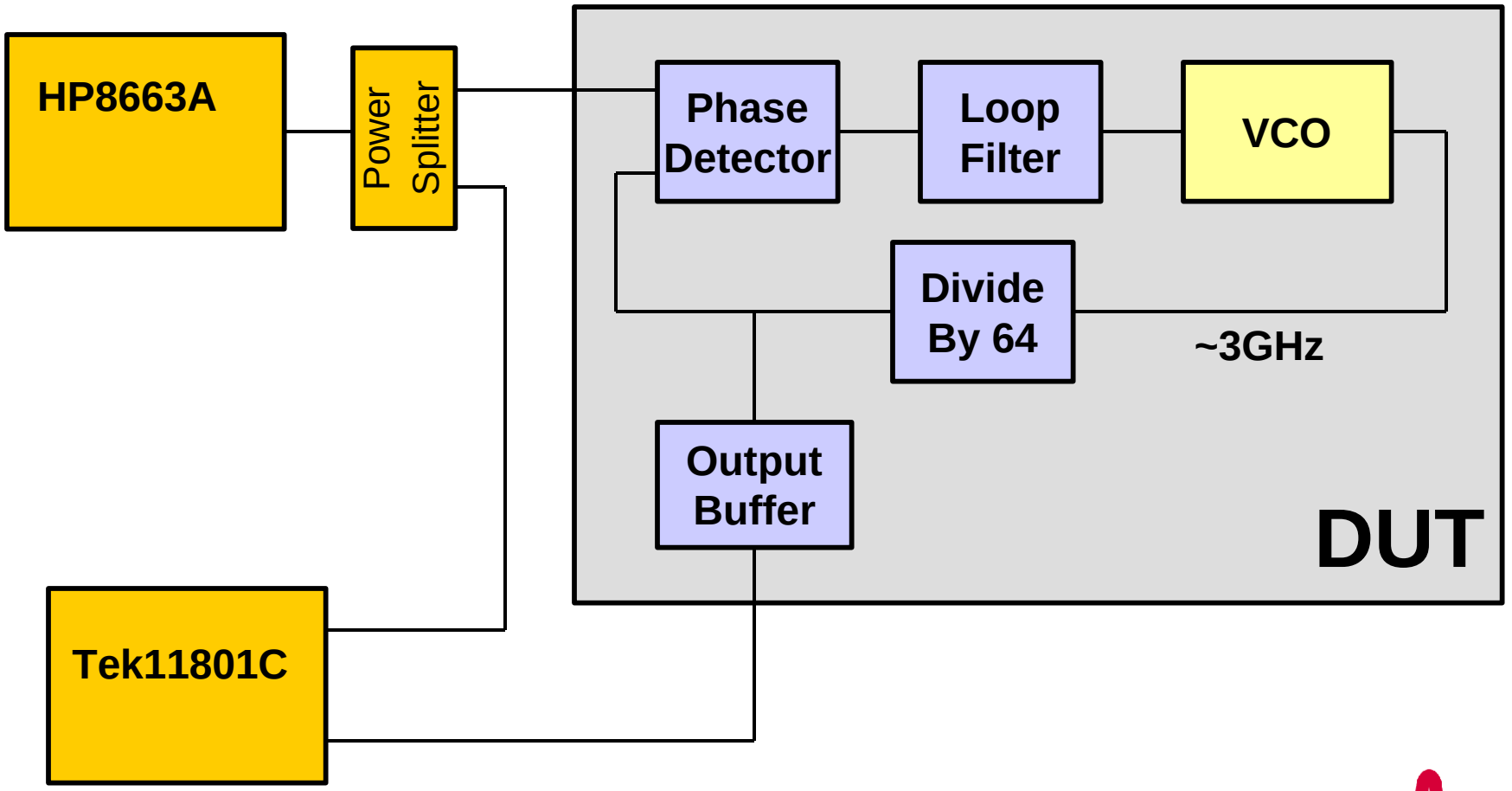
Measurement Setup



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Measured Jitter of PLL Output

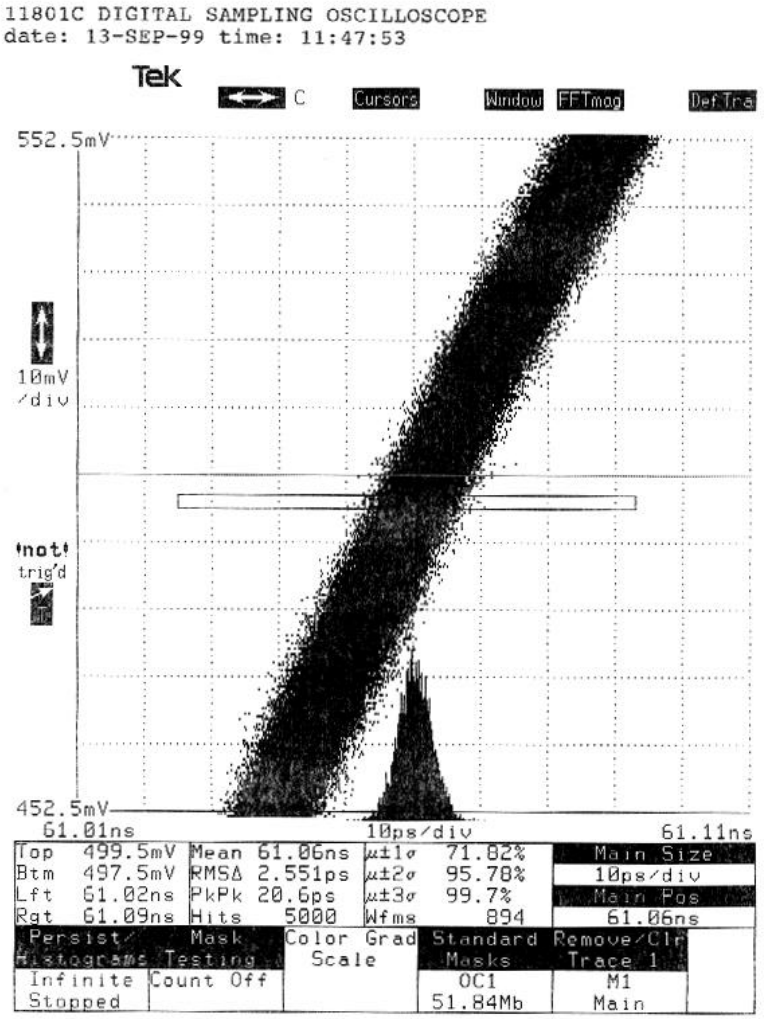
- **Divider Output**

  Trigger reference = Synthesizer

  Offset from trigger = 0µs

  Jitter = 2.551ps rms

  Note: Includes Scope Jitter



10 Gigabit Ethernet Transmitter

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10 Gigabit Ethernet Transmitter

- **Symbol rate = 5 Gbaud**
- **Symbol modulation = Pre-coded 5 PAM**
- **Output bandwidth ~ 4 GHz**
- **THD < -48dB**

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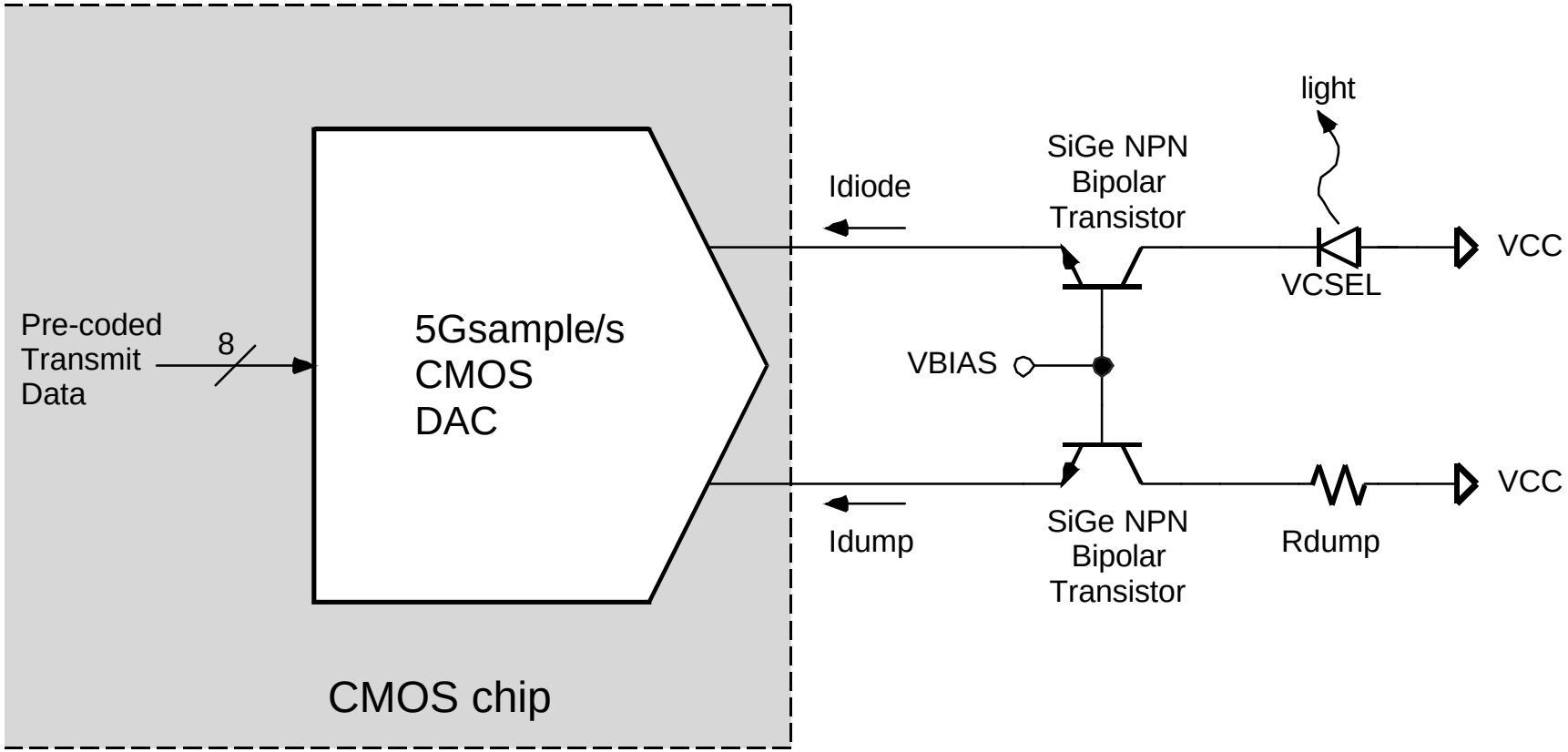
10 Gig Ethernet Line Driver Circuit



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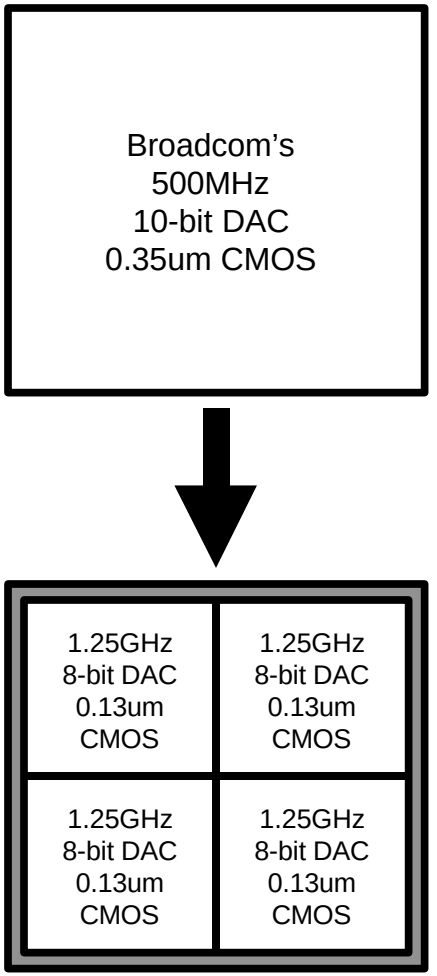
10 Gig Ethernet Transmit Components

- **Current-mode Digital-to-Analog Converter (DAC)**
  - Function - To convert pre-coded 5-PAM symbols to driver current
  - 8-bit digital input, 5Gsample/sec output
  - THD < -48dB
  - Single-ended output current = 5mA to 15mA
  - Output capacitance < 5pF
  - Implementation
    - Proven Broadcom's 500MHz 10-bit DAC in 0.35um CMOS process
    - Interleave four 1.25GHz 8-bit DAC in 0.13um CMOS process

      => Achieves 5Gsample/sec output

- **Current buffer**
  - Function - To isolate DAC's capacitive output from laser diode's series resistance
  - NPN Silicon Germanium RF Transistor (e.g., Infineon BFP620)
  - 70GHz ft SiGe process
  - Operating point
    - Idiode_DC = ~10mA
    - Input impedance < 4.0ohms
    - Input capacitance < 0.9pF
    - Output capacitance < 0.15pF

- **Vertical Cavity Surface Emitting Laser (VCSEL)**
  - Ion_max = 5mA
  - Input capacitance < 0.8pF
  - Series resistance < 30ohms



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Bandwidth Analysis Feasibility

- **DAC to Current Buffer interface**
  - DAC output capacitance including buffer < 5.9pF
  - Current buffer input impedance < 4.0 ohms
  - Bandwidth = (1 / (2 * pi * 4.5ohms * 7pF) = 6.74 GHz
- **Current Buffer to VCSEL interface**
  - Current buffer output capacitance including laser < 0.95pF
  - VCSEL series resistance < 30ohm
  - Bandwidth = (1 / (2 * pi * 30ohms * 0.95pF) = 5.58 GHz
- **Overall Output Bandwidth ~ 4 GHz**

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