

IEEE P802.3ae 10Gb/s Ethernet MDC/MDIO Proposal

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Initial Issue

- Need register access to external XGXS interfaces as well as PHY internal registers

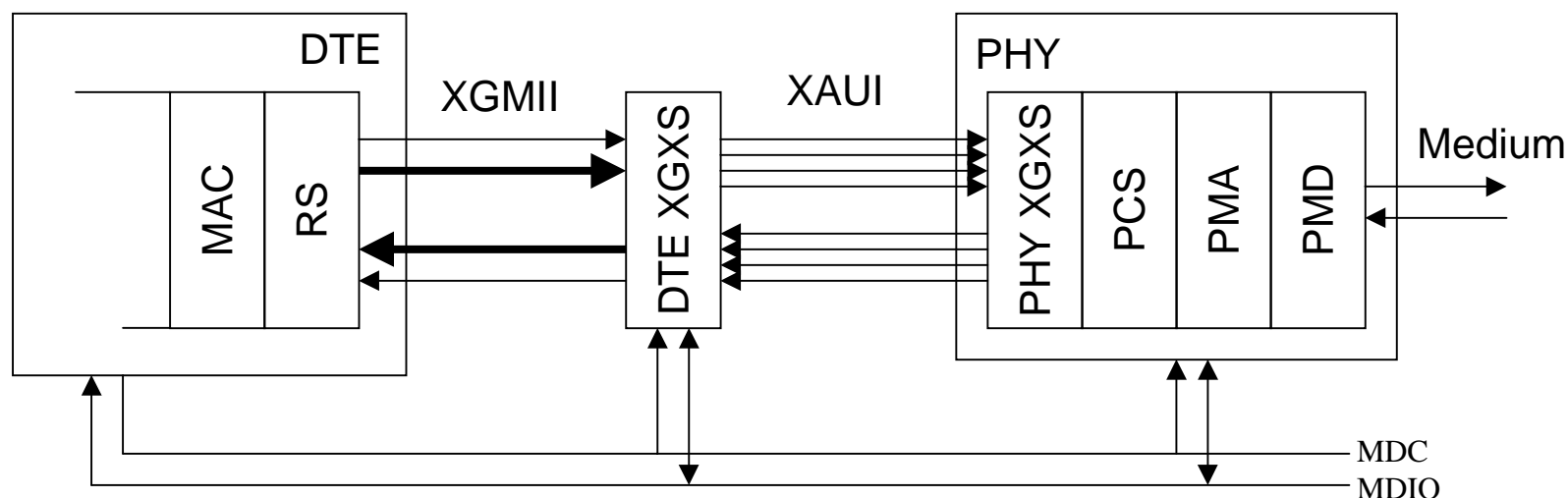


Diagram based on 'XAUI/XGXS Proposal', Rich Taborek et al, March 2000

URL: http://www.ieee802.org/3/ae/public/mar00/taborek_1_0300.pdf (Page 7)

also Brad Booth e-mail April 4th 2000 'XGMII a/k/r and XGXS - PCS Interface'

URL: http://www.ieee802.org/3/10G_study/email/msg02165.html

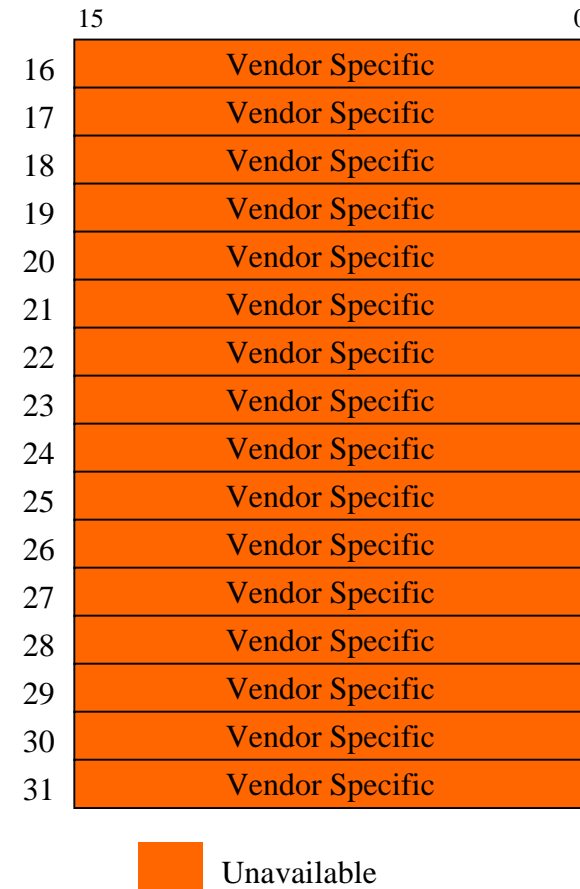
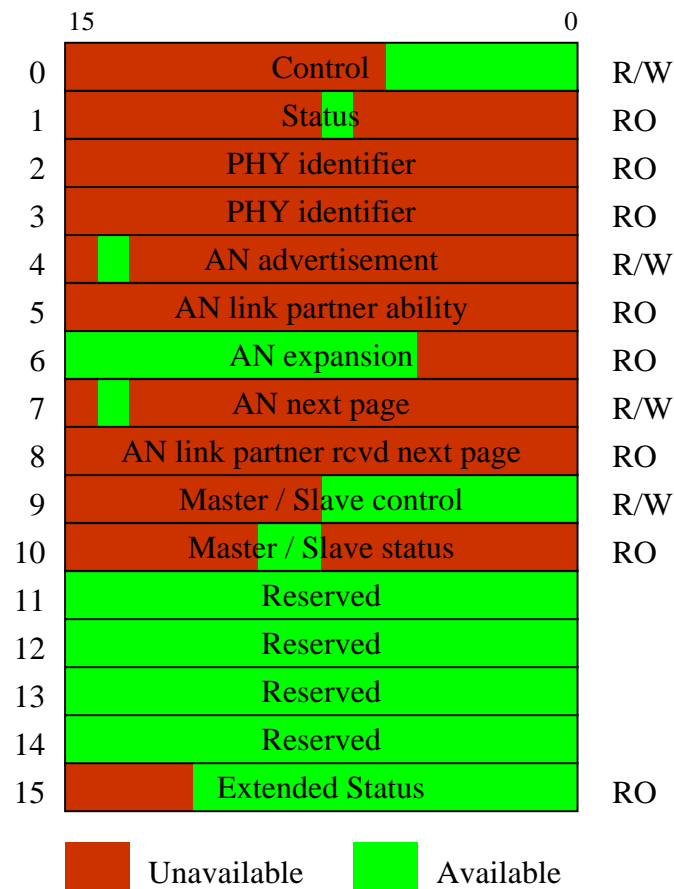
Issues

- Need to support expanded number of registers for 'PMD' use
- Other proposals may need register access
 - WIS
 - LSS
- Desire to provide larger register area for Vendor specified registers

Issues (Cont)

- Need to leave some space for the future
 - 100Gb/s ?
- Desire to support operation on same bus as existing PHY devices
- Bit and Register consumption means few Registers free in current address map

Use of existing registers



Current PMD Register Access Proposal

- New ST code proposal by Howard Frazier

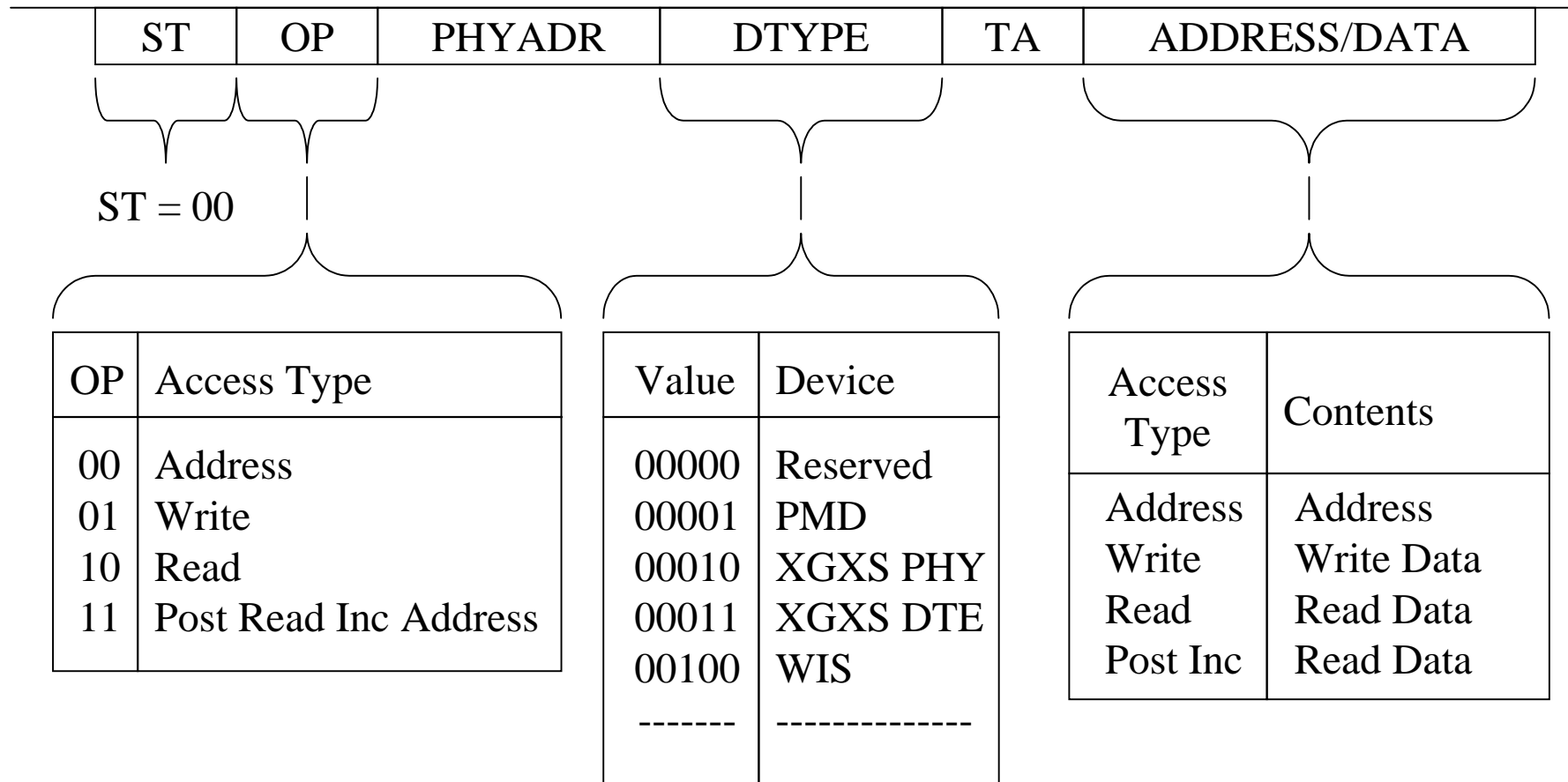
URL: http://www.ieee802.org/3/10G_study/public/sept99/frazier_3_0999.pdf

- Proposed use of the ST sequence (00) for transactions with PMD
 - Used a new ST sequence to open up a fresh set of 32 registers and allowed PHY and PMD to be defined independently
- Could be extended to provide another 64 registers by using all combinations of ST and OP codes
 - Appears not to be enough

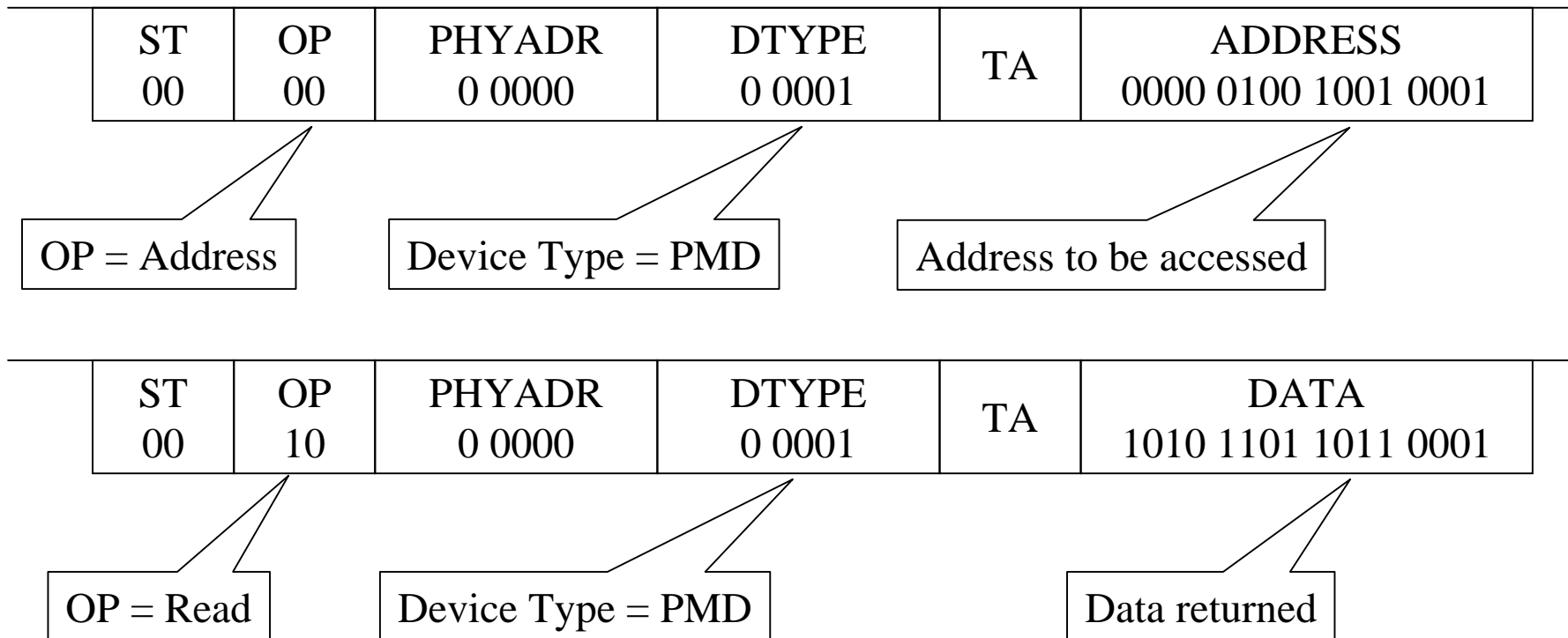
New Proposal

- Use spare ST code (00) as proposed before
 - No more ST codes available
- Define new Indirect Address register access
 - Applicable to ST code 00 only
 - Access consists of a Address cycle followed by a Read or Write cycle
- Provides many more registers
 - 32 Ports as at present
 - 32 ‘Devices’ per port
 - 65536 Registers per device

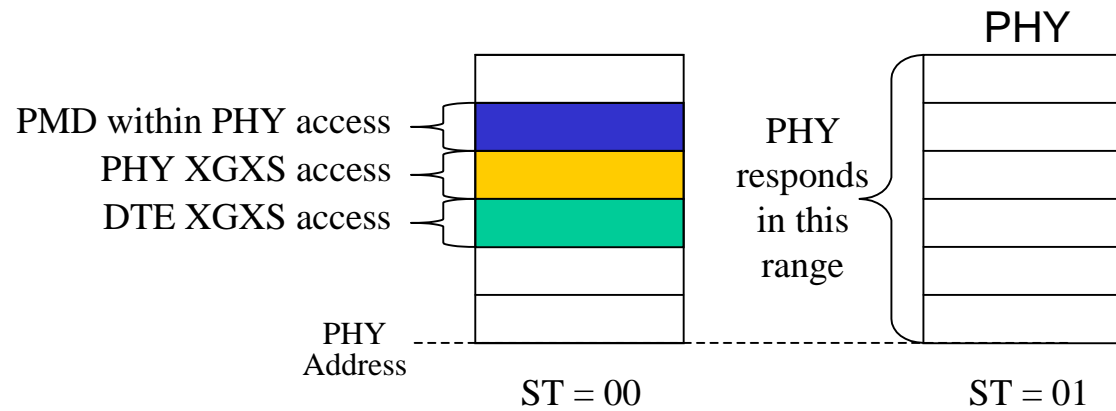
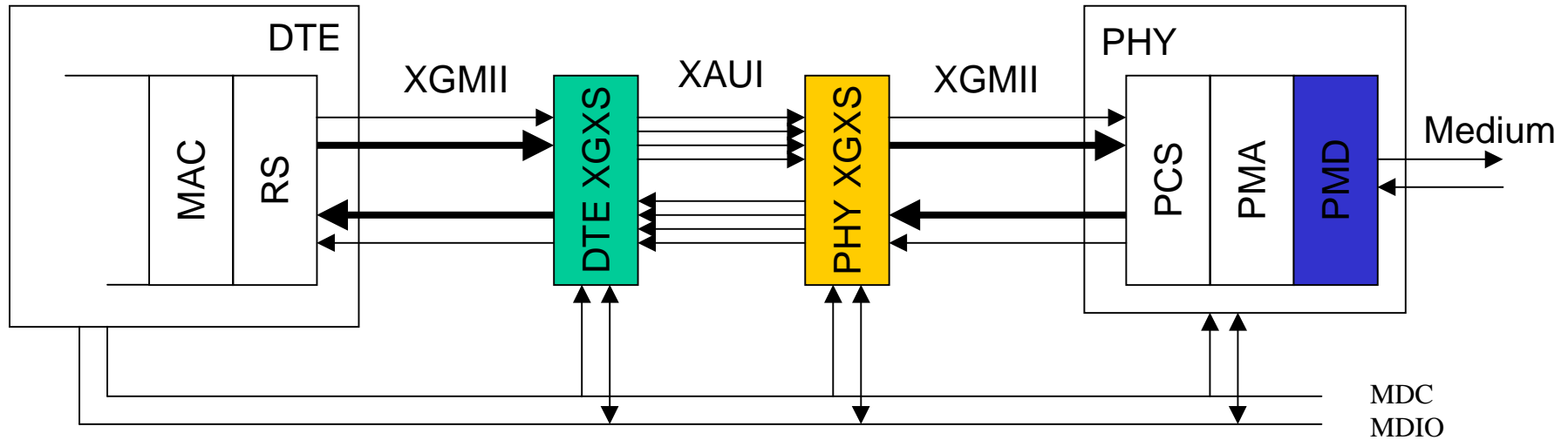
Indirect Addressing Proposal



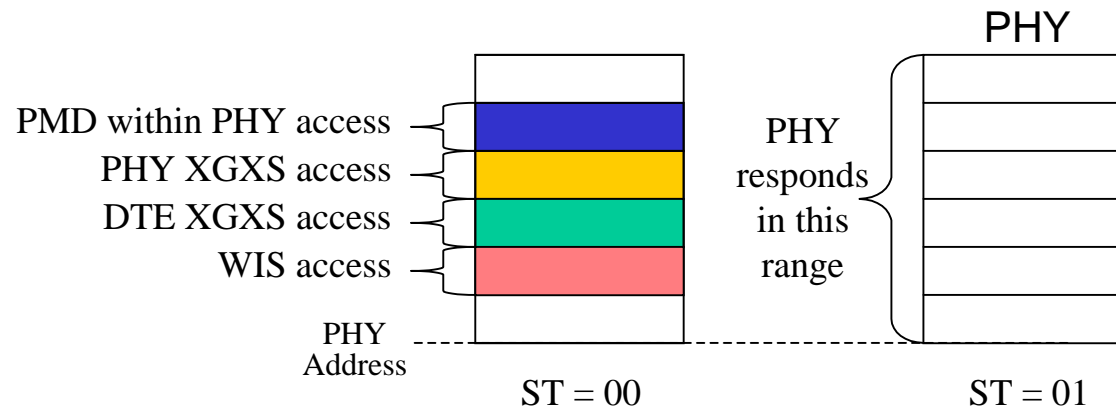
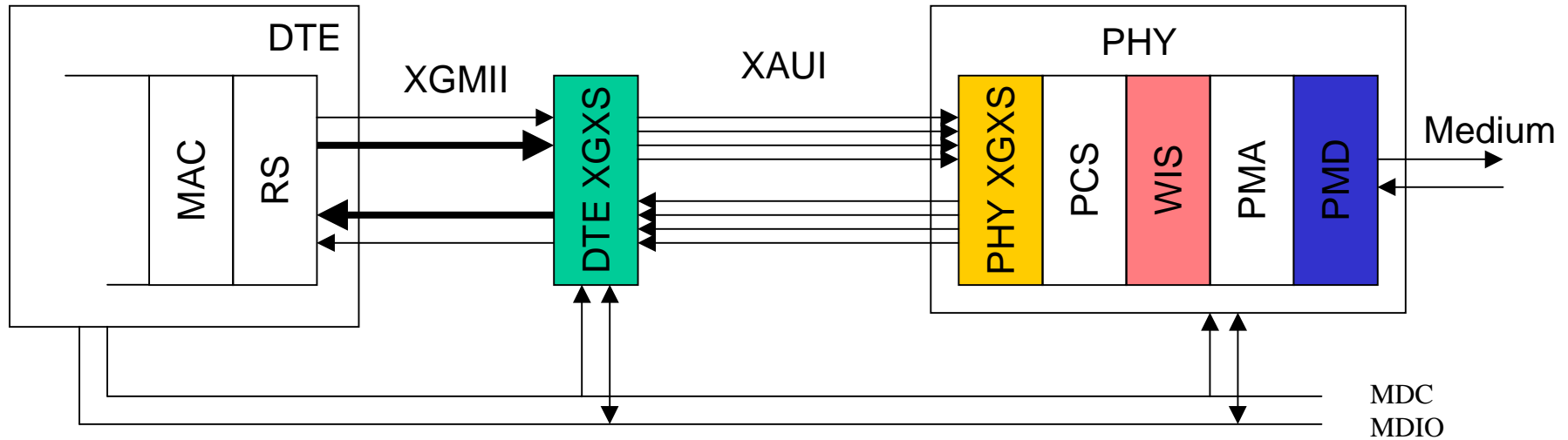
Indirect Addressing Example



LAN PHY Example



WAN PHY Example



Summary

- Define new Indirect Address register access
 - Access consists of a Address cycle followed by a Read or Write cycle
 - ‘PHY’ registers already defined access as today
- Opens up many more registers
 - 32 Ports as at present
 - 32 ‘Devices’ per port
 - 65536 Registers per device