

SONET Definition for WIS

(some nits worth picking)

IEEE 802.3ae
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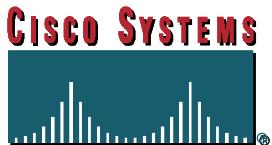


Overview

**Agree with WIS specification
proposal contained in:**

http://www.ieee.org/3/ae/public/may2000/bottorff_1_0500.pdf

Need to consider three issues



Issues for Consideration

- **Clock tolerance**
- **Overhead definition**
- **Jitter**

Clock Tolerance

- **Currently available SONET reference oscillators have +/- 20 ppm tolerance**
- **Cost difference between +/- 20 ppm and +/- 100 ppm oscillators is a tiny fraction of the total cost of a 10 GigE interface**
- **+/- 20 ppm ensures compatibility with all installed SONET regenerators and transponders**

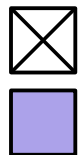
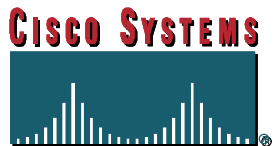
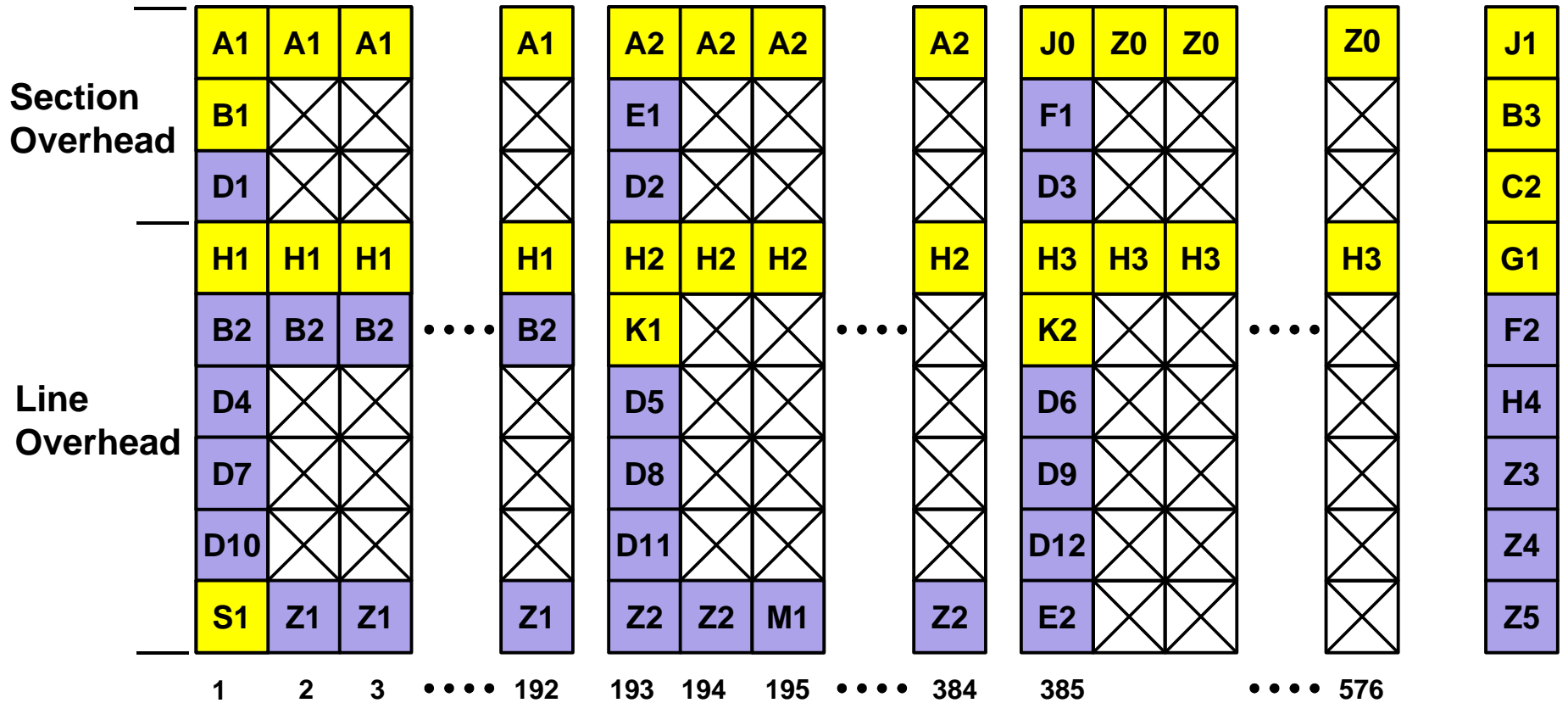
Clock Tolerance

- **Using +/-100 ppm clock tolerance in WAN PHY may require pointer processing in the transponder**
 - **added cost and complexity**
 - **incompatibility with the installed base**
- **Recommend +/- 20 ppm clock tolerance rather than +/-100 ppm**

OC-192c WIS - Overhead

From Bottorff, et al

Path Overhead



Undefined bytes (set to zero)

Defined but not used (set to zero)

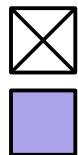
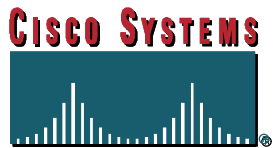
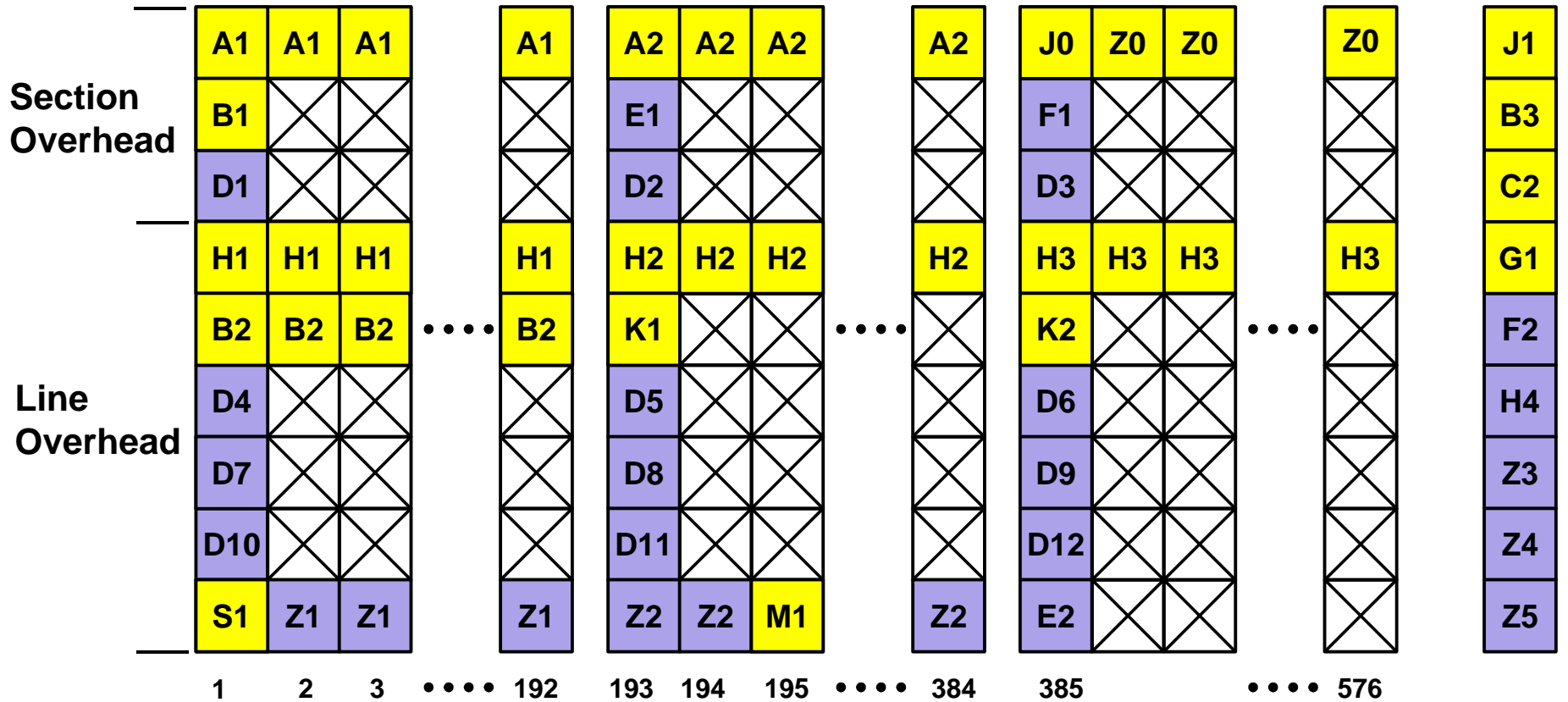


Defined and used by WIS

OC-192c WIS - Overhead

Our Recommendation

Path Overhead



Undefined bytes (set to zero)

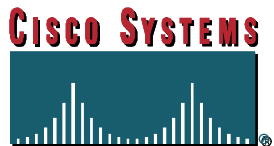
Defined but not used (set to zero)



Defined and used by WIS

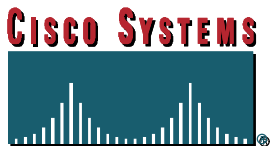
B2

- **B1 - Bit Interleaved Parity is a single 8 bit value which is used to measure bit error rate**
- **At OC-192, B1 saturates so quickly that you cannot distinguish between BERs higher than 10^{-7}**
- **B1 is useful for fault isolation, but not for performance monitoring**



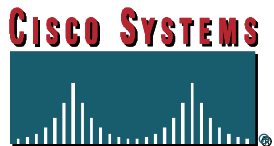
B2

- **B2 is calculated per STS-1**
- **Since there is a separate B2 for each STS-1, there is a constant ratio of parity bits to data bits, regardless of the line rate**
- **The saturation point is constant at 10^{-4}**
- **Therefore, B2 is useful for performance monitoring**



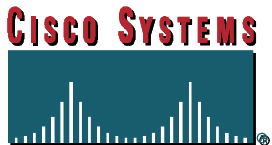
B2

- **Need to support B2 to maintain**
 - **Compatibility with other OC-192 interfaces (i.e. TDM, POS, etc)**
 - **Familiarity and consistency for crafts persons**
 - **Compatibility with existing test equipment**



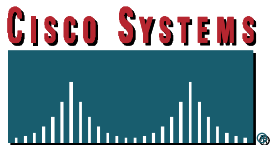
B2

- **Cost of supporting B2 entails:**
 - **192 8 bit registers in TX and RX**
 - **8 bit parity checker/generator can be shared across all 192 STS-1s**
 - **Also need a 32 bit accumulating counter in RX to report statistic to management system**



M1

- **M1 provides remote error monitoring**
- **Reflects remote value of B2**
- **Cost of supporting M1 entails:**
 - **One 8 bit register in RX**
- **Provides same compatibility benefits**



K1/K2

K1 and K2 are used on the protection line for automatic protection switching signaling.

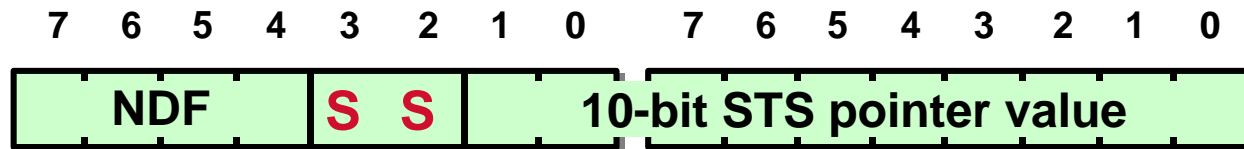
Recommend providing management (software) access to K1 and K2 to allow implementation of APS

Cost: Two eight bit registers

H1 Pointer SONET/SDH Compatibility

Need the ability to provision the **SS** bits in H1 for compatibility with SONET and SDH

SONET H1 = 0110**00**10 and H2 = 00001010
SDH H1 = 0110**10**10 and H2 = 00001010



NDF (new data flag) field

Jitter Requirements

- **What are the jitter specs for the UniPHY ?**
- **We could adopt the SONET jitter specs**
 - May add considerable cost to the interface
- **We could use the LAN PHY jitter specs**
 - May require jitter reduction FIFO in transponder
- **Recommend using LAN PHY jitter specs**

Summary

- **We need a SONET compatible UniPHY**
- **We need to specify the minimal subset of SONET functionality to reduce cost**
- **We need to maintain compatibility with**
 - **Installed OC-192 infrastructure**
 - **Existing component specifications**
 - **Existing test equipment**
 - **Existing installation and maintenance practice**

