Wide/Coarse WDM LAN PCS/PMA

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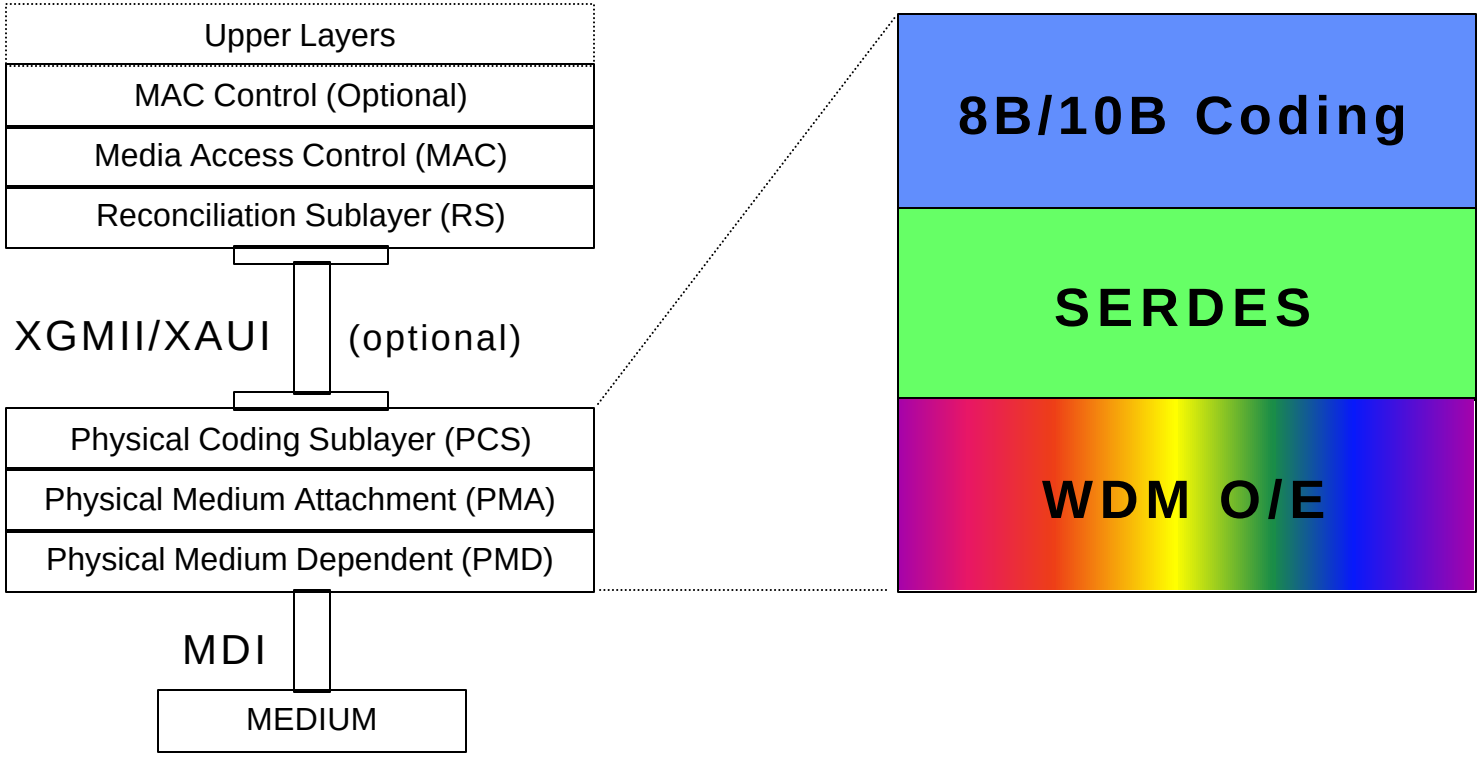
Presentation Purpose

- Illustrate WDM* LAN PCS/PMA
  - Architecture/Layer Model
  - Possible Implementations
- Distinguish XAUI/XGXS and WDM PCS/PMA
- Illustrate WDM LAN ➔ WAN via L1 Bridge

* Represents both WWDM and CWDM in this presentation

WDM Layer Model

10 Gigabit Ethernet Reference Model



WDM LAN PCS/PMA

- Based on XAUI/XGXS CODEC, SerDes & Electrical

  See http://grouper.ieee.org/groups/802/3/ae/public/may00/taborek_2_0500.pdf

  – 8B/10B based PCS
  – PCS maps directly to/from RS/XGMII/XGXS words
  – Robust packet delimiters and error control
  – Fast 7-bit unique pattern lane synchronization
  – Low-EMI Idle pattern adequate for link initialization

    See http://grouper.ieee.org/groups/802/3/ae/public/may00/taborek_1_0500.pdf
  – Lane deskew capability for longest WDM links
  – 4 lane serial, CDR-based, jitter attenuating, self-timed PMA
  – 3.125 Gbaud line rate per lane
  – May be implemented in CMOS, BiCMOS, SiGe
  – Low pin count, low power PMD interface
  – XAUI electrical basis for PMD electrical interface

Data Mapping Example

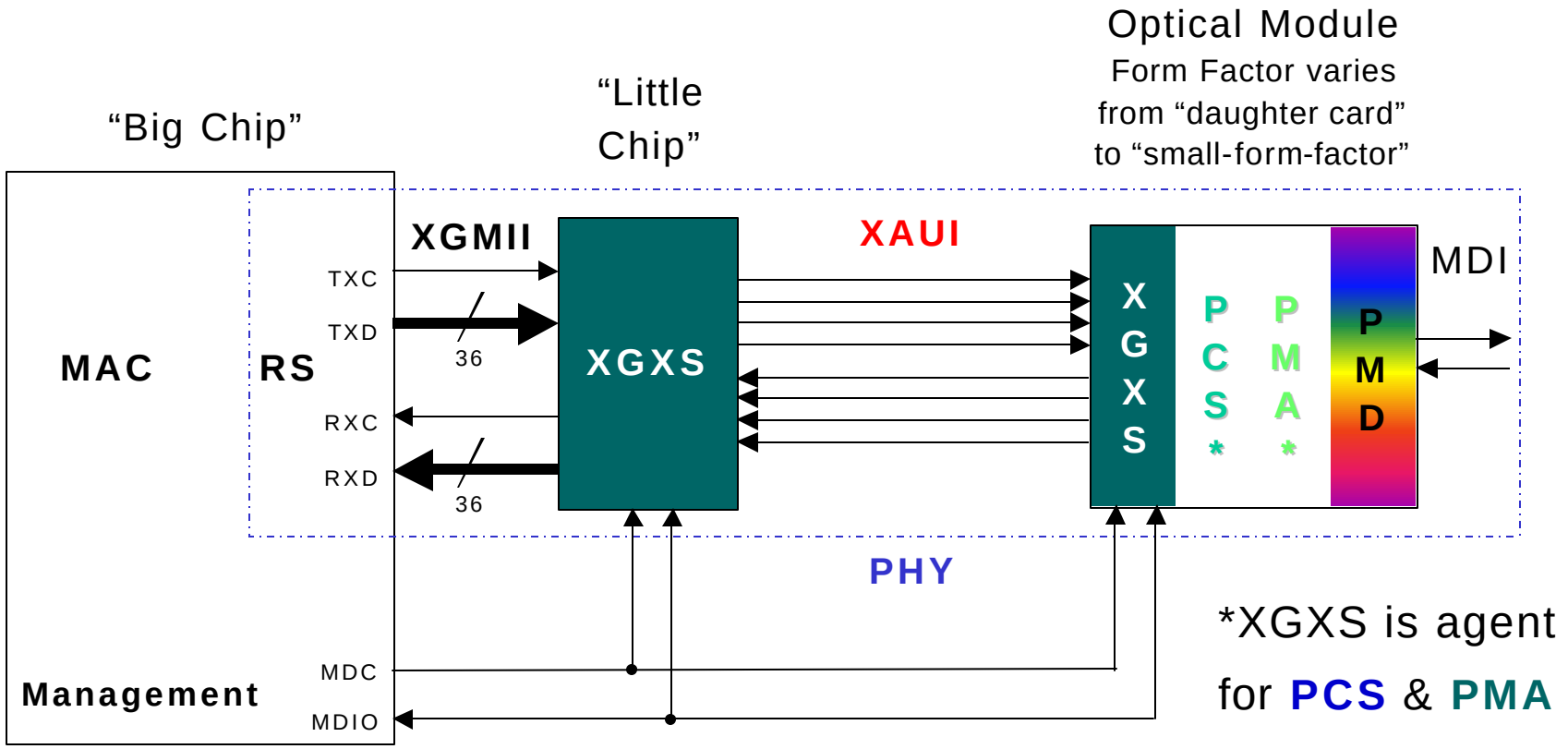
RS/XGMII Encoded Data

D<7:0,K0>	I	I	S	d_p	d	d	---	d	d	d	d_f	I	I	I	I
D<15:8,K1>	I	I	d_p	d_p	d	d	---	d	d	d_f	T	I	I	I	I
D<23:16,K2>	I	I	d_p	d_p	d	d	---	d	d	d_f	I	I	I	I	I
D<31:24,K3>	I	I	d_p	d_p	d	d	---	d	d	d_f	I	I	I	I	I

PCS Encoded Data

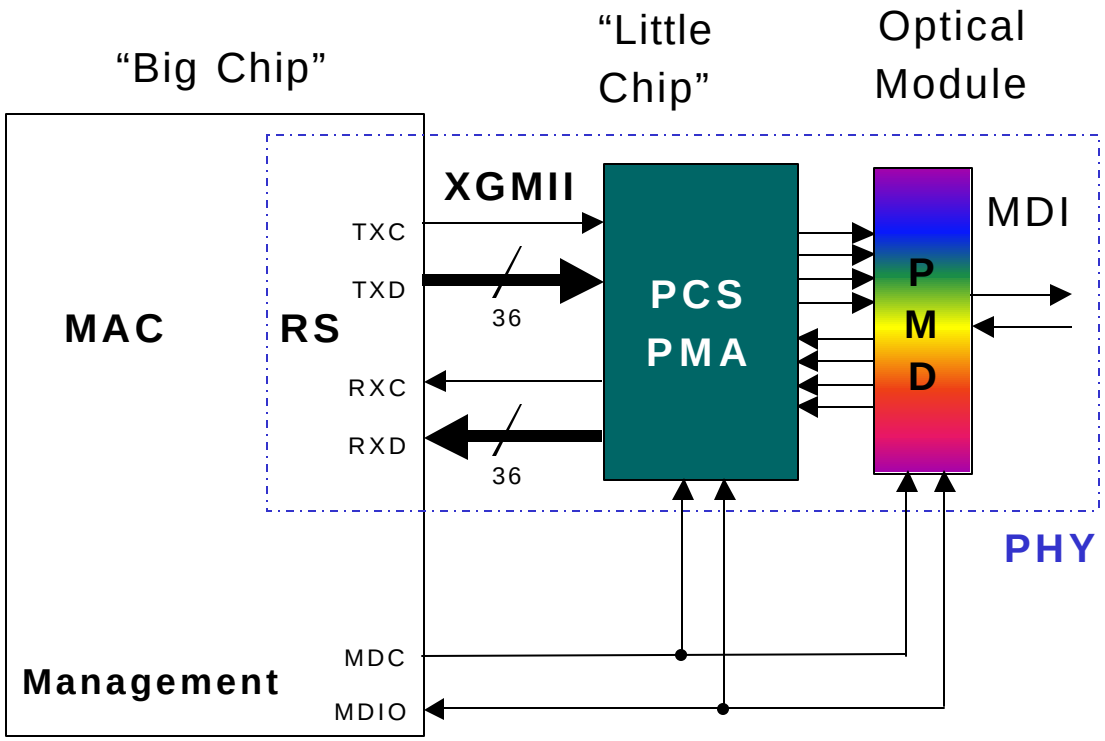
Lane 0	K	R	S	d_p	d	d	---	d	d	d	d_f	A	K	R	K
Lane 1	K	R	d_p	d_p	d	d	---	d	d	d_f	T	A	K	R	K
Lane 2	K	R	d_p	d_p	d	d	---	d	d	d_f	K	A	K	R	K
Lane 3	K	R	d_p	d_p	d	d	---	d	d	d_f	K	A	K	R	K

Complex Implementation



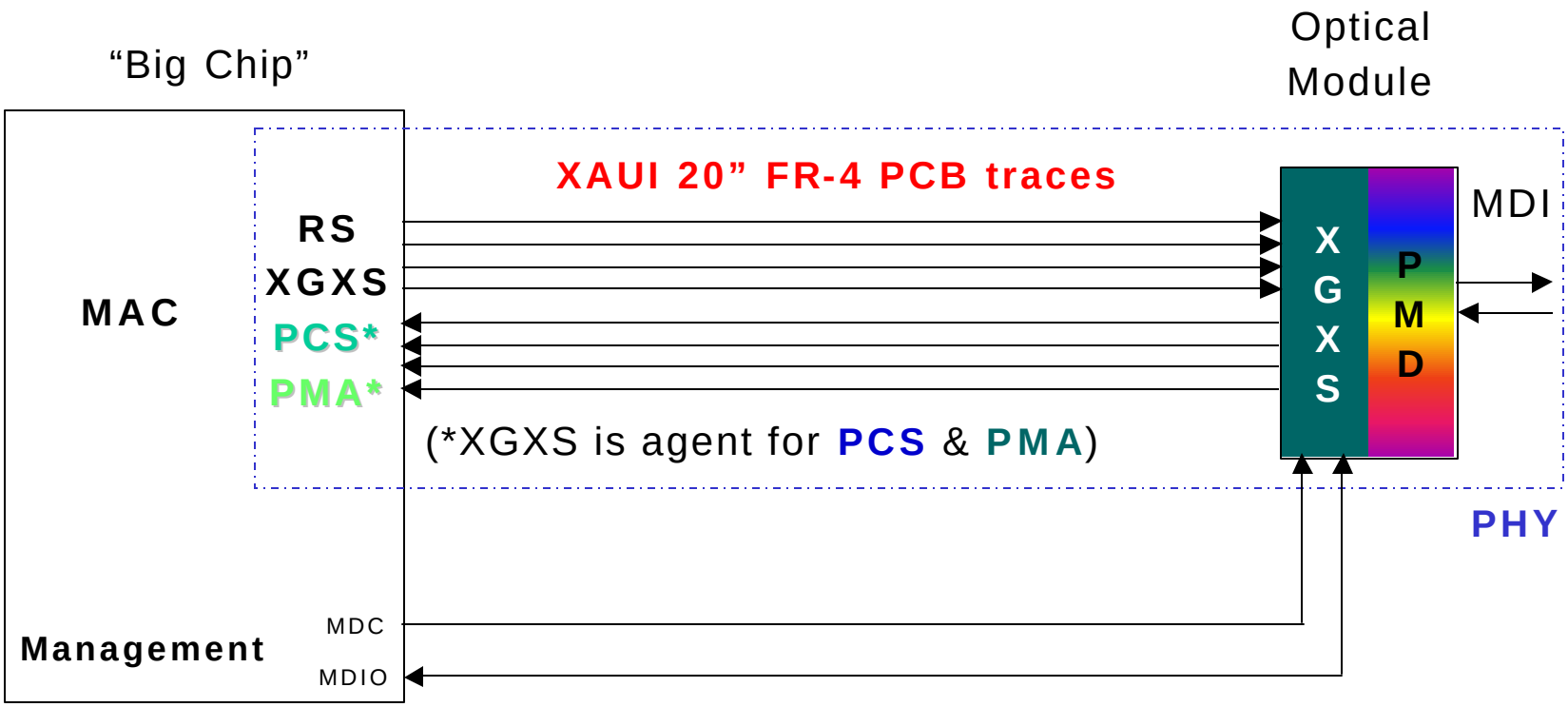
E.g. All the interfaces are implemented: 3” XGMII, 20” XAUI on 2 cards + backplane, Retimer/Repeater In Optical Module to attenuate jitter

Simple Implementation #1



E.g. NIC implementing short XGMII, no XAUI/XGXS, very short interface to PMD

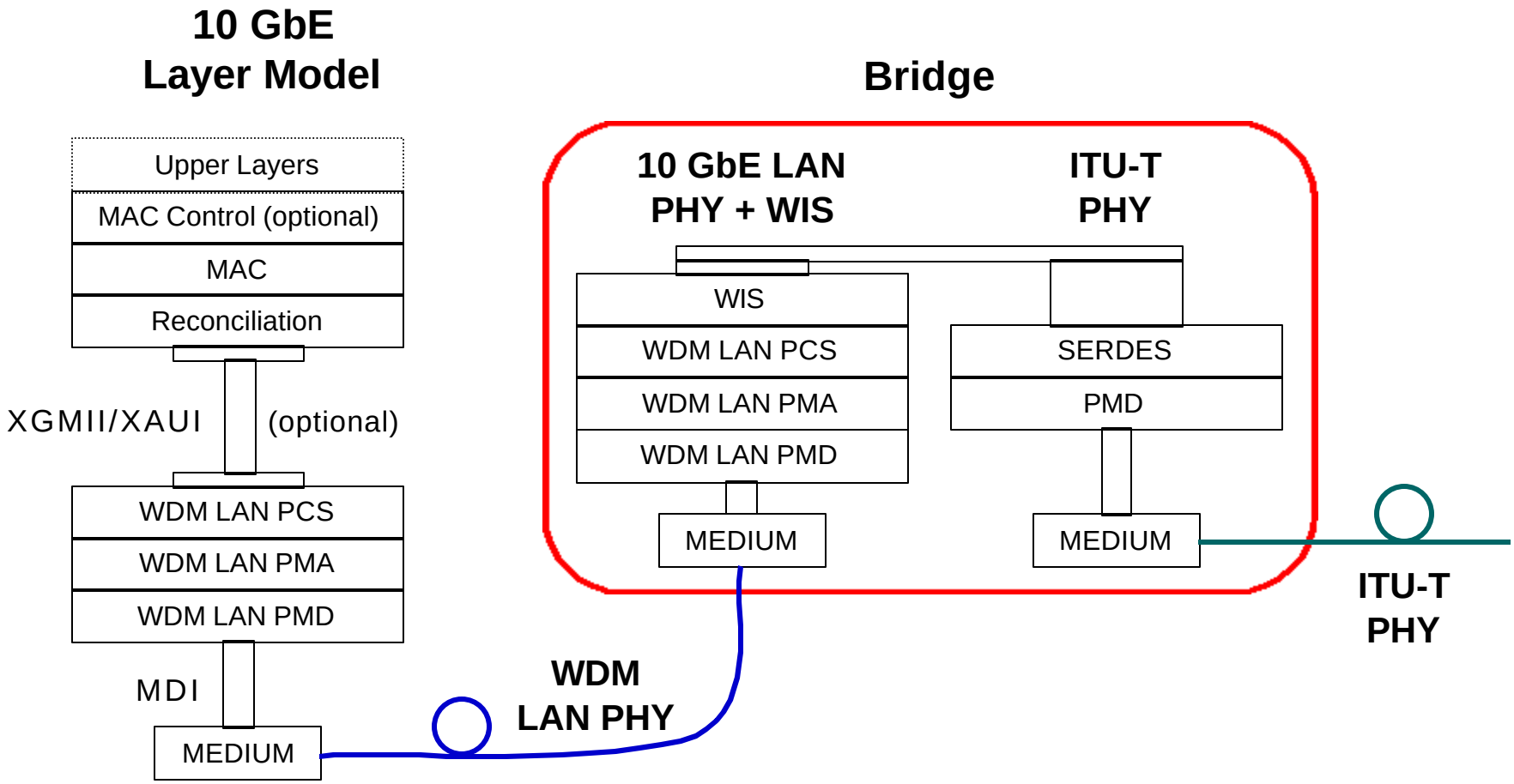
Simple Implementation #2



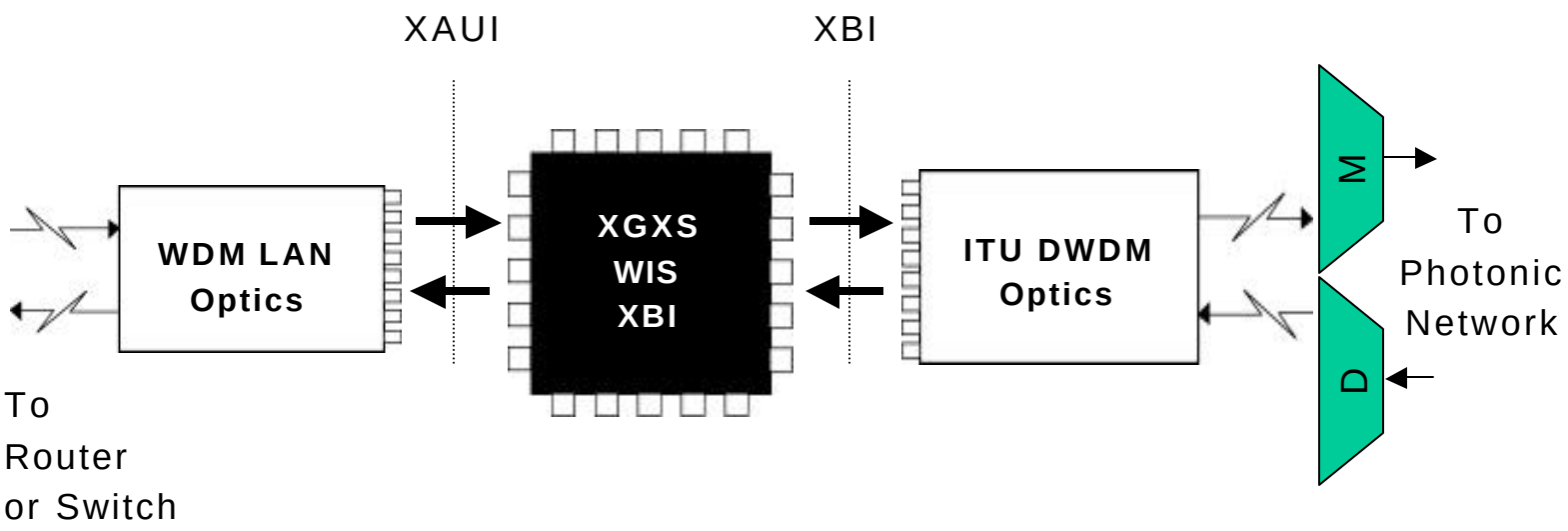
E.g. Switch port, no XGMII, integrated MAC/RS/XGXS, 20" XAUI on 2 cards + backplane

Retimer/Repeater In Optical Module to attenuate jitter

WDM LAN ➔ WAN via Layer 1 Bridge



WDM ➔ DWDM Transponder Example Implementation



XAUI/XGXS: http://grouper.ieee.org/groups/802/3/ae/public/may00/taborek_2_0500.pdf
WIS: http://grouper.ieee.org/groups/802/3/ae/public/may00/bottorff_1_0500.pdf
XBI: http://grouper.ieee.org/groups/802/3/ae/public/may00/robinson_1_0500.pdf

Summary

- Meets HSSG Objectives and PAR 5 Criteria
- Simple PCS/PMA Architecture resembling 1000BASE-X PHY
- Flexible PCS/PMA Implementation
- Compatible with XGMII, XAUI/XGXS interfaces
- MultiChannel (WDM, parallel) PMD Independent
- Simple L1 WAN Bridge implementation