WIS Jitter Patterns

Objectives

- 1. Conform to PMA/PMD test requirements
- 2. Keep the pattern generator/checker simple
- 3. Avoid modifying WIS functionality as far as possible
- 4. Stay close (or same as) standard SONET practice
 - ✓ Re-use SONET BERT and jitter test equipment, and pre-existing work
 - ✓ ITU-T Recommendation G.957: OPTICAL INTERFACES FOR EQUIPMENTS AND SYSTEMS RELATING TO THE SYNCHRONOUS DIGITAL HIERARCHY
 - ✓ ITU-T Recommendation 0.181: EQUIPMENT TO ASSESS ERROR
 PERFORMANCE ON STM-N INTERFACES



Opt. 2: Follow ITU 0.181 Annex C

(with modifications)



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Comparison of approaches

Option 1	Option 2
(custom pattern)	(re-use SONET framer)
Need extra hardware in WIS -Separate pattern generator -Separate framer and checker	Re-use most of the WIS functionality -Change input at PCS svc. I/F -Modify J0/Z0 bytes from framer
Completely controllable repeat rate and pattern	Fixed repeat interval (125 μ s) and pattern structure
Totally separate from WIS core	Combined with WIS functions
functionality	- Test pattern changes may
- Changes don't affect WIS	impact WIS

Recommendations

- If either test pattern is acceptable to the PMA/PMD groups, then select Option 2 (re-use WIS framer to generate pattern) as it is simpler and cheaper
- 2. Otherwise, select Option 1
- 3. Add MDIO register support for whichever option is adopted

SONET BERT/Jitter Pattern

(O.181 with CID generator)



From ITU O.181, Equipment to assess error performance on STM –N interfaces Courtesy Dan Wolaver, T1X1.3