#### P802.3ae Serial Jitter Test Pattern Ad-Hoc Summary

Ben Brown Ad-Hoc Chair 23-May-2001

## **Participants**

- Don Alderrou
- Piers Dawe
- Gareth Edwards
- John Ewen
- Dawson Kesling
- Peter Ohlen
- Anthony Sanders
- Pat Thaler

- Ben Brown
- Schelto van Doorn
- Jennifer Evans
- Steve Haddock
- Tom Lindsay
- Bill Reysen
- Jonathan Thatcher
- Tim Warland

#### Motivations - Why not use the 1+x<sup>28</sup>+x<sup>31</sup> PRBS?

- Use a "real life" pattern (some PLLs may expect/require sync bits)
- Use existing logic (1+x<sup>39</sup>+x<sup>58</sup> scrambler), easy to generate
- Focus on patterns that occur once in a given period of time (week/day/hour?)
- Find a pattern that is sufficiently stressful to test PLL designs

#### Tests to be supported

- Tests with mixed frequency pattern
  - Jitter
     RX Sensitivity/Saturation
  - Eye Mask
     Stressed RX Sensitivity
- Tests with square wave
  - Rise/Fall Time
    ER/OMA
- Tests that can be done either way
  - Optical power
    Encircled flux
  - RIN
  - Spectral Width/Center/Side Mode Suppression

#### **Square Wave Pattern**

- A single frequency is adequate
- Decided upon a range to suit different implementation styles
  - Minimum 4 bits high/4 bits low
  - Maximum 11 bits high/11 bits low
- Repeat forever
- Transmit tests only
- No need to capture at receiver

### LAN vs. WAN

- This discussion is LAN Serial only
- The WAN PHY intends to provide a separate solution to a comment against Clause 50.
  - Modifications to pattern in ITU-T G.957
  - Other pattern using SONET framing and scrambler with fixed payload

#### Ideal Jitter Pattern "Must Have"s

- Short enough to fit into a BERT
- Several content types:
  - Long run length with no transitions
  - Long run lengths with few transitions
  - Rapid change in transition density
  - Extreme running disparity
  - Rapid change in running disparity
  - Polarity bias, stresses a particular data edge

# "Must Have"s (cont.)

- Ability to generate and check the pattern in the same device at the same time
- Error counter attributes:
  - Sticky at max
  - Can be reset for new measurement
  - Count only once per 66-bit block
- Ability to synchronize in the presence of errors - at 10<sup>-5</sup> or perhaps even 10<sup>-3</sup>

#### "Nice to Have"s

- Ability to measure BER "down" to a particular value
  - 8-bit counter supports 10<sup>-8</sup> when read once per second
  - Higher BERs might require a wider counter or more frequent reads
- Pattern should not be so stressful that EMI is compromised

## Methodology: Common to Original Proposals

- Use the existing  $1+x^{39}+x^{58}$  scrambler
- Seed the scrambler with start values
  - Repeatable
  - Predictable
- Operate the scrambler for a finite time
- Use 66-bit blocks with fixed, control block sync header
- Count errors at the receiver

## Methodology: Agreed upon by Ad-Hoc participants

- Fixed pattern length: 33792 bits (4x128x66)
- 2 58-bit Seeds (e.g. "typical" & "atypical" patterns)
- Always invert the patterns in the following format:
  - Seed A
  - Seed A Invert
  - Seed B
  - Seed B Invert

# Methodology (Cont.)

- Registers common between TX & RX
- Data input selectable between all 0s and the LF value
- Receive:
  - No elaborate PCS sync state machine
  - Ignore the first error in every group of 128
  - BERT without 64B/66B may compare every bit to known pattern
  - BERT must find unique bit pattern for sync

#### Pattern Content

- Run length on the order of ~50 bits
- "Stressful" portion NOT at beginning
- Impossible to suggest exact bit patterns
- Use disparity slopes & base line wander sigmas instead
- Choose something that is close
- All should test it
- If a better one is found later, that's why the seeds are programmable!

# **Continuing work**

- Specify what the pattern contents actually need to be
- Search for seeds that will generate the associated patterns

## HELP

- Once we find appropriate patterns, we can make them available on the web site (hex/ascii)
- We need individuals that can actually test these patterns

## **Straw Poll Questions**

- Is it mandatory for a transmitter to support these testing modes?
- Y: 54 N: 3 A: 14
- Is it mandatory for a receiver to include the random portion of the testing modes?
- Y: 47 N: 2 A: 23
- Is it mandatory be able to operate both transmit and receive simultaneously?
- Y: 35 N: 4 A: 30

# Motion

Accept the proposals and straw poll results from brown\_1\_0501.pdf to be used as guidance through comment resolution

Move: Ben Brown

Second: Pat Thaler

Technical (75%)

Pass:85	Fail:1	Abstain:9	Everyone
Pass:56	Fail:1	Abstain:7	802.3 Voters