

# LSS for Link Status Mechanism

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10 Gigabit Ethernet

LSS for Link Status Mechanism

Slide 1

# Presentation Purpose

- Review of Sept'00 LSS Proposal\*

\* Link Signaling Sublayer Proposal by 47 individuals from 25 companies  
[http://grouper.ieee.org/groups/802/3/ae/public/sep00/ishida\\_1\\_0900.pdf](http://grouper.ieee.org/groups/802/3/ae/public/sep00/ishida_1_0900.pdf)

- Concept of Link signaling
- Mechanism of Break Link (BL) and Remote Fault (RF)

- Update receive detection state diagrams for LSS

- Improve robustness by adopting a watchdog timer and hysteresis

- Propose overall link status mechanism with LSS

- Define RF&BL mechanism in Reconciliation Sublayer
- Up-the-stack BL signaling by pure Idle generation in PCS/XGXS

# What is Link Signaling?

- Convey status/control register bits to its Link Partner
  - RF (remote fault) : fault detected on the receive path
  - BL (break link) : link\_reset by STA
  - optional OAM&P\* : WAN-PHY compatible trace identifier, e.t.c.
    - \* Operations, Administration, Management, and Provisioning
- Use an Idle Column as the vehicle
  - Signal on the data path, not on the MDIO nor on “Pins”
  - Replace an Idle Column with an Link Signaling Column
- Signal repeatedly once every time frame (e.g. 125 us)
  - Independent of PCS/XGXS varieties
  - Less frequent to avoid XAUI EMI
  - Sufficiently frequent for robust detection

# Link Signaling Example

PHY stream  
after RS

Lane 0	...		LS			...	...			LS		...	...		LS			...
Lane 1	...		d <sub>1</sub>			...	...			d <sub>1</sub>		...	...		d <sub>1</sub>			...
Lane 2	...		d <sub>2</sub>			...	...			d <sub>2</sub>		...	...		d <sub>2</sub>			...
Lane 3	...		d <sub>3</sub>			...	...			d <sub>3</sub>		...	...		d <sub>3</sub>			...

after XGXS  
or X PCS  
(8b/10b)

Lane 0	...	A	LS	K	R	...	...	K	K	LS	R	...	...	K	LS	A	R	...
Lane 1	...	A	D <sub>1</sub>	K	R	...	...	K	K	D <sub>1</sub>	R	...	...	K	D <sub>1</sub>	A	R	...
Lane 2	...	A	D <sub>2</sub>	K	R	...	...	K	K	D <sub>2</sub>	R	...	...	K	D <sub>2</sub>	A	R	...
Lane 3	...	A	D <sub>3</sub>	K	R	...	...	K	K	D <sub>3</sub>	R	...	...	K	D <sub>3</sub>	A	R	...

after  
R PCS  
(64b/66b\*)

header	...	10	10	...	...	10	10	...	...	10	10	...	...	10	10	...	...	
Lane 0	...	2d	0000	1e		...	...	1e		4b	0000	...	...	2d	0000	1e		...
Lane 1	...		d <sub>1</sub>			...	...			d <sub>1</sub>		...	...		d <sub>1</sub>			...
Lane 2	...		d <sub>2</sub>			...	...			d <sub>2</sub>		...	...		d <sub>2</sub>			...
Lane 3	...		d <sub>3</sub>			...	...			d <sub>3</sub>		...	...		d <sub>3</sub>			...

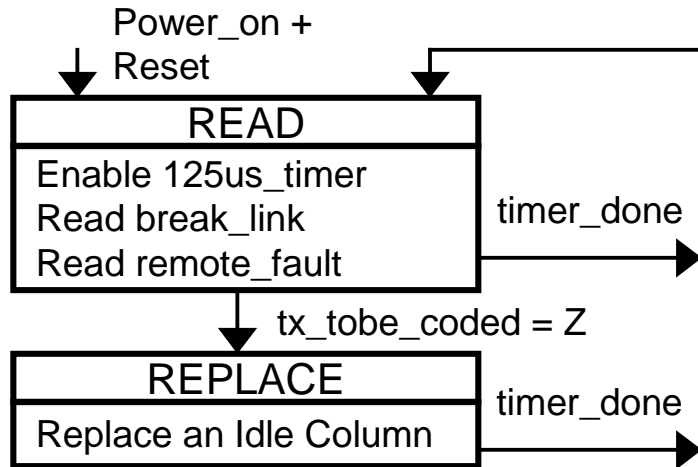
LS: Link Signaling Identifier K28.4 (0x9c,1)

\* See Page 19 (Optional Code Features) of [http://www.ieee802.org/3/ae/public/jul00/walker\\_1\\_0700.pdf](http://www.ieee802.org/3/ae/public/jul00/walker_1_0700.pdf)

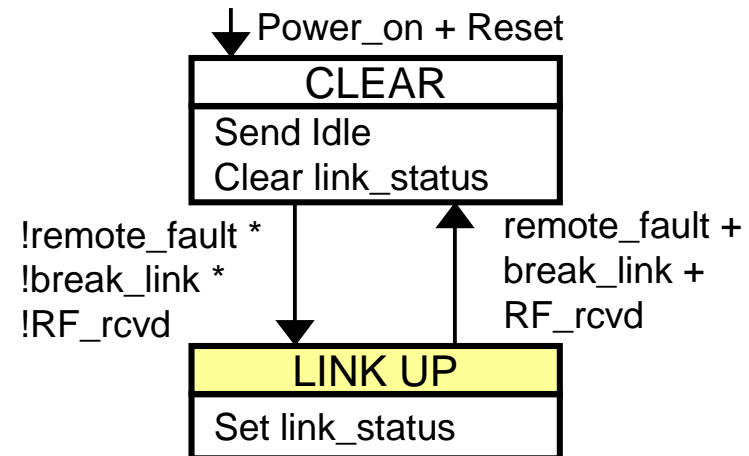
# BL&RF Mechanism on LSS (1/2)

- Transmit the Link Status Column once every 125 us
  - Covey BL/NoBL and RF/NoRF simultaneously
  - Assert BL when STA triggers link\_reset
  - Assert RF when failure is being detected on the receive path
- Define Link Status simply as a Boolean variable
  - $\text{link\_status} = \text{!(rx\_in\_sync + BL\_rcvd)} * \text{!(RF\_rcvd + break\_link)}$ 
    - $\text{!rx\_in\_sync + BL\_rcvd}$  : failure on the receive path
      - And hence RF is being sent on the transmit path
    - $\text{RF\_rcvd + break\_link}$  : failure on the transmit path
      - That's why RF is being or will be detected on the receive path
- Send Idles whenever link\_status is False
  - Use Idle stream for link initialization

# BL&RF Mechanism on LSS (2/2)



LS Code Transmit State Diagram



Link State Diagram

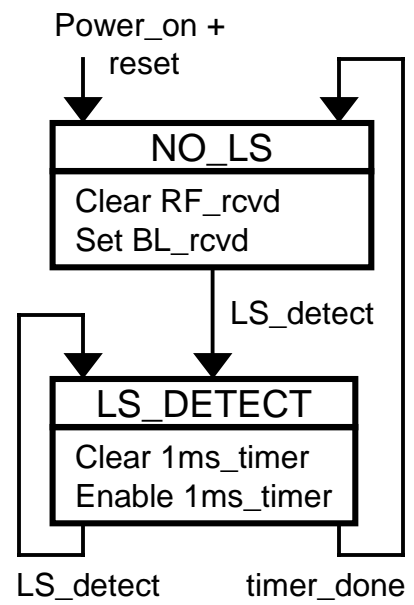
Notes: break\_link = link\_reset + power\_down  
remote\_fault = !rx\_in\_sync + BL\_rcvd

In this mechanism RF is sent whenever the local receiver is not ready to use. Receiving break link (BL\_rcvd) asserts remote\_fault since Link Partner wants to reset Local Device's PHY. Whether or not resetting the receiver sync status is an implementation.

# What is Updated from Sept'00 ?

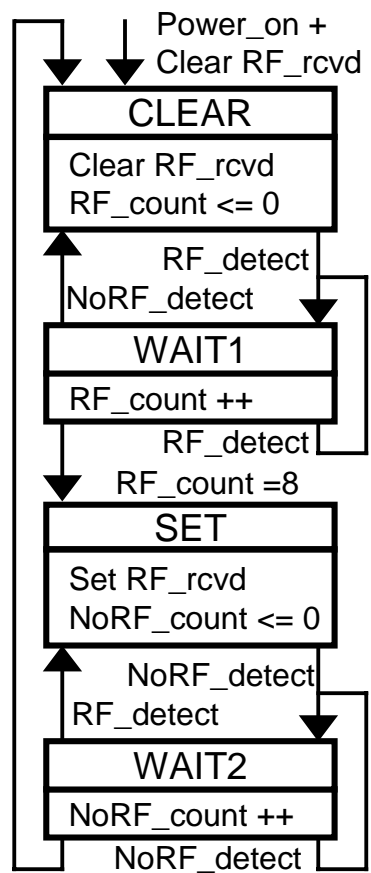
- Improved robustness in Link Signaling Detection
  - Add a watch dog timer
    - Link Signaling Failure should be detectable
    - Clear link\_status if the Link Status Column is not detected for greater than 1 millisecond
  - Adopt hysteresis for BL&RF detection
    - Protect from misdetection during error burst
    - Require 8 consistent Link Status Column detection before setting/clearing the BL/RF received status

# Rx Detection State Diagrams; Updated



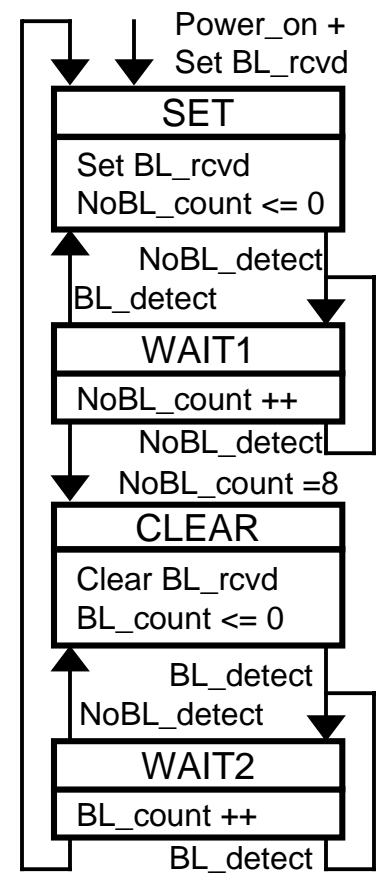
RX LS Detection S. D.

$$\begin{aligned}
 \text{LS\_detect} = & (\text{TYPE}=\text{Z}) \\
 & (\text{lane0}=\text{K28.4}) + \\
 & (\text{lane1}=\text{D18.2}) + \\
 & (\text{lane2}=\text{D18.2}) +
 \end{aligned}$$



NoRF\_count = 8

RX RF Detection S. D.



BL\_count = 8

RX BL Detection S. D.

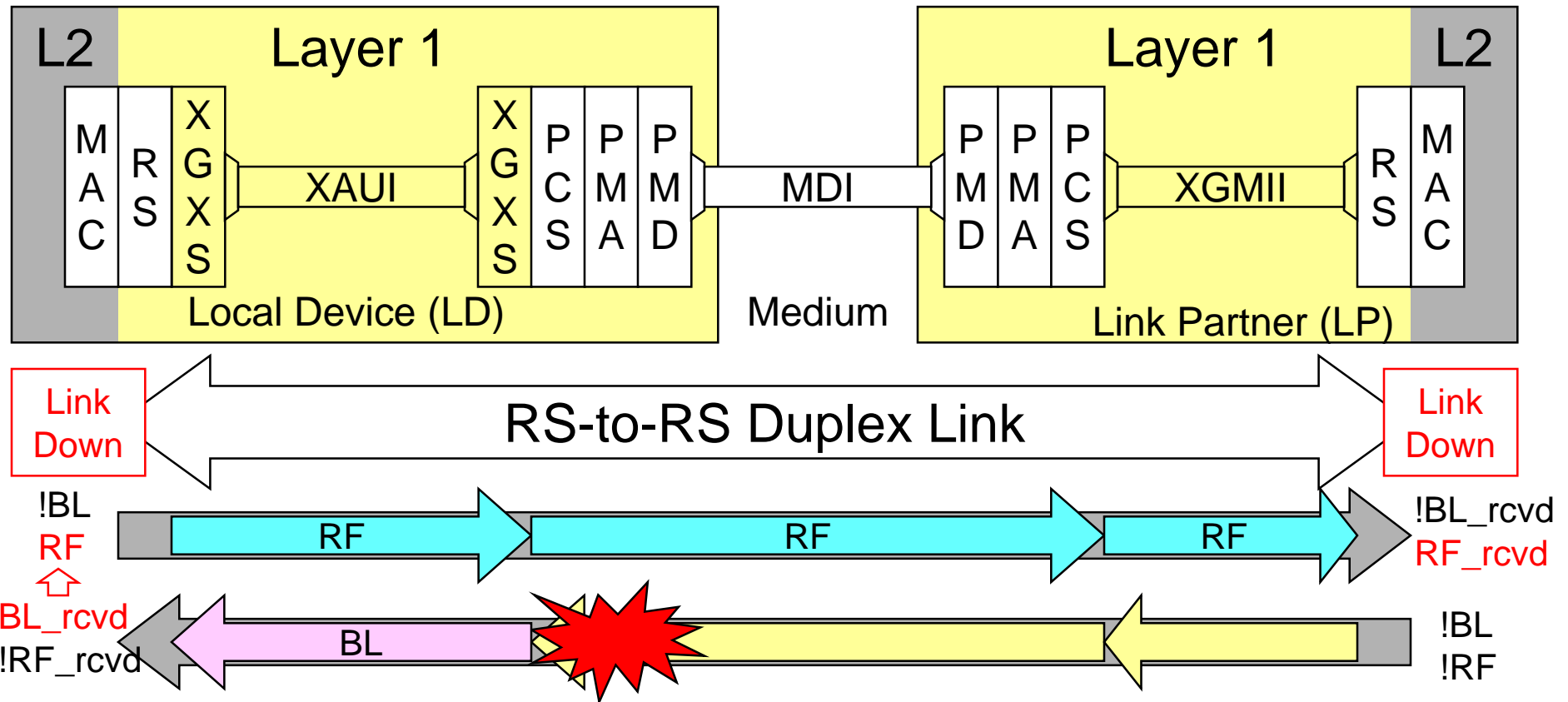
$$\begin{aligned}
 \text{RF\_detect} &= \text{LS\_detect} * \\
 & \quad (\text{lane3} = \text{RF}); \\
 \text{NoRF\_detect} &= \text{LS\_detect} * \\
 & \quad (\text{lane3} = \text{NR}); \\
 \\ 
 \text{RF} &= (\text{D14.6} + \text{D9.2} + \\
 & \quad \text{D10.1} + \text{D13.5}); \\
 \text{NR} &= (\text{D18.2} + \text{D21.6} + \\
 & \quad \text{D22.5} + \text{D17.1}); \\
 \\ 
 \text{BL\_detect} &= \text{LS\_detect} * \\
 & \quad (\text{lane3} = \text{BL}); \\
 \text{NoBL\_detect} &= \text{LS\_detect} * \\
 & \quad (\text{lane3} = \text{NB}); \\
 \\ 
 \text{BL} &= (\text{D21.6} + \text{D9.2} + \\
 & \quad \text{D17.1} + \text{D13.5}); \\
 \text{NB} &= (\text{D18.2} + \text{D14.6} + \\
 & \quad \text{D22.5} + \text{D10.1});
 \end{aligned}$$



# Overall Link Status Bit

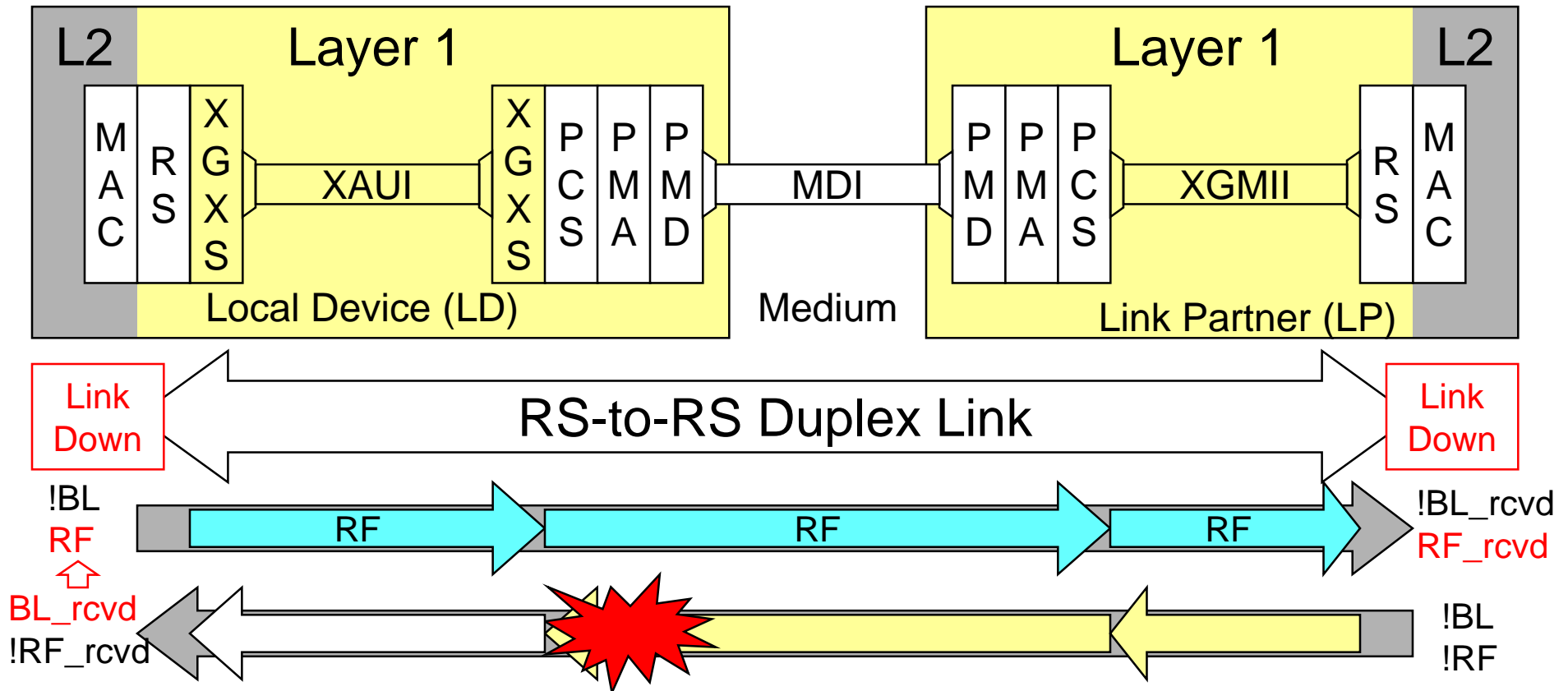
- Requirement
  - Link Aggregation refers to the unique link status bit
  - This status bit should be cleared in real time whenever
    - something wrong on the entire receive path, such as
      - Rx can not establish the synchronization
      - Break Link is received
    - something wrong on the entire transmit path, such as
      - Remote Fault is received
      - Break Link is transmitted (e.g. STA is resetting the link status)
  - MDIO is less useful for this real time management
    - while it provides fault debugging capability within the Local Device
- Issue in 802.3ae
  - Cumulative link status over multiple intermediate links
    - XGXS-to-XGXS, PCS-to-(WIS-to-WIS)-to-PCS,XGXS-to-XGXS

# How About Up-the-stack BL Signaling?



- Local Device's PCS detects !rx\_in\_sync, then asserts BL on the receive path
  - PCS generates Idle stream with interspersed BL-asserted Link Status Column
- RS receives BL, then asserts RF on the transmit path based on the BL&RF mechanism

# Simpler PCS Still Works!



- Local Device's PCS detects !rx\_in\_sync, then **just generates Idles** on the receive path
  - Idle stream with no Link Status Column yields BL\_rcvd in RS
- Local Device's RS then asserts RF on the transmit path based on the BL&RF mechanism

# Link Status Mechanism Proposals

- Adopt LSS and its BL&RF mechanism in Reconciliation Sublayer
  - This does not preclude BL&RF mechanism in XGXS/PCS instead of RS as far as no exposure interface is implemented between them
  - Generate a Link Status Column for BL/RF on the transmit path
  - Detect BL/RF on the receive path with a watchdog timer and hysteresis
  - Set or clear link status simply as a Boolean variable as
    - $\text{link\_status} = \text{!BL\_rcvd} * \text{!RF\_rcvd}$
- Minimize the requirement in the other PHY sublayers
  - Just be transparent to the Link Status Column
  - Produce Idles out when they do not have input sync
    - None of LSS, Idle equivalent, and its translation is required in XGXS/PCS
    - This does not preclude intelligent XGXS/PCS/PMA that could process the Link Signaling Column for optional OAM&P
    - OAM&P would also be useful for remote fault-debugging