MDIO issues

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Issues to resolve

- Electrical interface specification
- Optionality
- PMA/PMD speed control
- Devices in chip register
- Access types
- Adjust register locations

Electrical interface

- Is a new electrical interface specification required for MDIO ?
  - Clause 22 required 5V tolerance, but can operate at 3v3 levels. 5V tolerance seems an unnecessary burden.
  - Even 3V3 tolerance may be too restrictive for future developments

Motion

- Move that an IEEE P802.3ae Task Force Ad Hoc will specify a low voltage electrical specification for the MDIO interface for adoption in January 2001.
- Moved : Ed Turner, Seconded : David Law

802.3 voters : Passed by acclamation.

Motion to amend to :

- Move that an IEEE P802.3ae Task Force Ad Hoc will specify a low voltage electrical specification for the MDIO interface for adoption in January 2001, based on the JEDEC 1.5V HSTL standard.
- Moved : Tom Dineen, Seconded : Don Pannell

802.3 voters : Y : 9, N : 26, A : 55

Motion to amend motion fails

Motion

- Move that the IEEE P802.3ae Task Force adopt the timing specified in Clause 22 for the MDIO interface.
- Moved : Ed Turner, Seconded : Brad Booth

802.3 voters : Y : 51, N : 1, A :44

Passed

Optionality

- Is the MDIO interface optional ?
  - The MDIO interface is now separate from the XGMII interface
  - Previously part of *optional* MII / GMII
  - You did not *have* to implement the MDIO interface
    - e.g. a PHY without an MII did not require an MDIO interface. Could use a processor interface.

Example from auto-negotiation

28.2.4 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. If an MII is physically implemented, then management access is via the MII Management interface. **Where no physical embodiment of the MII exists, an equivalent to MII Registers 0, 1, 4, 5, 6, and 7 (Clause 22) are recommended to be provided.**

Optionality

- We can :
  - Make the MDIO interface optional
    - Then you don't have to implement it at all
    - Would need words in the Clauses for required registers
  - Make MDIO interface part of each optional interface (XGMII, XAUI, XSBI, SUPI)
    - Any device with one of these interfaces would have to also implement the MDIO interface
  - Make the MDIO interface mandatory for 10G
    - How do you conformance test it ?

Straw poll

- Make the MDIO interface
  - optional (124)
  - mandatory (0)
  - a mandatory part of the optional interfaces XGMII, XAUI, XSBI, SUPI. (0)

Motion

- Move that the IEEE P802.3ae Task Force makes the MDIO electrical interface optional.

Moved : Ed Turner, Seconded : David Law

All present : Passed by acclamation

PMA/PMD speed

- Currently one bit per MDI interface speed giving the PMA / PMD capability
  - 10GBASE-W4, 10GBASE-X4, Serial 10GBASE-W, 10GBASE-R
- Propose the addition of control bits to select the speed to lock to
  - similar to 10/100 PHY's 'ability' and 'speed selection'
  - allows PLL filters to be tuned

Motion

- Move that the IEEE P802.3ae Task Force clause editors define control bits for PMA/PMD port type selection.

Moved : Ed Turner, Seconded : David Law

All present : Passed by acclamation

Proposal

- Include a ‘devices in chip’ register with a bit per device.
- Control bits ‘reset’ and ‘power down’ will affect all devices listed in the ‘devices in chip’ register
- Clears up ambiguity over what these bits do in chips containing multiple MDIO devices
- Will need to move registers around to fit the ‘devices in chip’ register in at the base of the address space

Motion

- Move that the IEEE P802.3ae Task Force adopt a ‘devices in chip’ register with a bit per device.

Moved : Ed Turner, Seconded : David Law

Motion to table :

- Move that the IEEE P802.3ae Task Force adopt a ‘devices in chip’ register with a bit per device.

Moved : Bob Grow, Seconded :Don Pannell

All present : Passed by acclamation

Tabled.

Proposal

- Write, read and post-read-increment-address access types allow for:
  - single register reads and writes
  - polling of a single register without re-sending the address frame
  - read bursts
  - write-then-verify bursts

Proposal

- Write, post-write-increment-address and post-read-increment-address access types allow for:
  - single register reads and writes
  - write bursts
  - read bursts
  - write-then-verify bursts
- Will not allow polling without re-sending the address frame

Motion

- Move that the IEEE P802.3ae Task Force change the read access type to a post-write-increment-address access type.

Moved : Ed Turner, Seconded : David Law

All present : Fails by acclamation

DTE XGXS / 10GBASE-X PCS register bits

- Bit locations for DTE XGXS don’t match those for 10GBASE-X PCS
- Need approval to move XGXS register bits around to make them match

Motion

- Move that the IEEE P802.3ae Task Force authorize the editor of Clause 33 to re-order the registers and register bits to accommodate the approved changes.

Moved : Ed Turner, Seconded : David Law

All present : Passed by acclamation

Outstanding issues

- PICS
  - Still to be done
- Updates as required by other Clauses
  - PCS and WIS devices to be separated
  - PMA/PMD signal detect / lock
  - Request editors to pass register bit requirement to me