Optical link model
that treats jitter and amplitude fluctuations jointly

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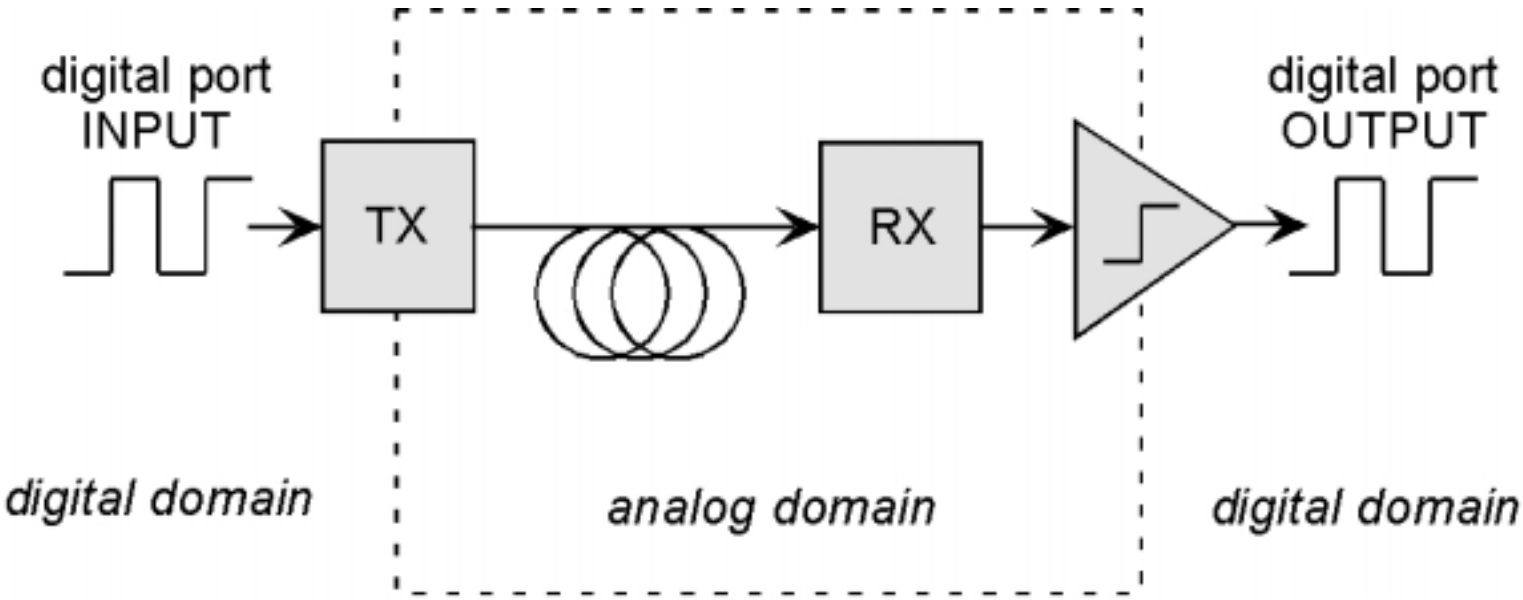
Objective

Development of a quasi-analytic model for digital transfer performance (digital in to digital out) for worst-case analysis of real-life implementations.



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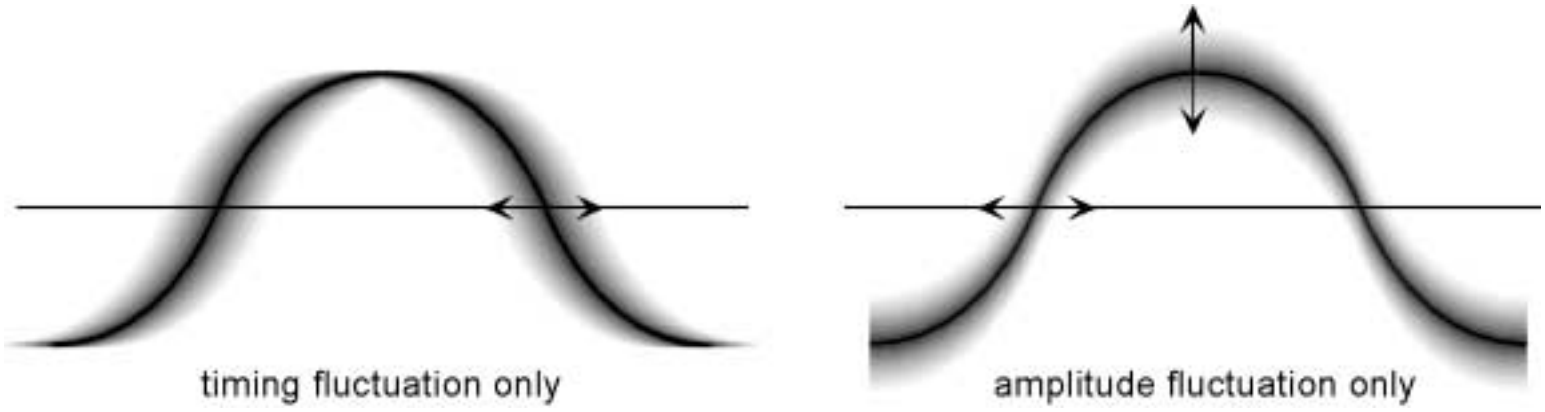
Sources of jitter

Pure timing fluctuation (random and deterministic)

- Digital input
- Other pure timing disturbances

Amplitude fluctuation manifested as jitter

- Laser, fiber, and receiver noise -> random jitter
- ISI, cross-talk, power-supply -> deterministic jitter



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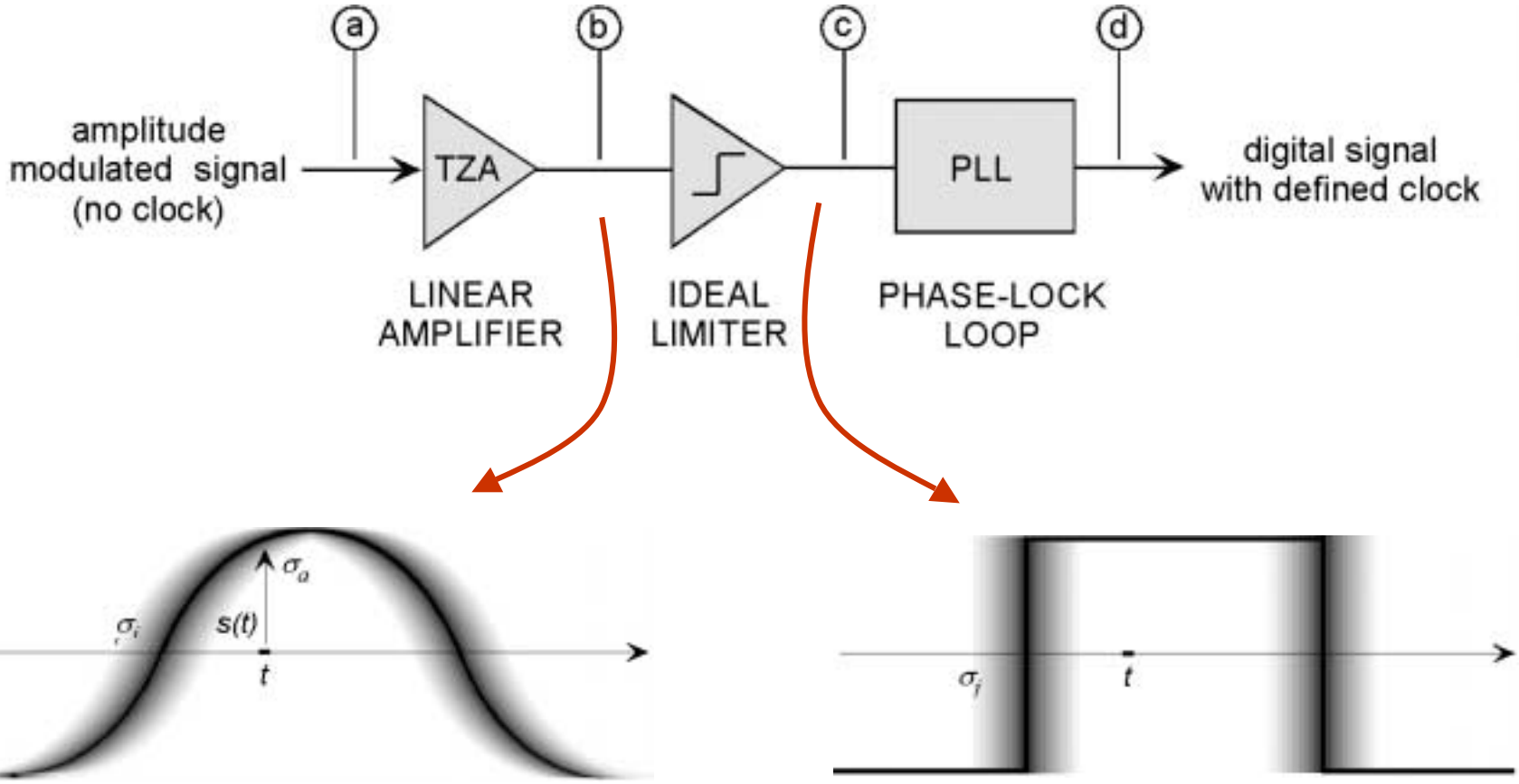
Model for the receiving chain



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How to combine timing and amplitude fluctuations?

- ✓ Band-limiting and attenuation treated in amplitude (same as GbE model).
- ✓ Random (Gaussian) fluctuations treated in amplitude
  - Amplitude noise (MPN, MN, RIN, RX) – (same as GbE model)
  - Jitter converted to amplitude at the edge
- ✓ Deterministic fluctuations (amplitude and time)
  - Separated into equivalent random and deterministic signal
  - Both treated in time domain and as inputs to model
    - Deterministic *W* parameter in Clauses 52/53.

- Focused on link implementation rather than standardization
- Unstressed receiver sensitivity is an input.
- Included decision level shift due to DCD .
- 850 nm MM VCSEL links (at the moment).

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Key results

o It is possible to obtain noise and jitter at any place in the link.
o Approximate expressions for random jitter at TP3 and TP4.
o Measured jitter parameters can be entered into the model

Main issue:

TP3 jitter space determined in Clauses 52/53
TP4 jitter space determined by PLL jitter tolerance
*Consequence: Jitter generation in the receiver is **limited***

With assumptions:

- **All** jitter contributed by receiver is random
- Edge-rate and eye-shape at TP3 is known (compliance signal)

This leads to an additional *unstressed receiver sensitivity* requirement.
If this requirement is lower than the unstressed receiver sensitivity assumed in the 10GbE model, the difference becomes an RX-RJ power penalty.

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Can we build the parts that are specified by the standard?

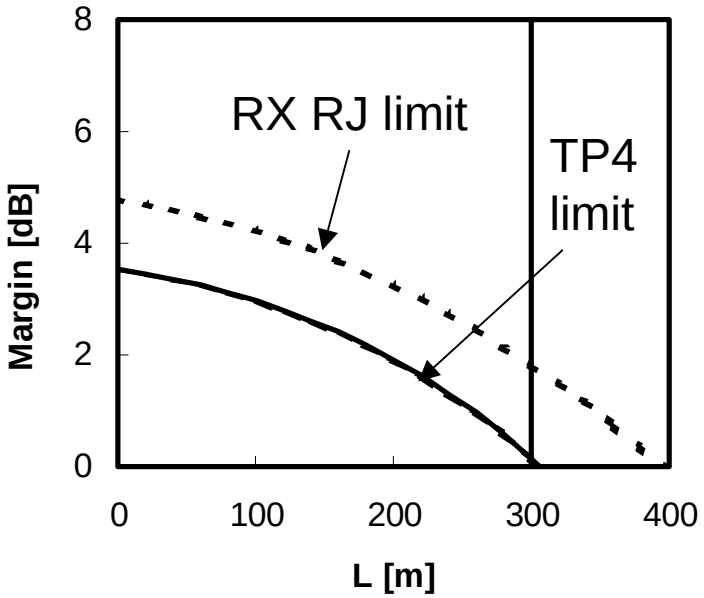
Specifically: receivers and re-timers.

- Jitter tolerance of practical PLLs at 3.2 GBaud ranges 0.5 – 0.7 UI. Analyzing link performance with center-of-the-eye makes the link performance overly optimistic.
- TP3 jitter specification should consider practical receiver limitations. Is it practical to build 850 nm 10 Gbaud receiver with –18 dBm OMA unstressed sensitivity?
- Stringent specifications mean higher cost.

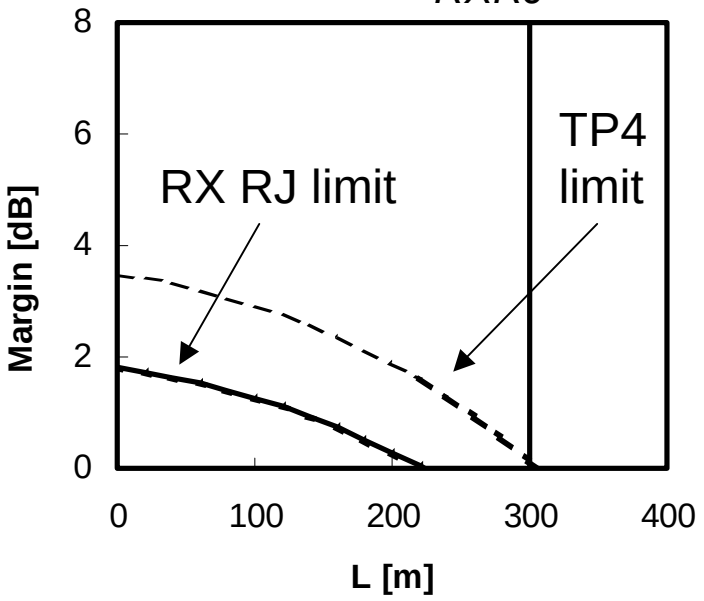
10GBASE-SR example (RX RJ Limit)

TP3 jitter: W = 0.35 σ = 15 mUI, TP4 DJ = 0.4 UI
Unstressed RX OMA = -12 dBm
TP4 sampling: center of the eye

P_{RXRJ} = 1.2 dB



Eye opening 0.0 UI
Stress OMA = -8.9 dBm



Eye opening 0.25 UI
Stress OMA = -8.9 dBm

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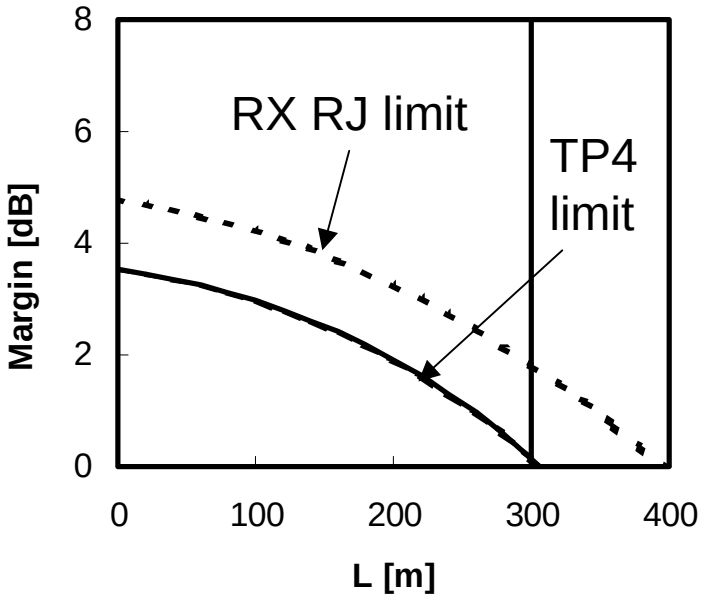
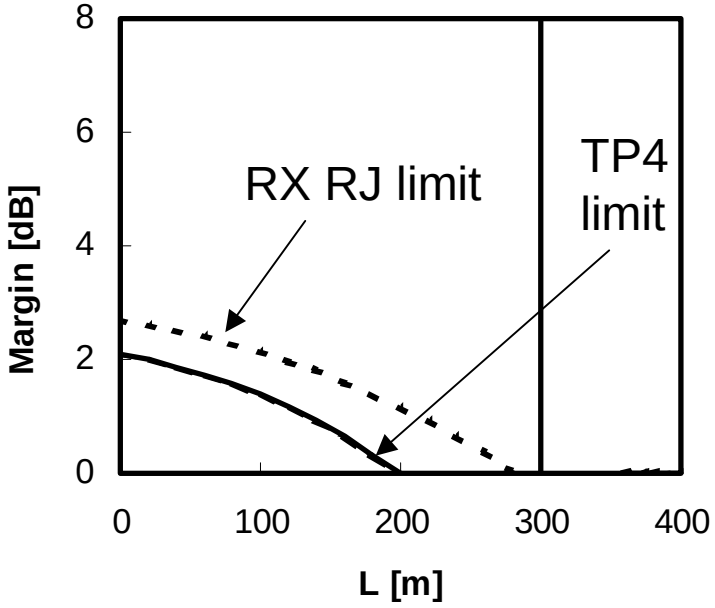
10GBASE-SR example (eye opening limit)

TP3 jitter: W = 0.35 σ = 15 mUI, TP4 DJ = 0.4UI
Uns. RX OMA = -12 dBm
TP4 sampling: 0.25 UI eye opening edge P_{TP4} = 6.3dB



Eye opening 0.0 UI
Stress OMA = -8.9 dBm



Eye opening 0.25 UI
Stress OMA = -13.9 dBm

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Summary

- Quasi-analytic optical link model that includes time and amplitude fluctuations developed the similar assumptions as the 10GbE link model.
- Implemented on a Excel spreadsheet
- White-paper describing the analysis in detail is available
- The model allows for relating jitter and noise parameters.
- TP4 jitter and TP3/TP4 jitter should be included into analysis for practical device realization and “informative” values.

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