DSP-Based Equalization for Optical Channels

Feasibility of a VLSI Implementation

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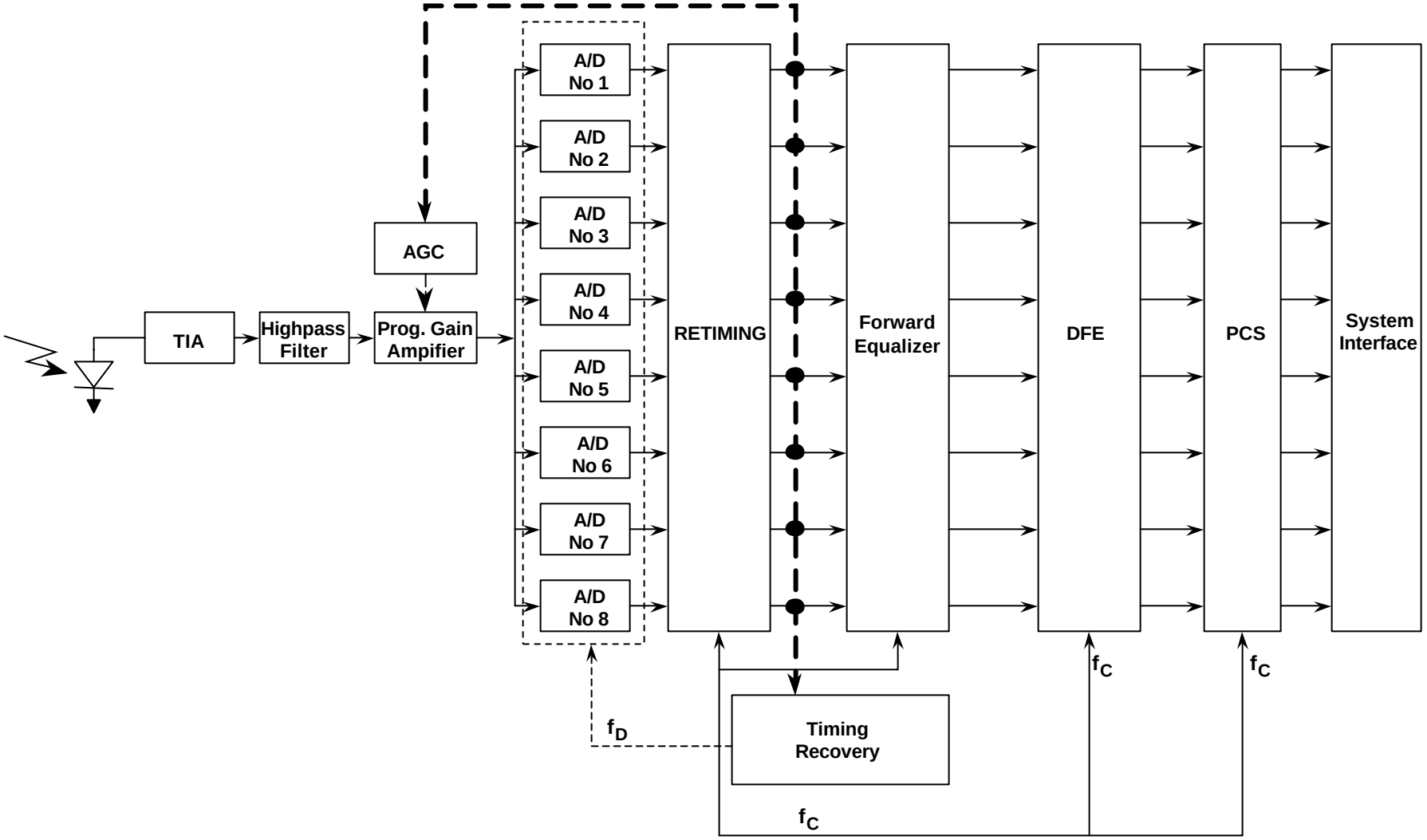
Introduction

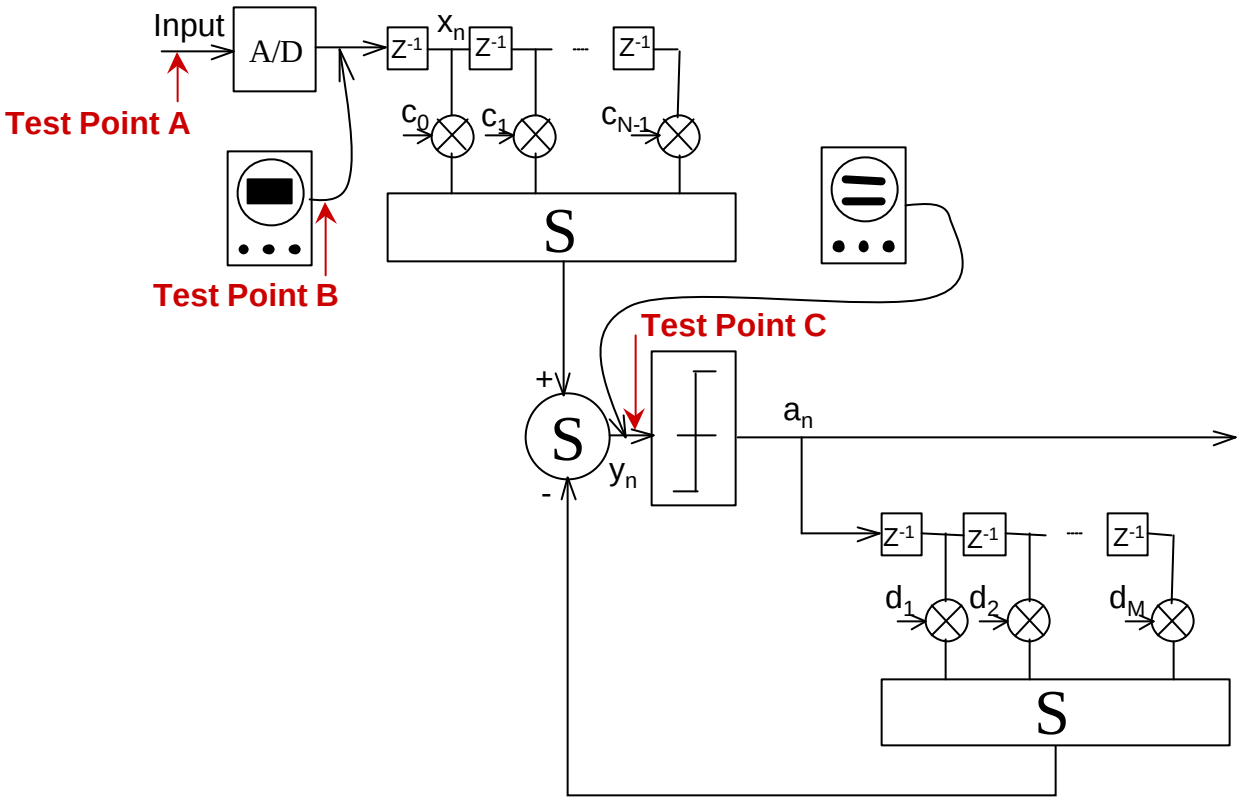
- **This talk will discuss a receiver based on Decision-Feedback Equalization (DFE) and its implementation using DSP techniques**
- **The proposed equalization technique is entirely done at the receiver. It does not require any modification to the current PMD proposals considered by 802.3ae**
- **It is not necessary to know the channel a priori, since the equalizer is adaptive and it automatically identifies the channel response**
- **The time constant for the equalizer adaptation is <<1ms (typically a few microseconds at 10Gb/s data rates)**
- **The DSP-based architecture described in this presentation is only intended to be an example of a possible implementation. Alternative implementations are also possible and they will be investigated by the ad-hoc group**

Block Diagram of Receiver



NOTE: Block diagram assumes a parallelization factor of 8

Block Diagram of Equalizer



NOTE: This is a conceptual block diagram. It does not reflect a parallel implementation

The eye patterns at Test Points A, B, and C from simulations at 3.125Gb/s and 10Gb/s will be shown in slides 11 through 13 and 16 through 18

Digital Equalization

- **The Feedforward Equalizer (FFE) does mostly phase equalization so that the intersymbol interference (ISI) at its output is caused by the "postcursors" (samples occurring after the main sample) of the channel impulse response**
- **The Decision-Feedback Equalizer (DFE) cancels the postcursor ISI**
- **It is possible to design the DFE in such a way that it can deal effectively with nonlinear ISI**

Simulation Environment

- **Pulse Preprocessing:**
  - ➢ Remove DC bias
  - ➢ Resample pulse with a sampling rate f_s
  - ➢ Convolve with trapezoidal pulse with rise and fall times t_s
  - ➢ Convolve with single-pole high-pass filter with cutoff frequency f_h and with single-pole low-pass filter with cutoff frequency f_l. The high-pass filter models AC coupling in the TIA, and the low-pass filter models the bandwidth limitation of the TIA
  - ➢ The pulse is normalized by dividing it by the power of the calibration pulse and multiplying it by the assumed launch power
- **Phase selection and decimation to the symbol rate:**
  - ➢ The pulse is decimated to the symbol rate using as sampling phase the phase that maximizes the energy of the decimated pulse
- **Equalization:**
  - ➢ The coefficients of the FFE and DFE are computed using the Minimum Mean Squared Error algorithm (Ref.[4], pp. 521-524)

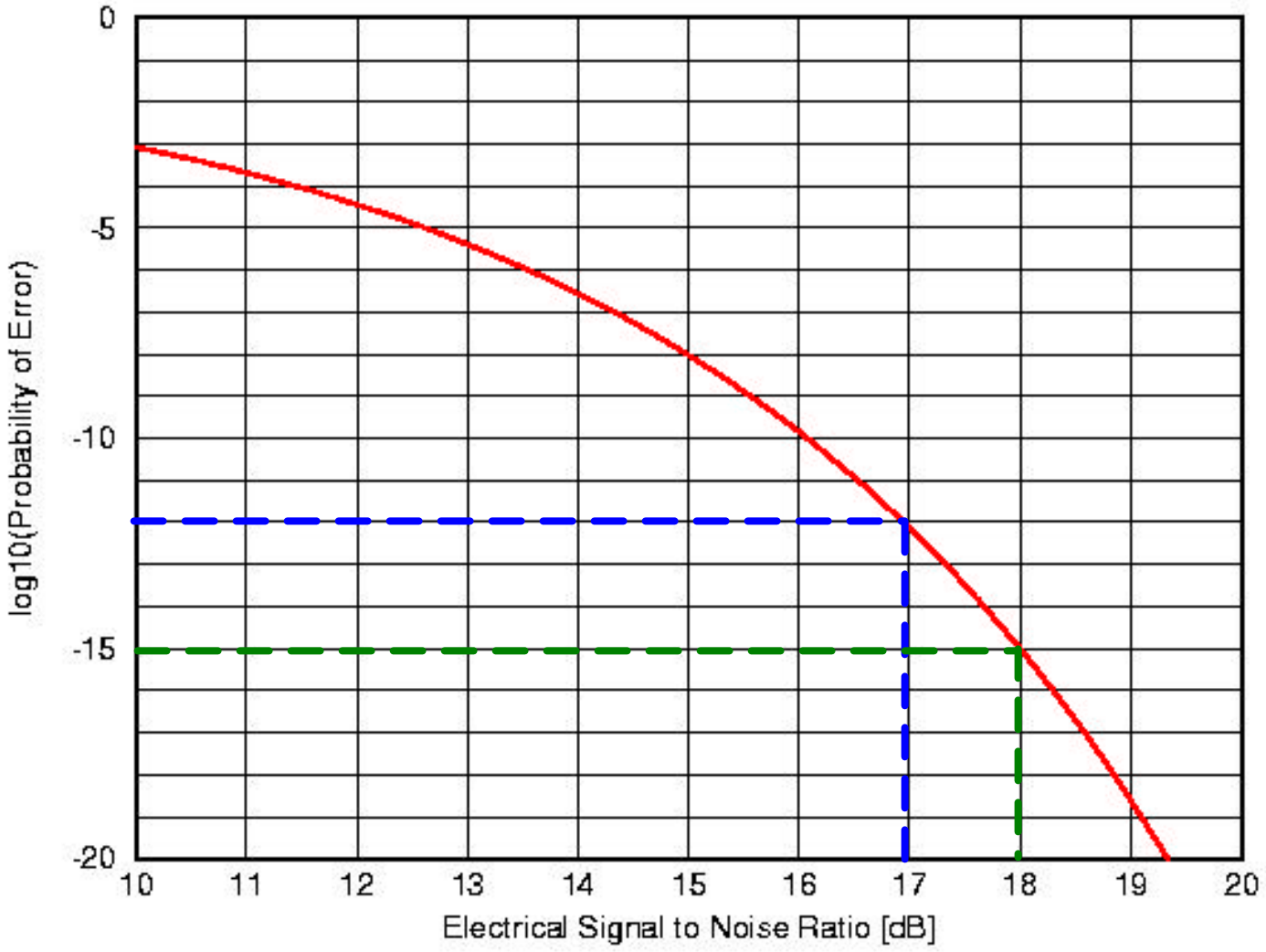
Assumptions in Simulations

- **The quasi-linear approximation (Ref.[1]) holds:**
  - ➢The optical power at the input of the receiver can be represented as the convolution of the transmitted bits with an impulse response that models the attenuation and dispersion of the fiber
  - ➢This requirement can be relaxed by using nonlinear equalization techniques
- **Any time variations of the channel response are sufficiently slow that they can be tracked by the adaptation algorithm:**
  - ➢The time constant of any time dependence of the channel response must be equal to or larger than 1 microsecond

Parameters of Simulations

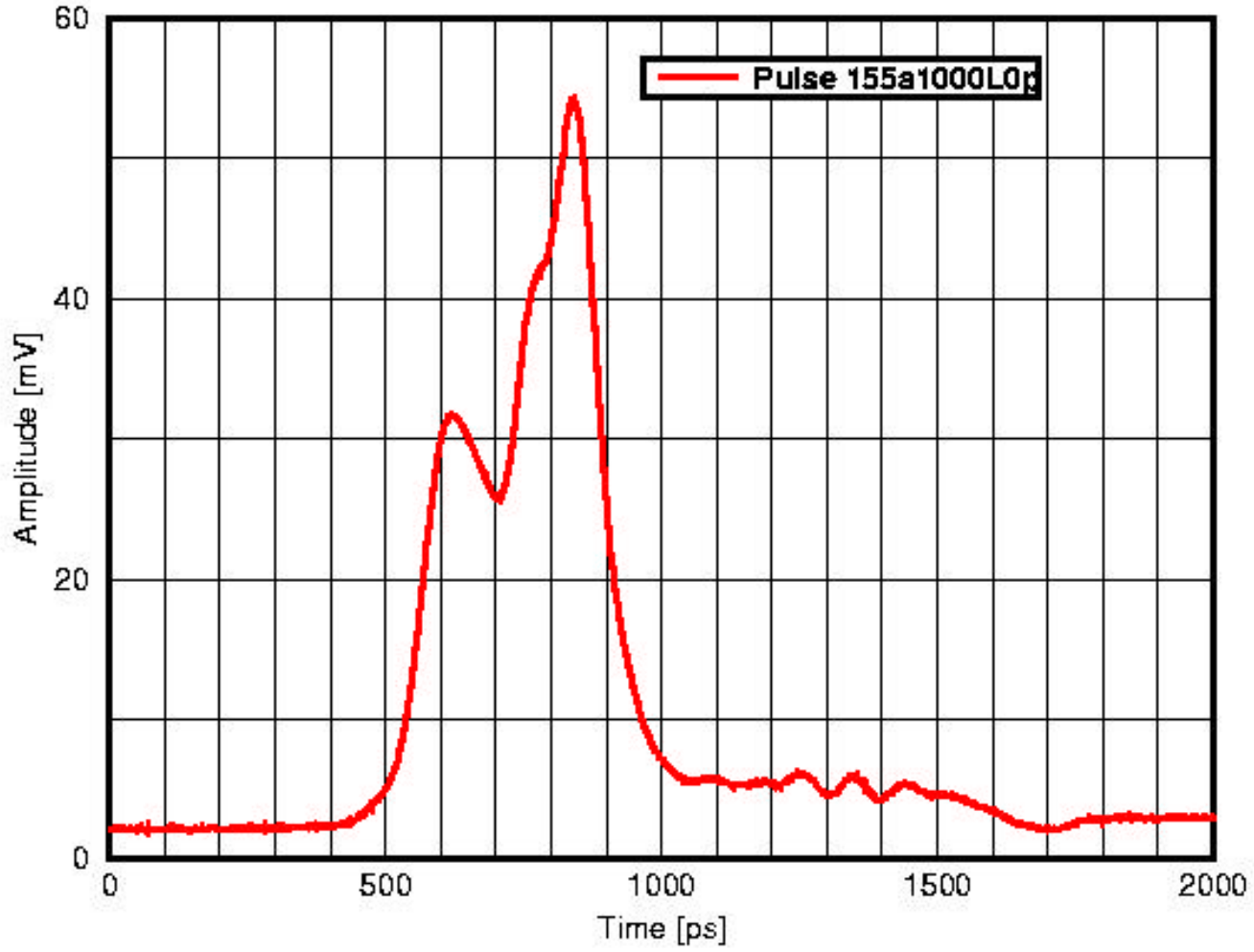
Symbol Rate (f_B)	10/3.125 Gbaud
Time Resolution of Simulation ($1/f_s$)	5ps
Rise and Fall Times of Tx. Pulse	35ps
Full-width at half maximum (FWHM)	65ps
TIA Bandwidth (f_l)	$0.75f_B$
TIA High-Pass Corner (f_h)	2MHz
Launch power	-9dBm
Responsivity of photodetector	0.7Amp/Watt
TIA Input-Referred Noise Current (includes RIN, modal noise, shot noise, and thermal noise of TIA)	1μA
Probability Density Function of the Noise	Gaussian
Power Spectral Density of the Noise	White
Number of FFE Taps	8
Number of DFE Taps	6

Error Rate vs. Electrical SNR for Binary Modulation



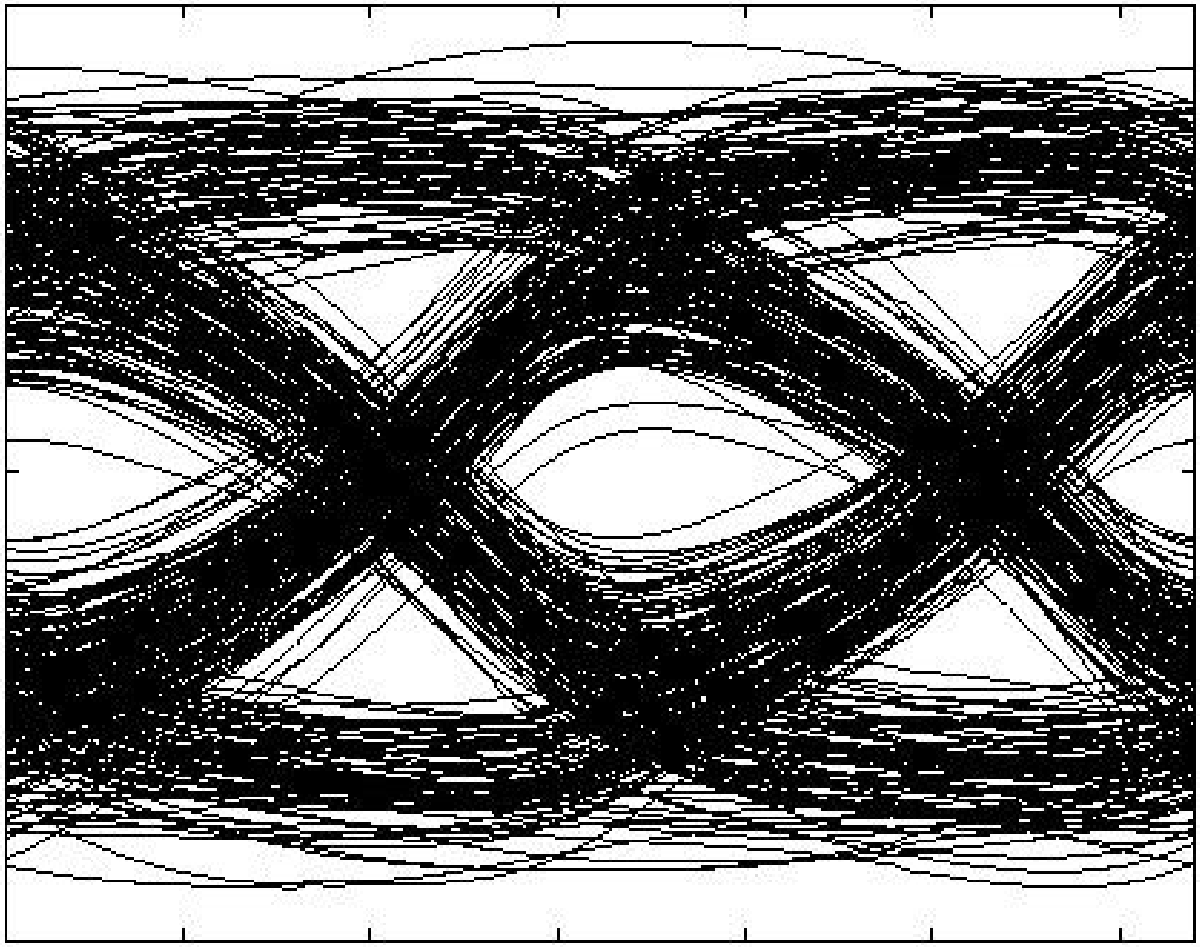
Fiber Impulse Response

(An example of DMD pulse from 802.3z database; 1310nm, 320m MMF)



Eye Pattern at Input of A/D (3.125Gb/s)

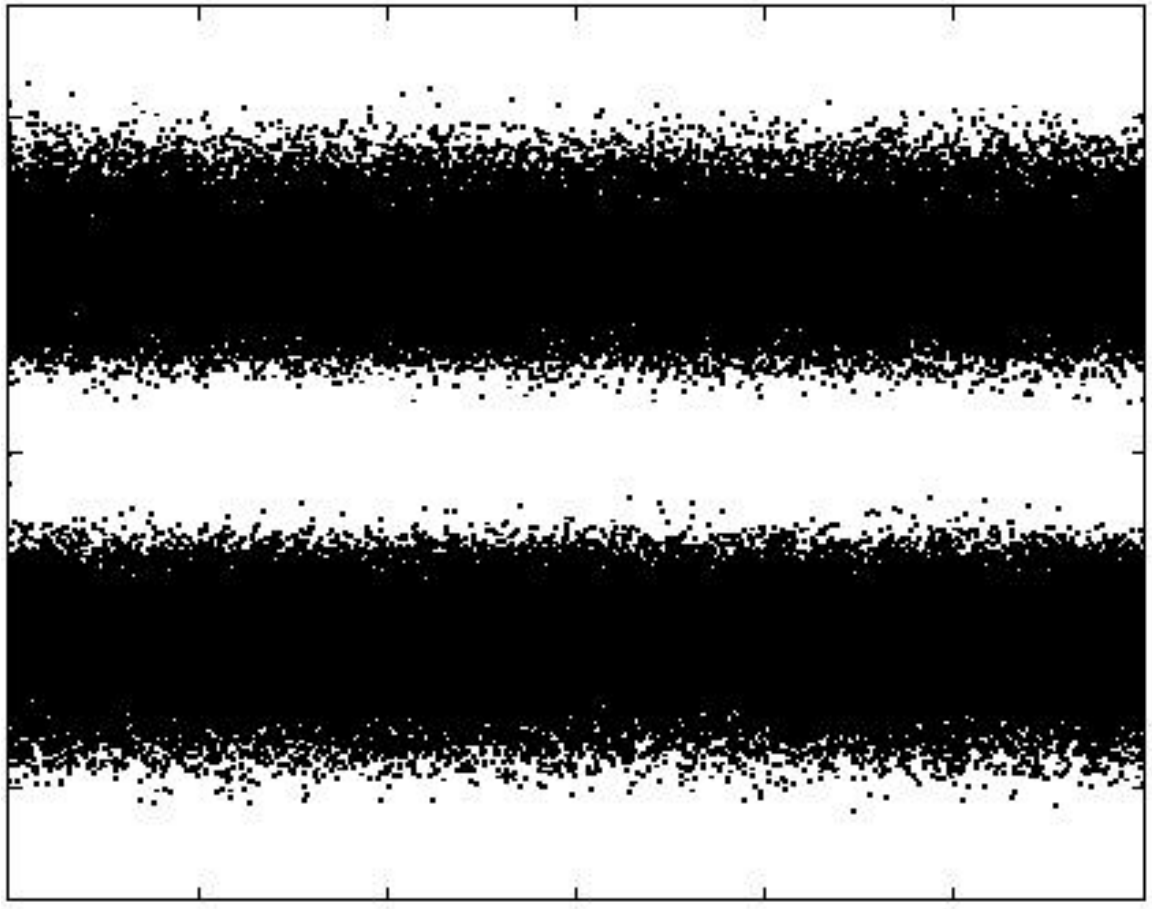
(An example of DMD pulse from 802.3z database; 1310nm, 320m MMF)



Test Point A

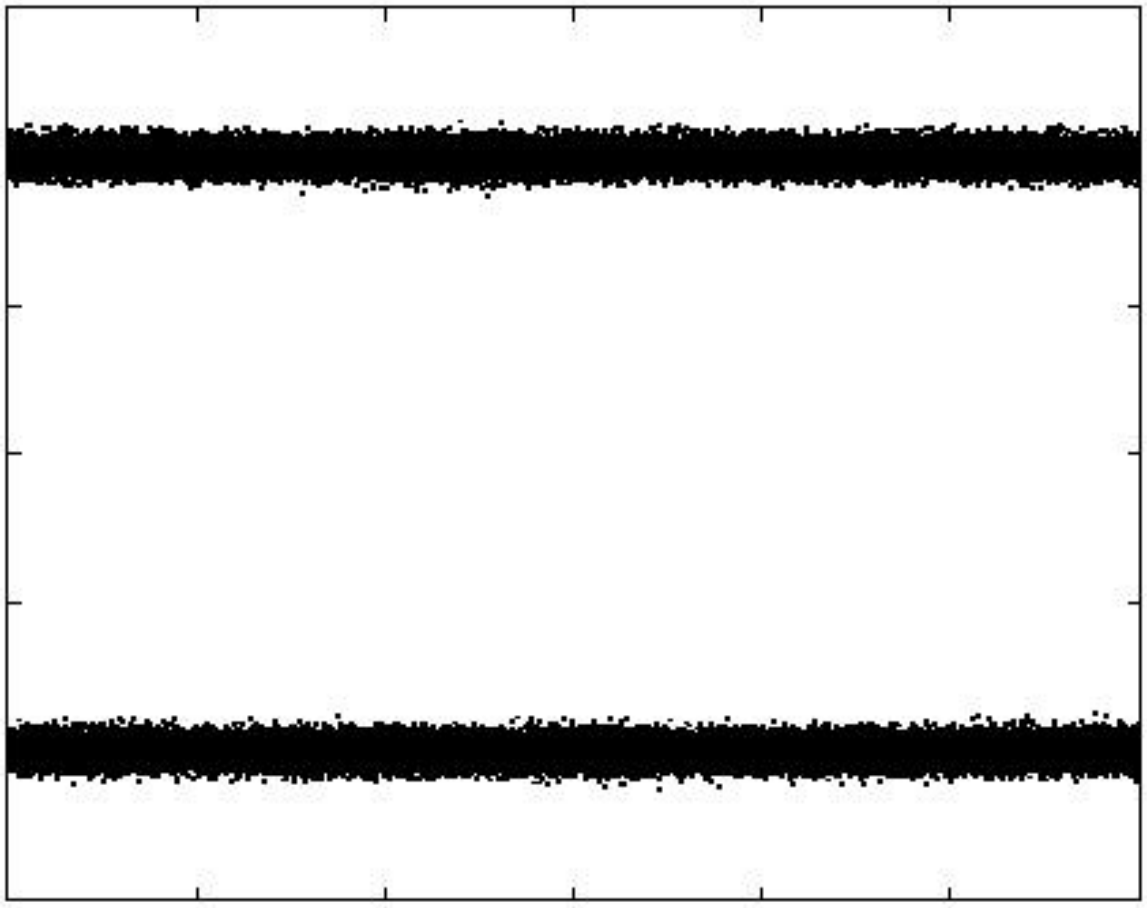
Eye Pattern at Output of A/D (3.125Gb/s)

(An example of DMD pulse from 802.3z database; 1310nm, 320m MMF)



Test Point B

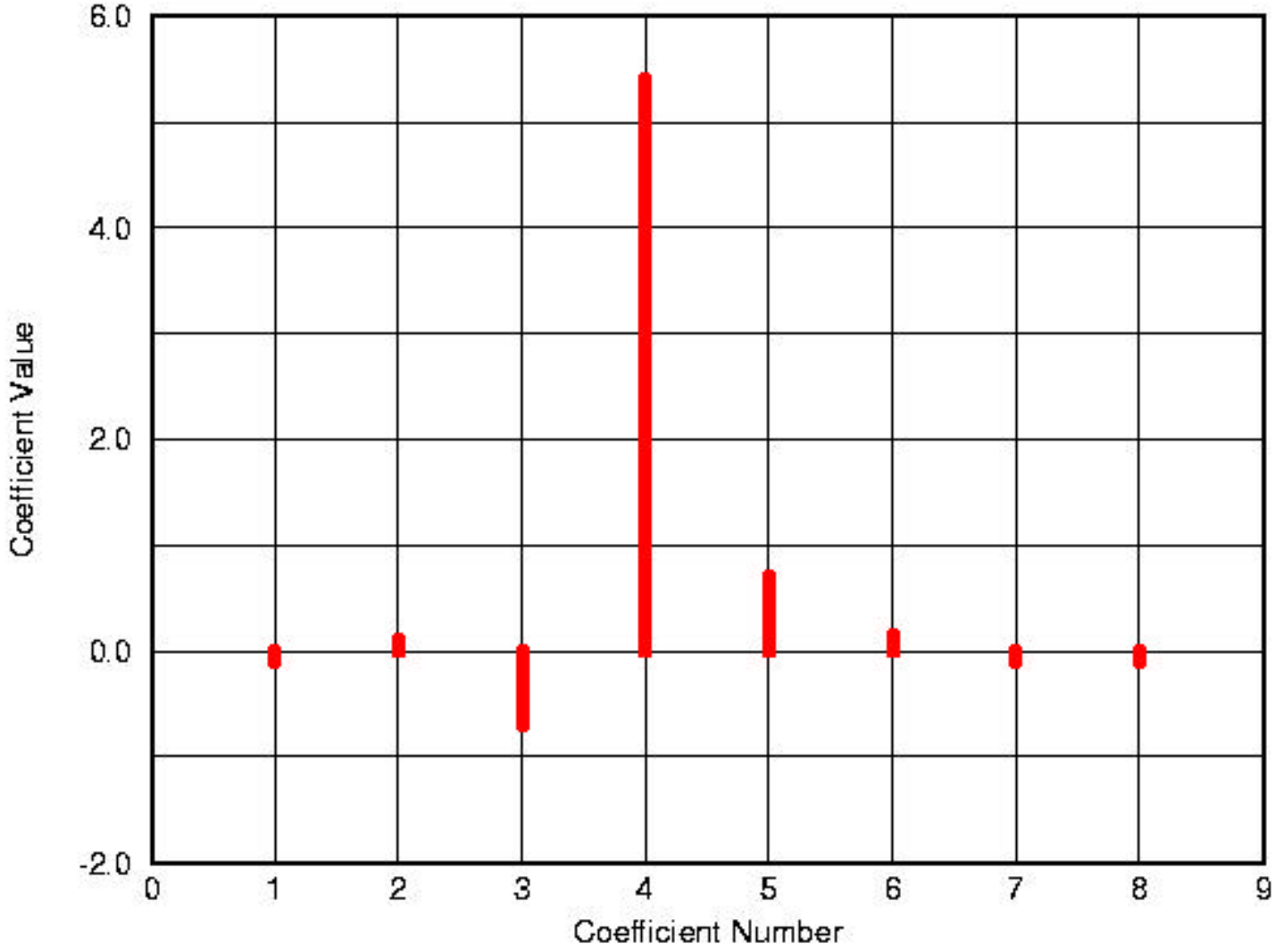
Equalized Eye Pattern at Input of Slicer (3.125Gb/s)
(An example of DMD pulse from 802.3z database; 1310nm, 320m MMF)



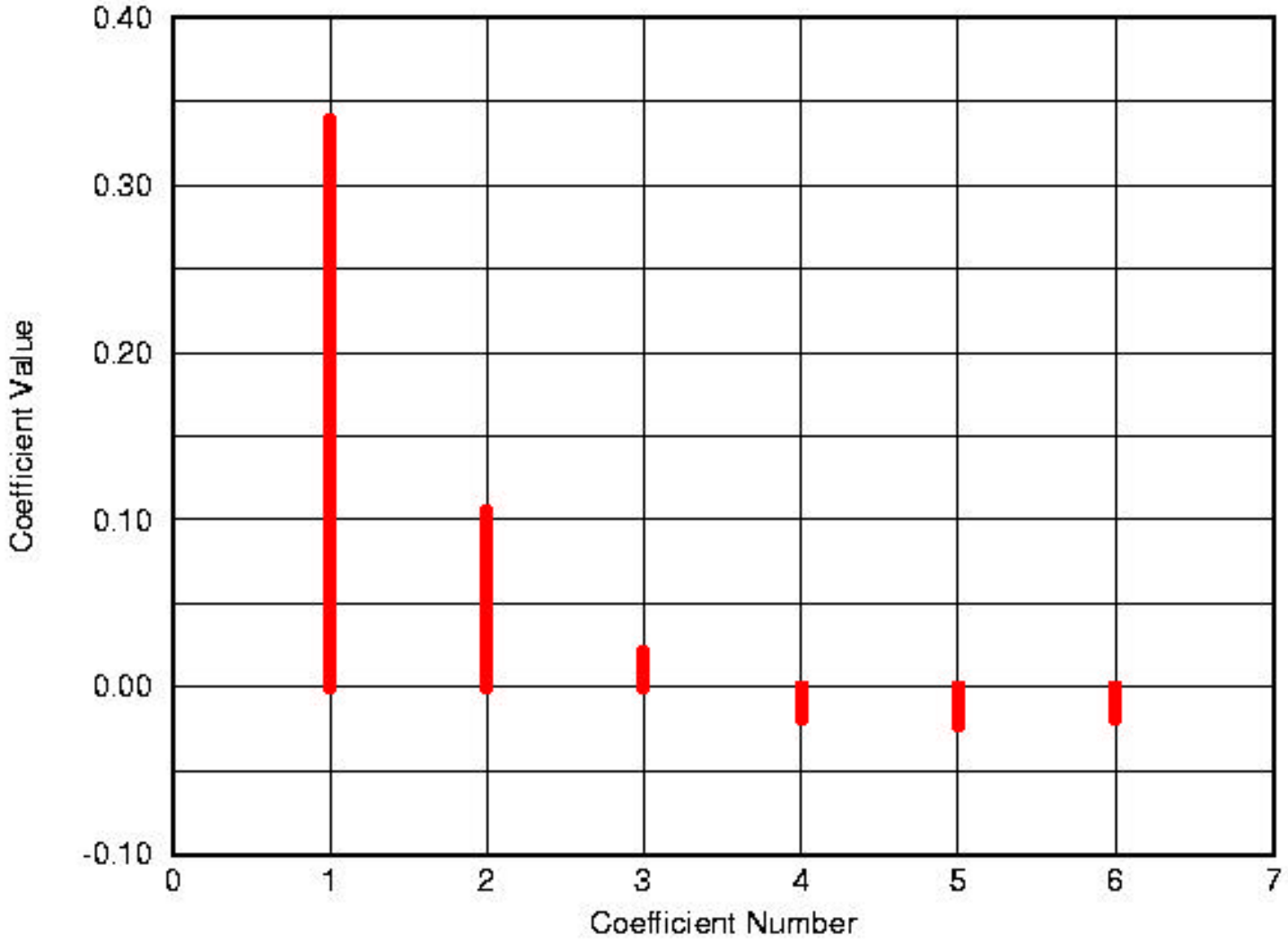
Test Point C

SNR at the Slicer = 28dB - BER <<

FFE Coefficients - 3.125Gb/s

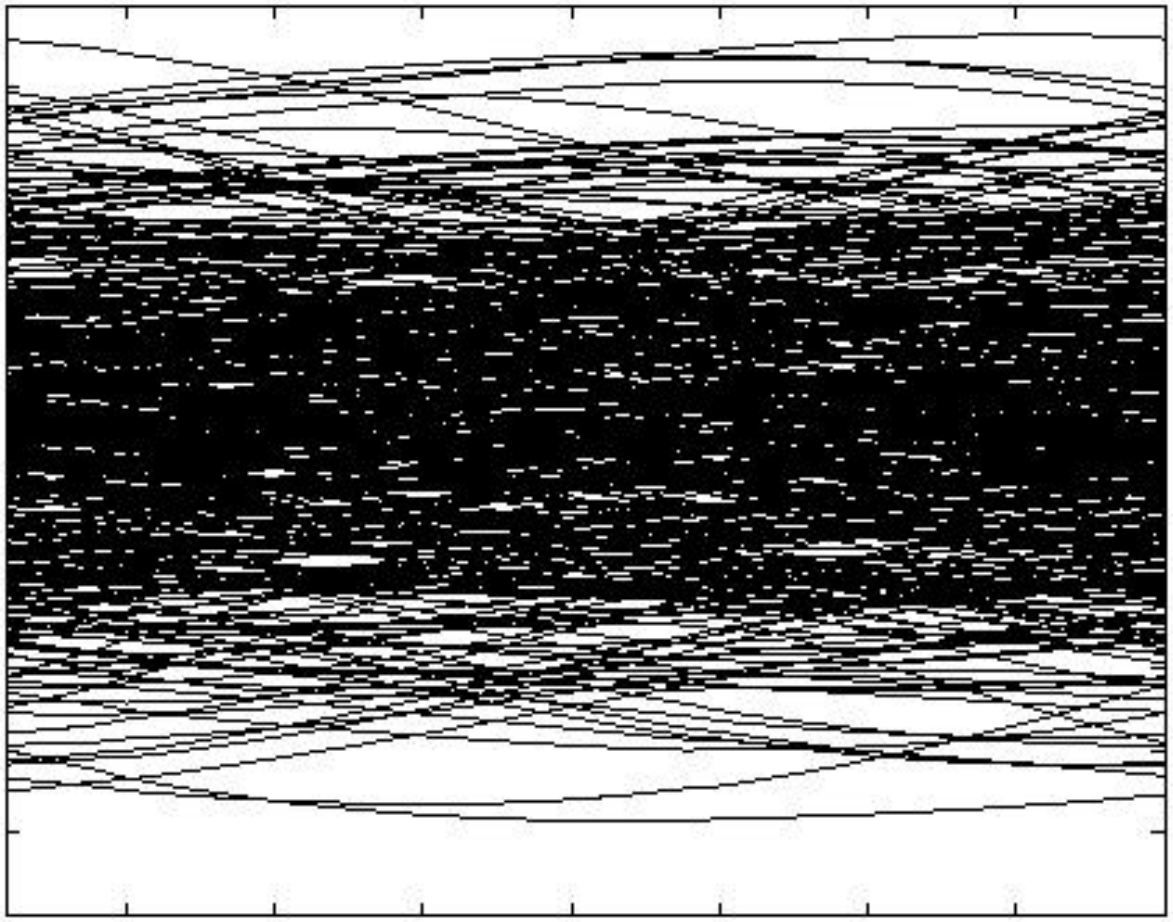


DFE Coefficients - 3.125Gb/s



Eye Pattern at Input of A/D (10Gb/s)

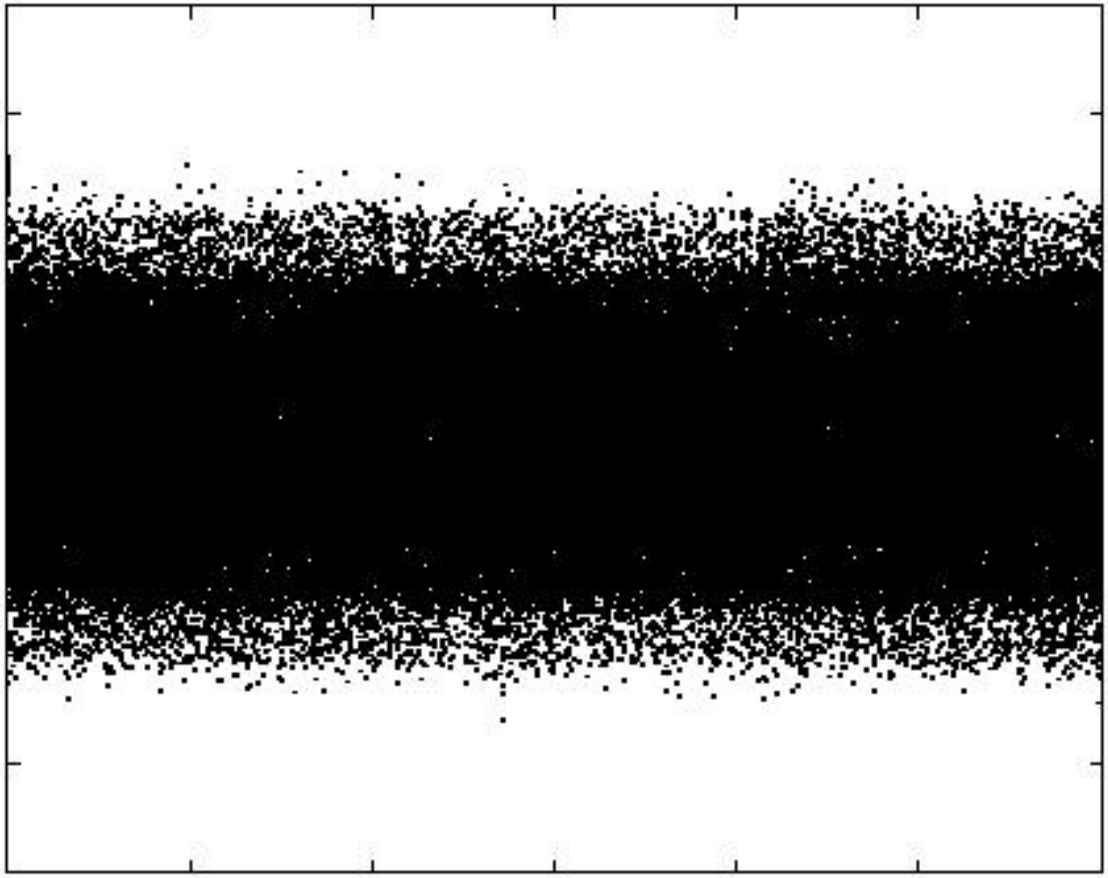
(An example DMD pulse from 802.3z database; 1310nm, 320m MMF)



Test Point A

Eye Pattern at Output of A/D (10Gb/s)

(An example of DMD pulse from the 802.3z database; 1310nm, 320m MMF)



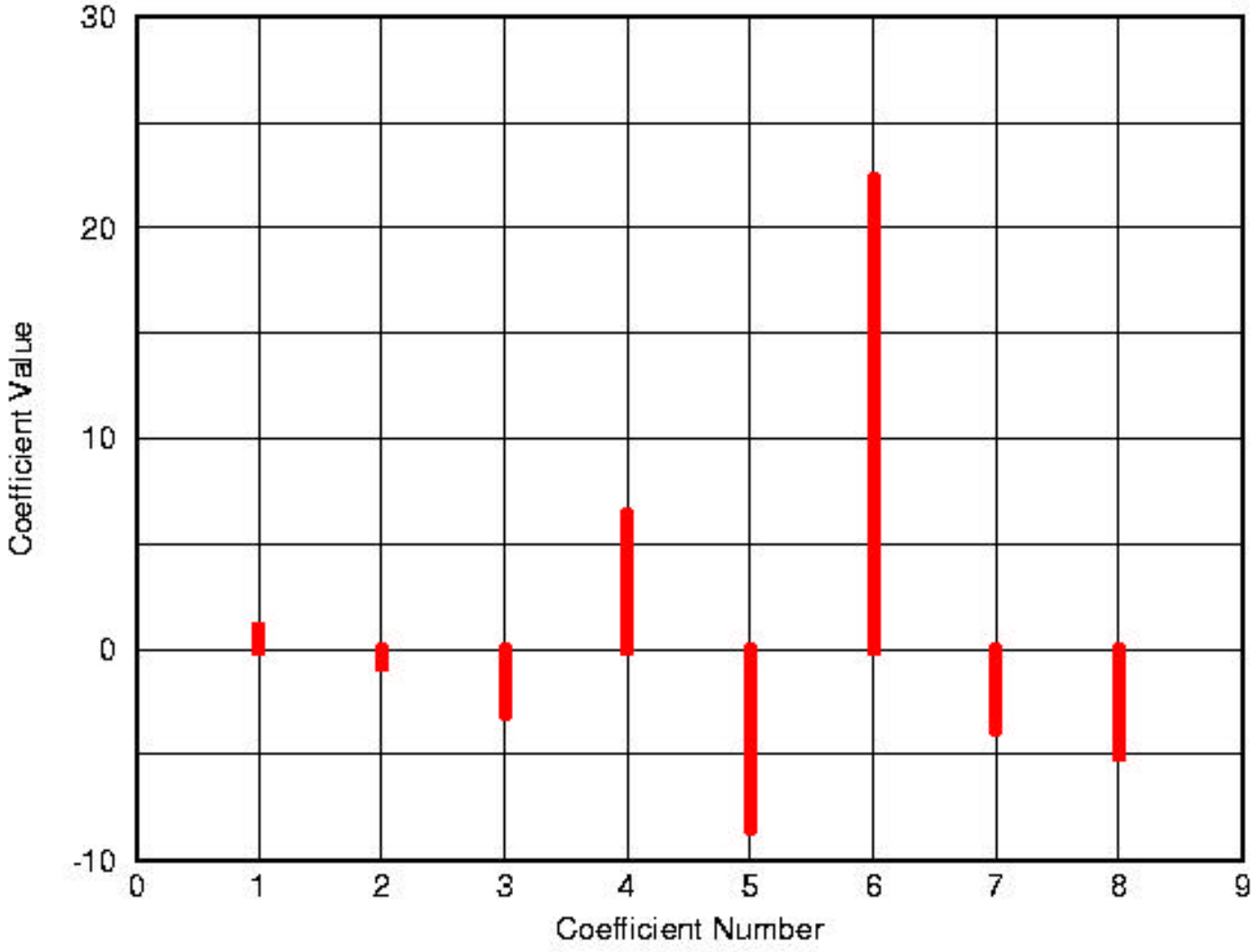
Test Point B

Equalized Eye Pattern at Input of Slicer (10Gb/s)
(An example of DMD pulse from the 802.3z database; 1310nm, 320m MMF)

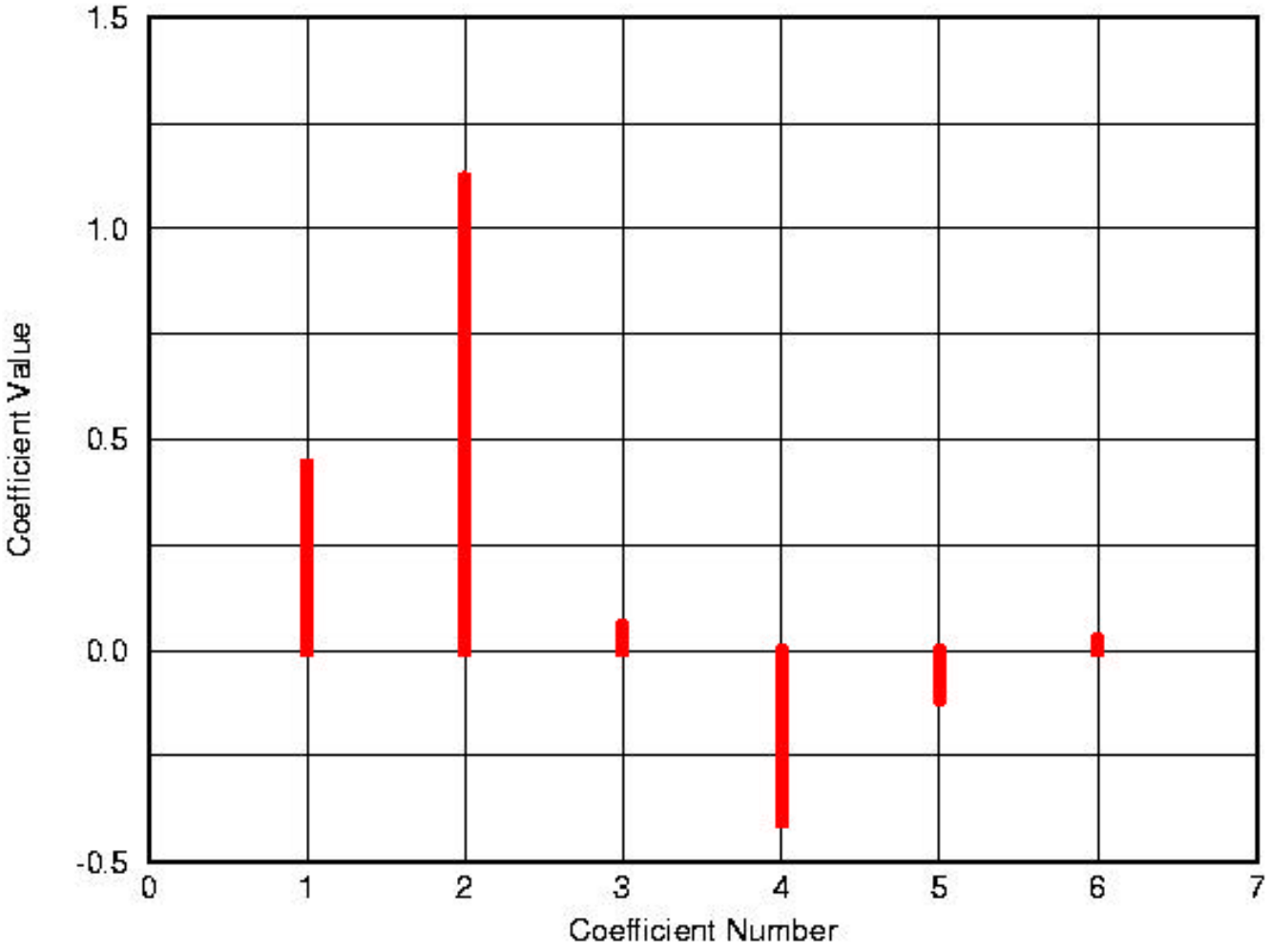
Test Point C

SNR at the Slicer = 19dB - BER = 10^{-19}

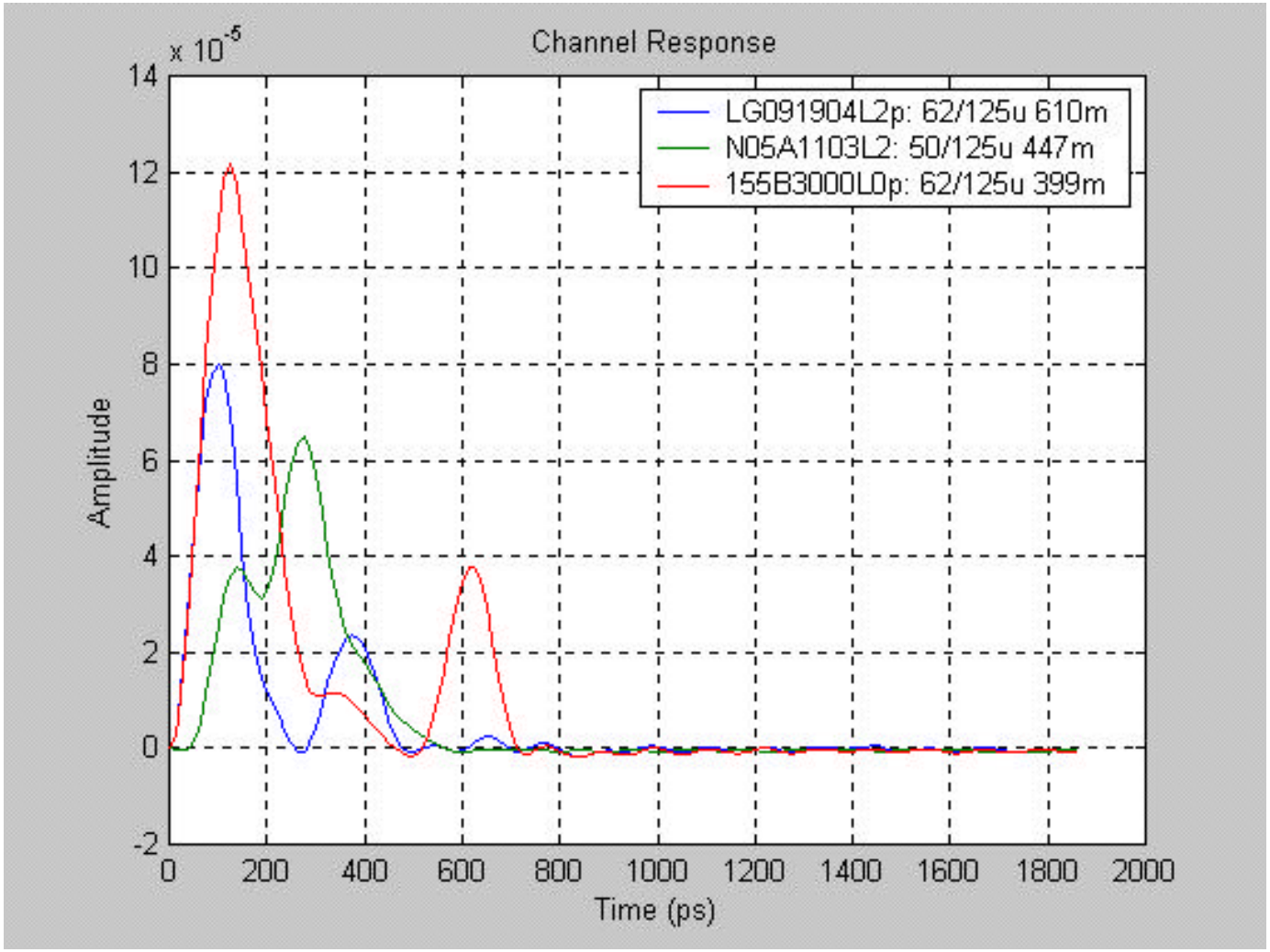
FFE Coefficients - 10Gb/s



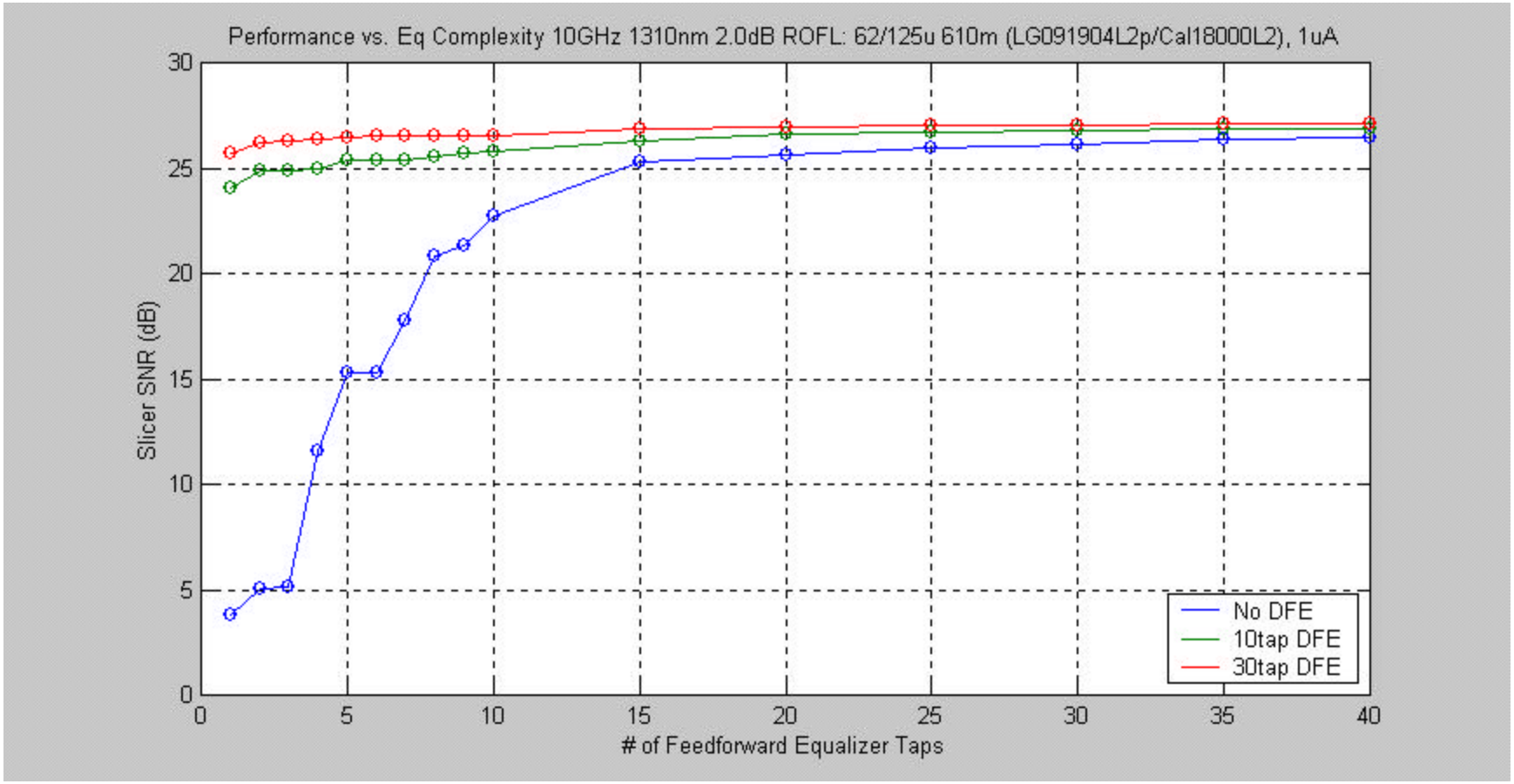
DFE Coefficients - 10Gb/s



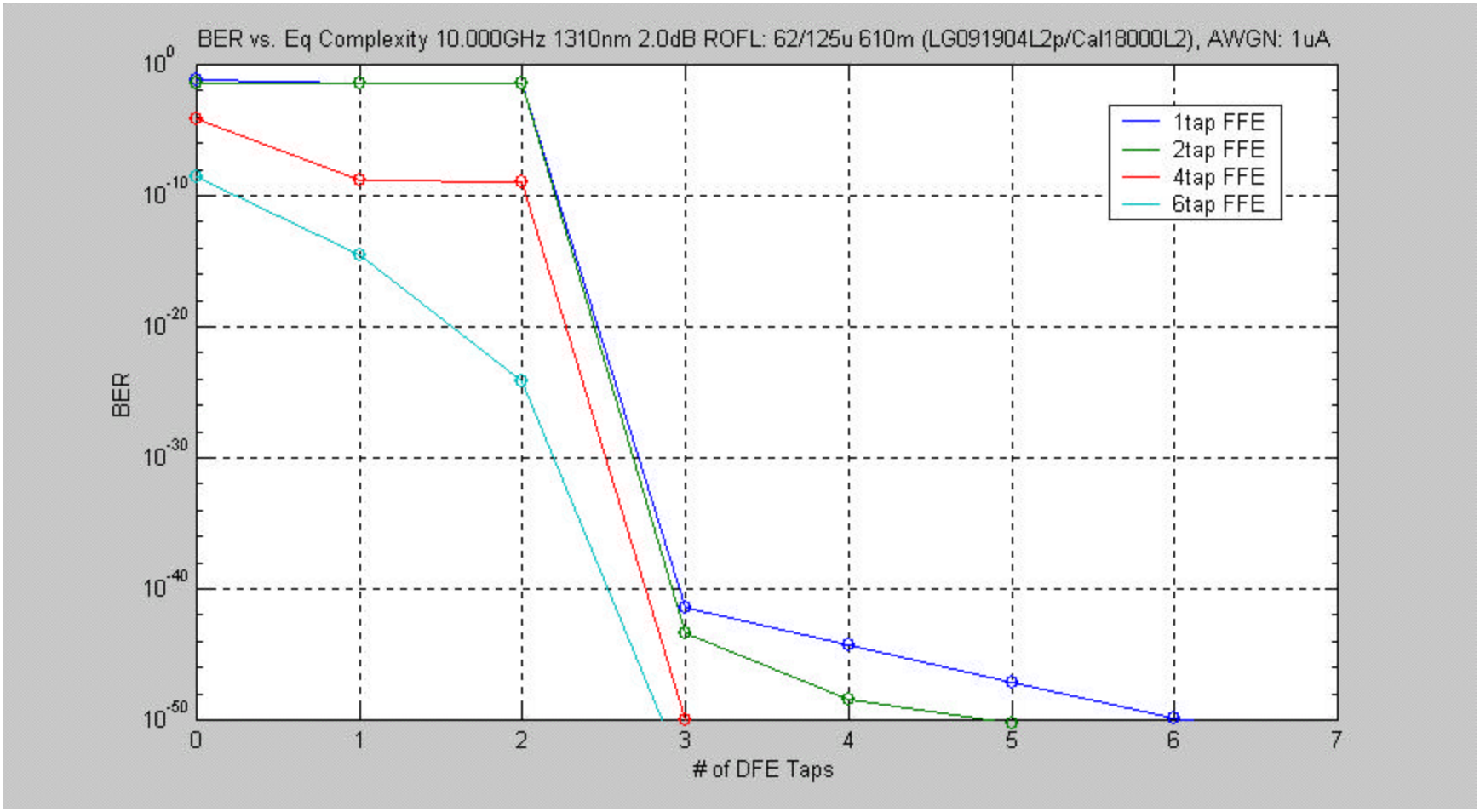
DMD Channel Response



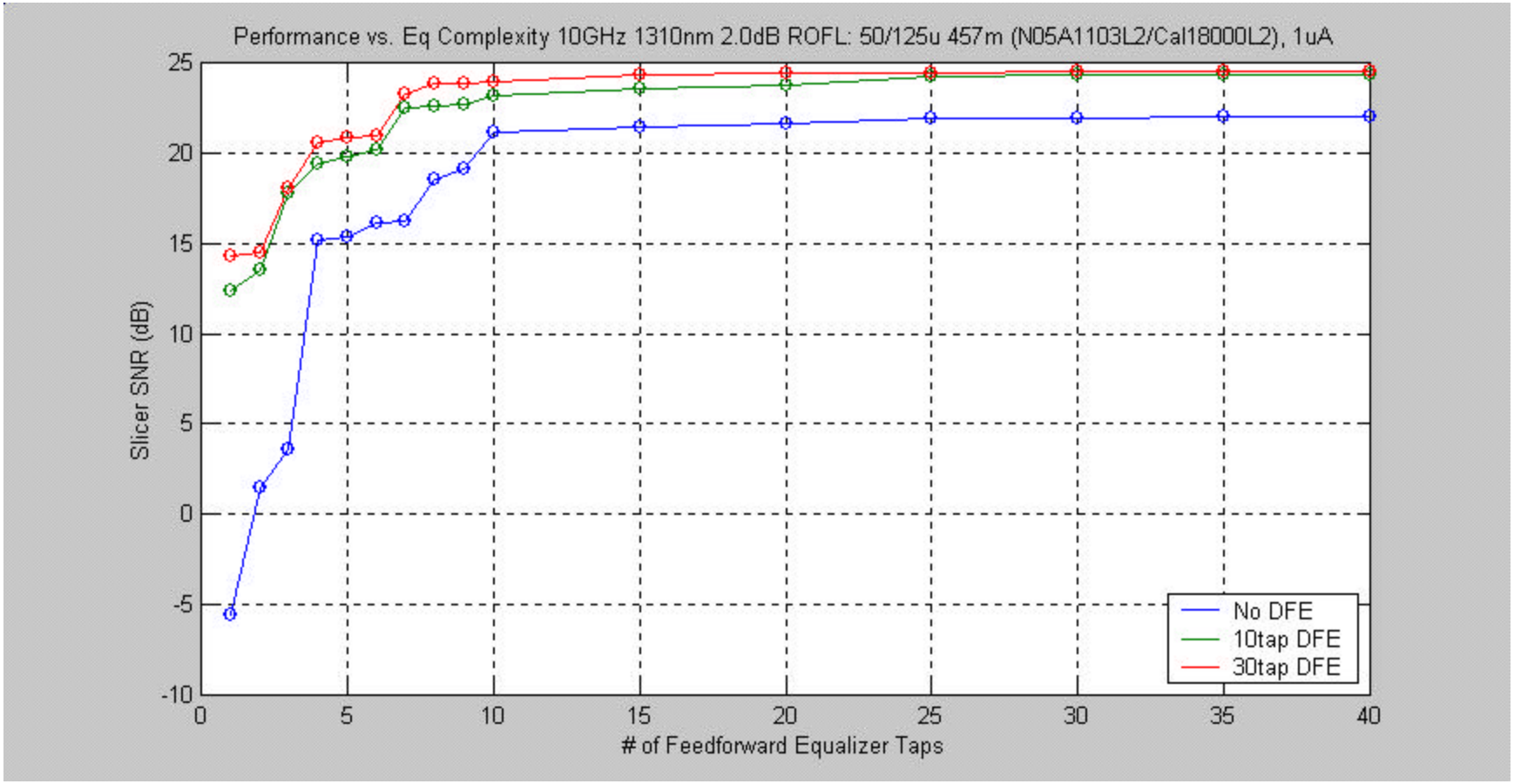
62/125u MMF, 610m, 10GHz
(ID LG091904)



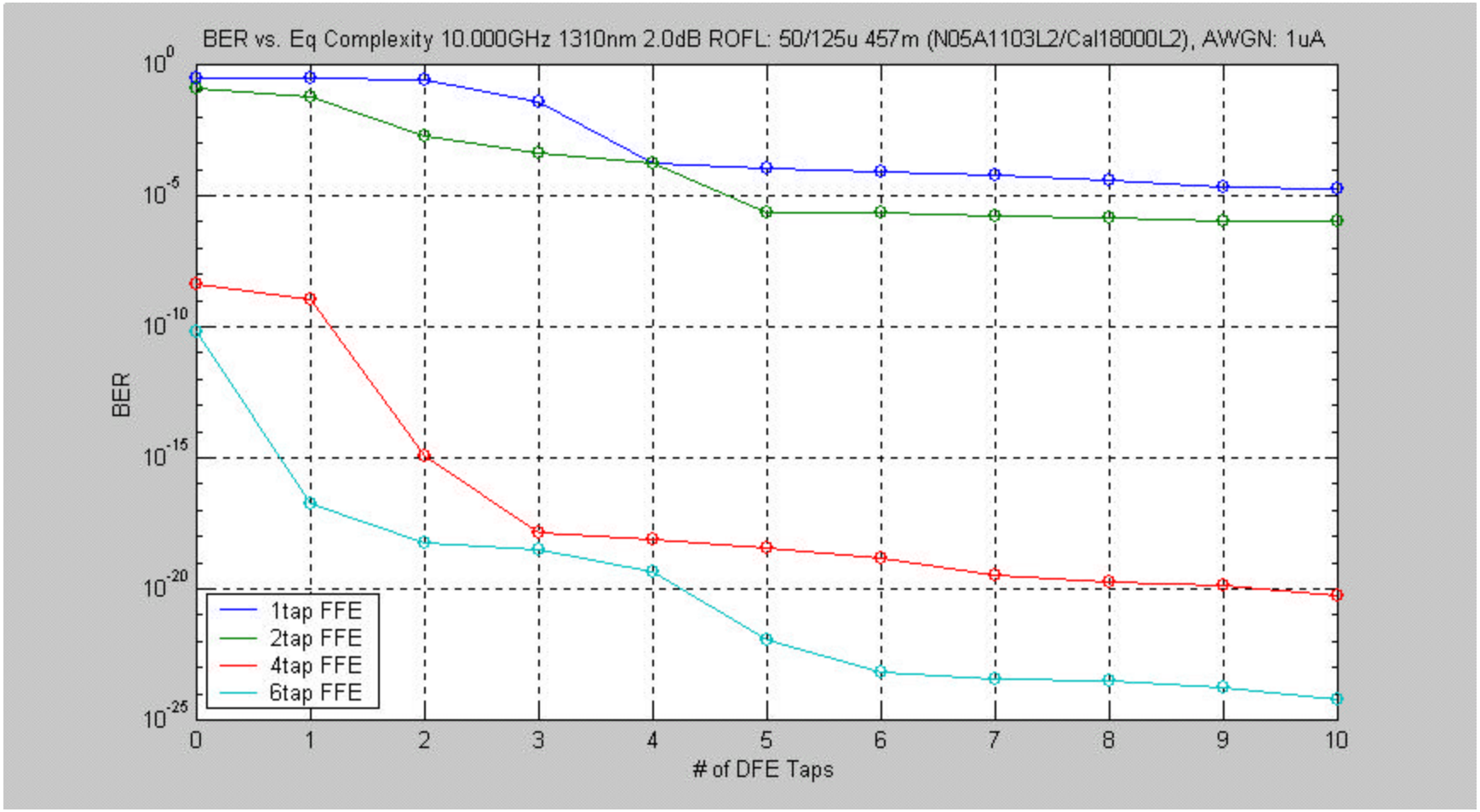
62/125u MMF, 610m, 10GHz
(ID LG091904)



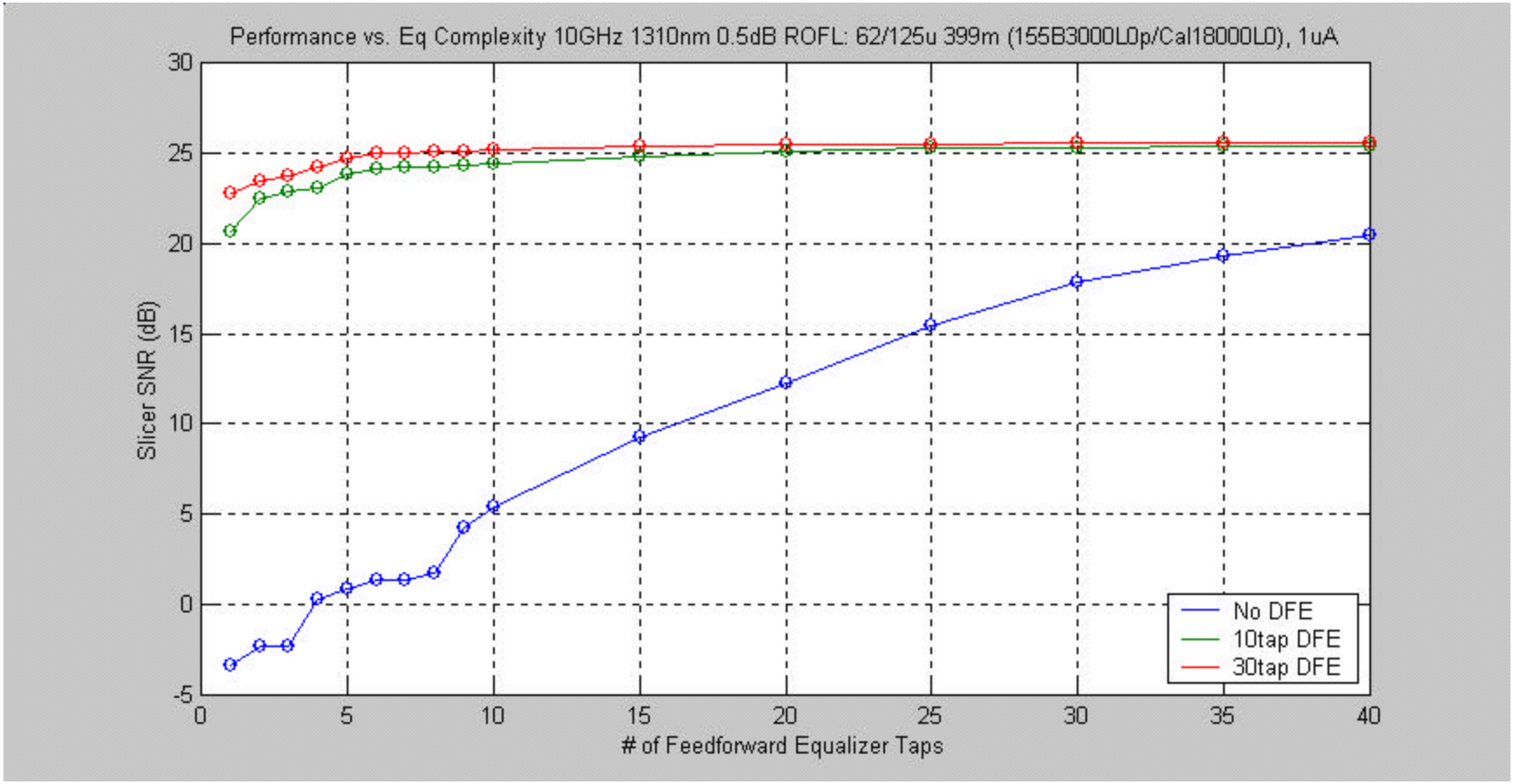
50/125u MMF, 457m, 10GHz
(ID N05A1103)



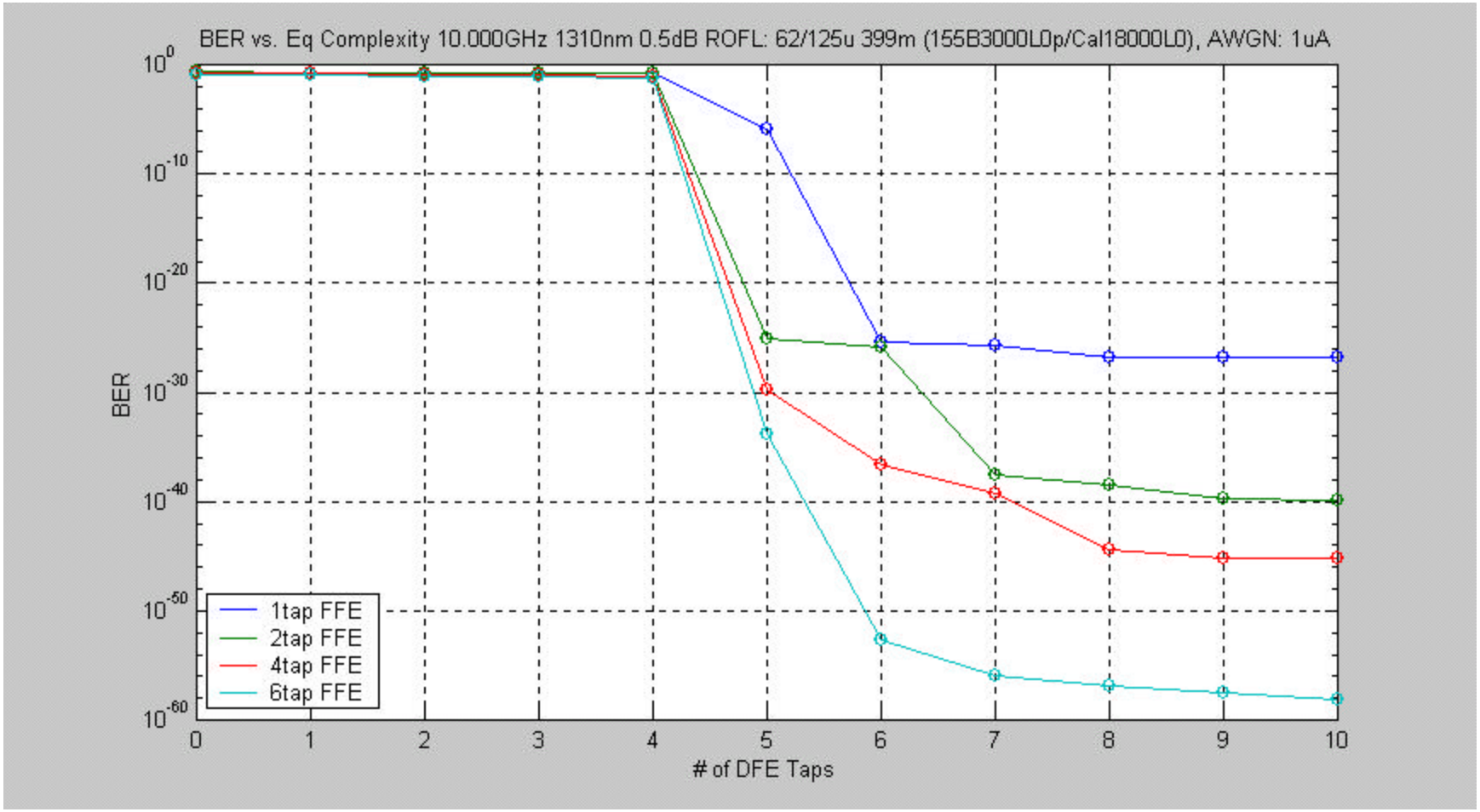
50/125u MMF, 457m, 10GHz
(ID N05A1103)



62/125u MMF, 399m, 10GHz
(ID 155B3)



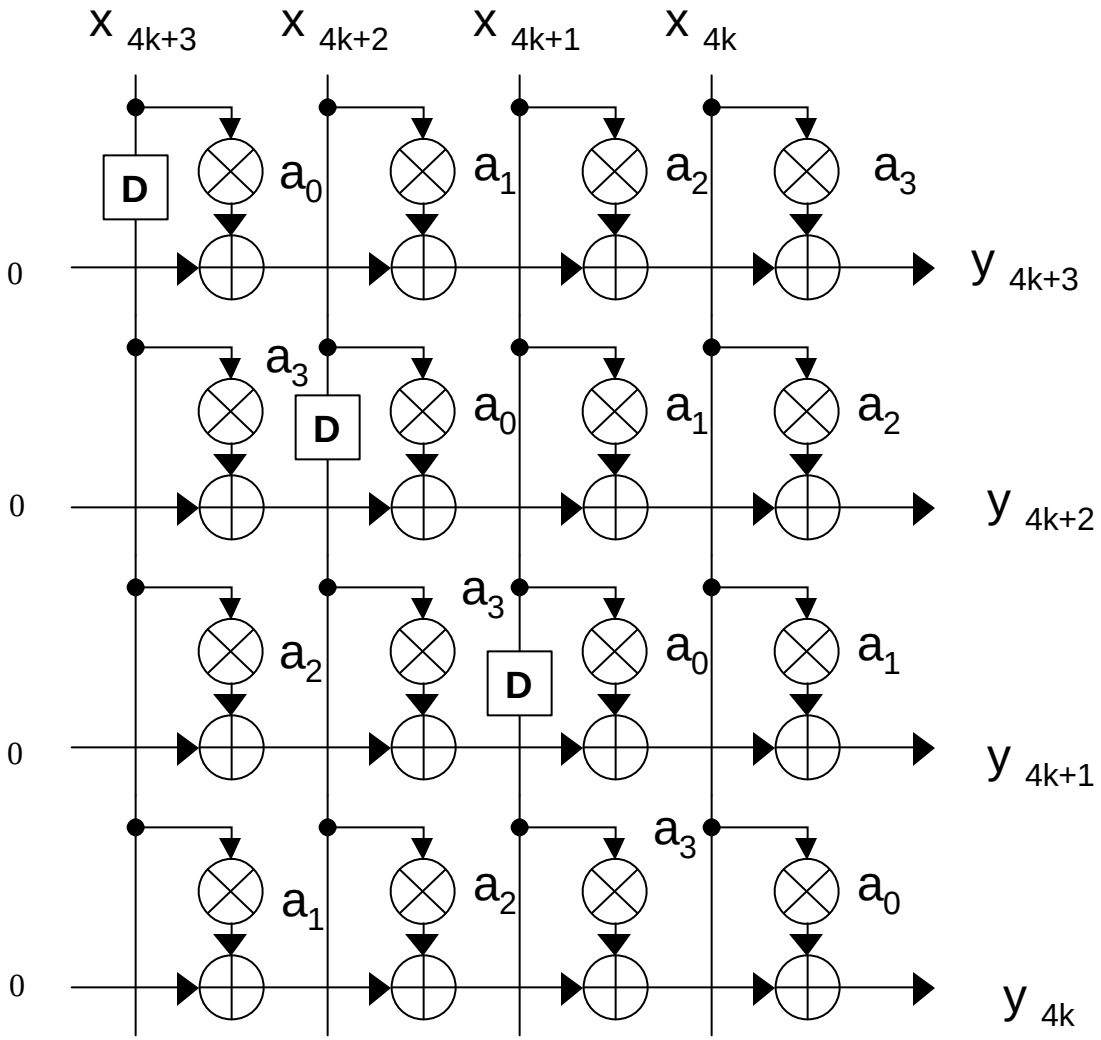
62/125u MMF, 399m, 10GHz
(ID 155B3)



VLSI Implementation

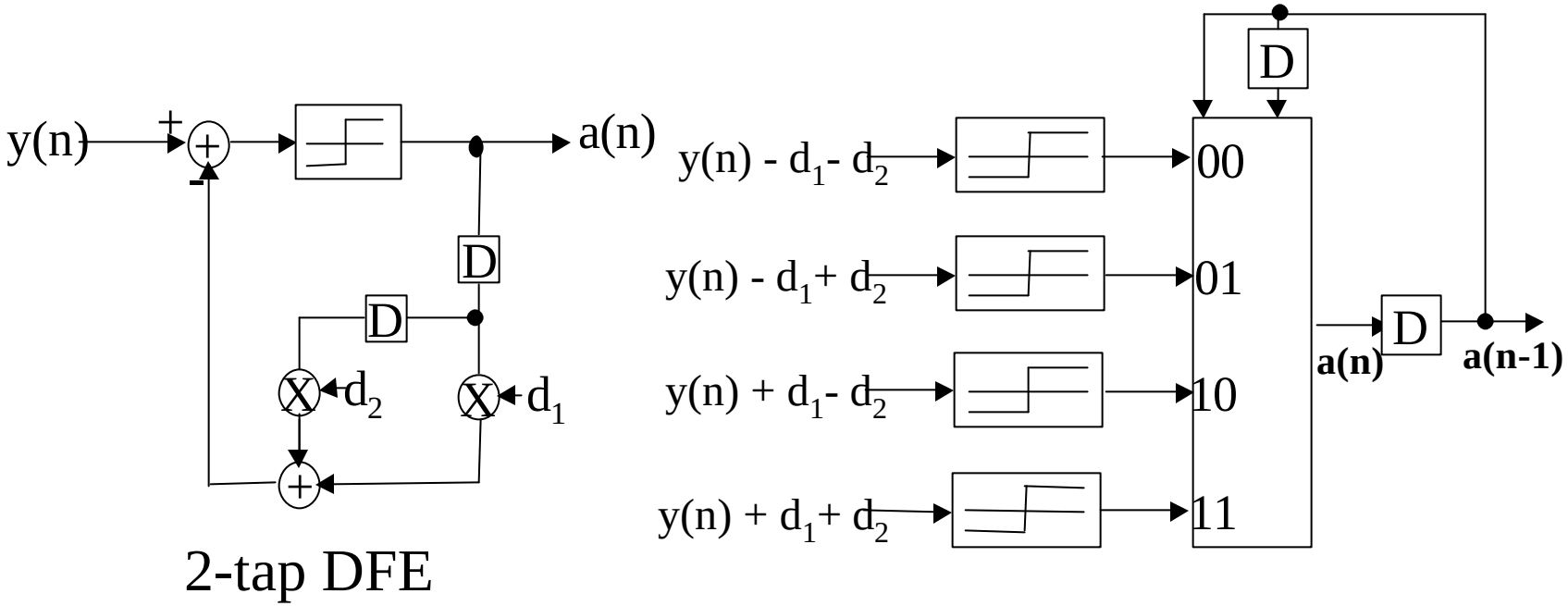
- Parallel FFE (Straightforward)
- DFE parallelization requires loop reformulation followed by application of look-ahead
- 8 FFE and 6 DFE taps assumed. This is the same number used in the simulations reported in slides 11 through 20. No attempt was made to optimize the number of taps
- Interleaved A/D converter
- Power and area estimates

4-Parallel 4-Tap FIR Filter



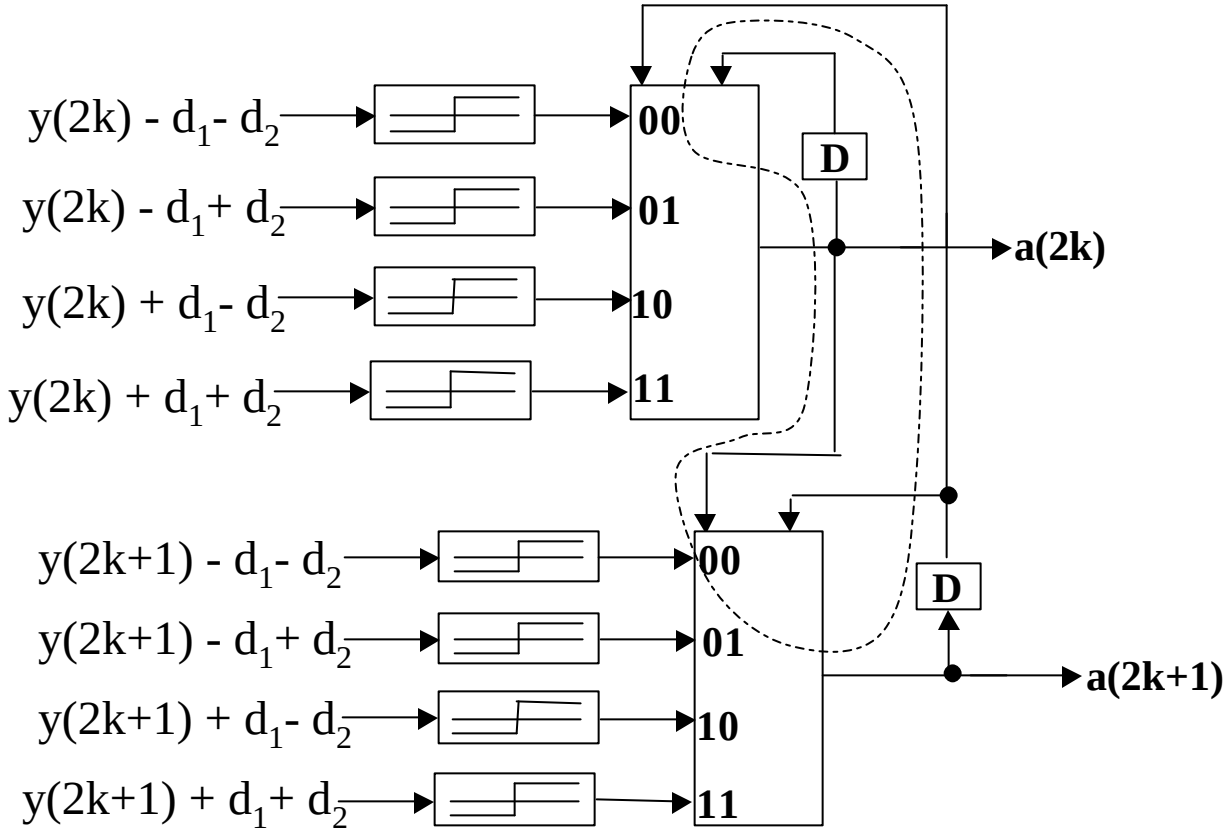
$$y(n) = a_0\, x(n) + a_1\, x(n-1) + a_2\, x(n-2) + a_3\, x(n-3)$$

DFE Loop Reformulation



- Complexity grows as 2^N for a N-tap DFE.
- Speed inherently limited by 2-to-1 MUX (typically 0.2ns in 0.13μ). (See Parhi, 1991 [2] and Kasturia et.al., 1991 [3])

2-Parallel Implementation



- Complexity ~ L 2^N for L-Parallel and N-tap DFE.
- Speed bounded by L multiplexers (L ≤ 5 for 1GHz clock).

Look-Ahead

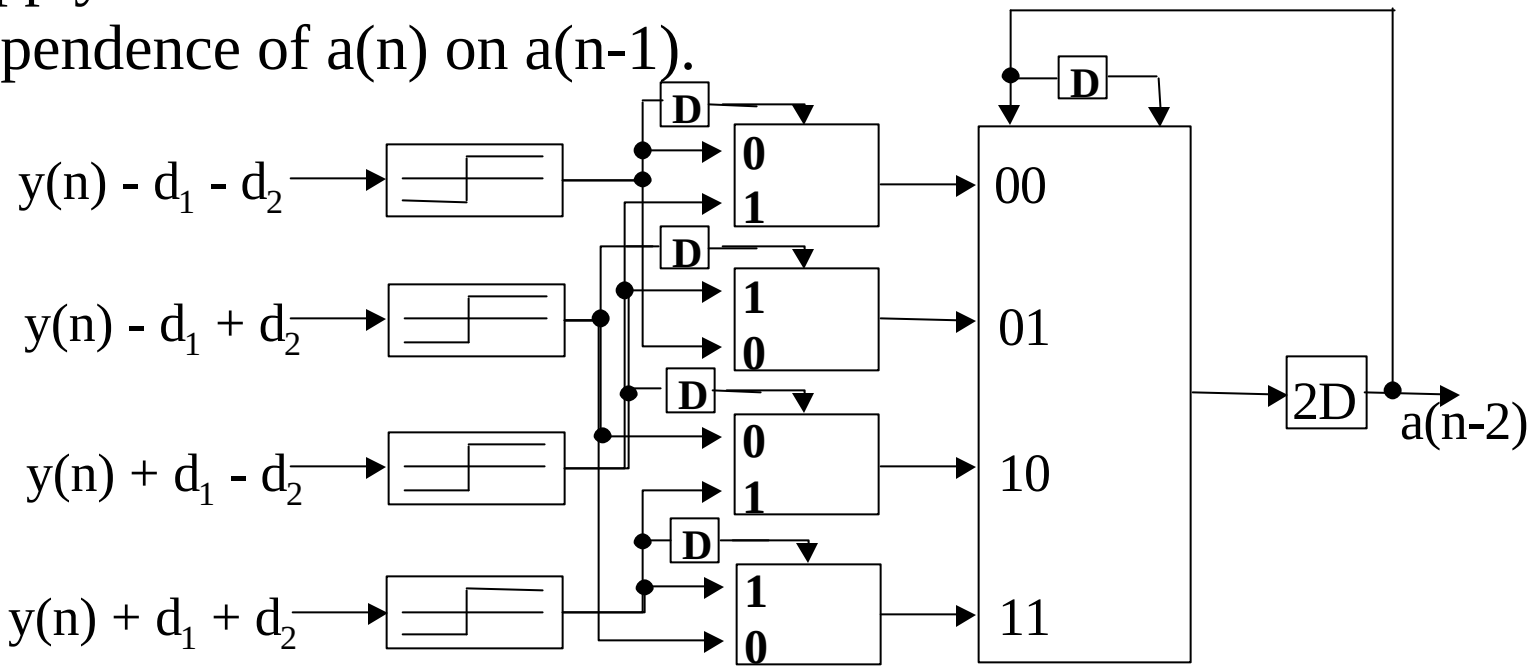
$$a(n) = f_1(n)\overline{a}(n-1)\overline{a}(n-2) + f_2(n)\overline{a}(n-1)a(n-2) + f_3(n)a(n-1)\overline{a}(n-2) + f_4(n)a(n-1)a(n-2)$$

$$= [f_1(n)\overline{f_1}(n-1) + f_3(n)f_1(n-1)]\ \overline{a}(n-2)\overline{a}(n-3) + [f_1(n)\overline{f_2}(n-1) + f_3(n)f_2(n-1)]\ \overline{a}(n-2)a(n-3) + [f_2(n)\overline{f_3}(n-1) + f_4(n)f_3(n-1)]\ a(n-2)\overline{a}(n-3) + [f_2(n)\overline{f_4}(n-1) + f_4(n)f_4(n-1)]\ a(n-2)a(n-3)$$

- One step of look-ahead requires one column of multiplexers.
- Obtained by substituting expressions for a(n-1) and $\overline{a}(n-1)$ in terms of a(n-2) and a(n-3).

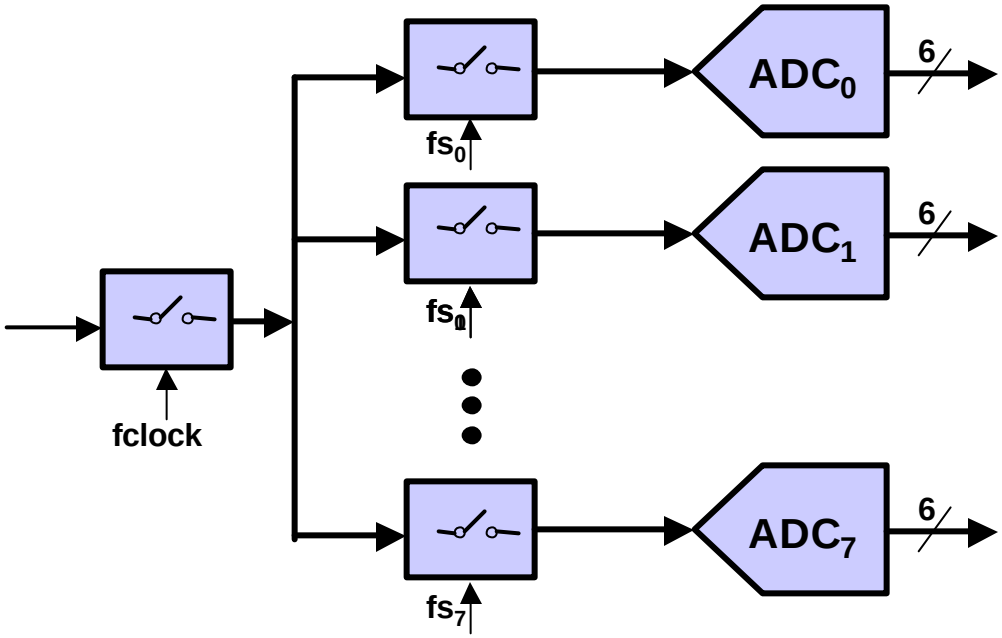
Highly Parallel Implementation

- Apply Look-Ahead to Reformulated DFE and eliminate dependence of a(n) on a(n-1).



- When unfolded or unrolled by factor 2 leads to 2-parallel architecture with a critical path of 1 multiplexer delay.
- Loop critical path = L/2 multiplexer delays.
- Attractive for L ≤ 10 for a critical path to be less than 5 MUX delays.

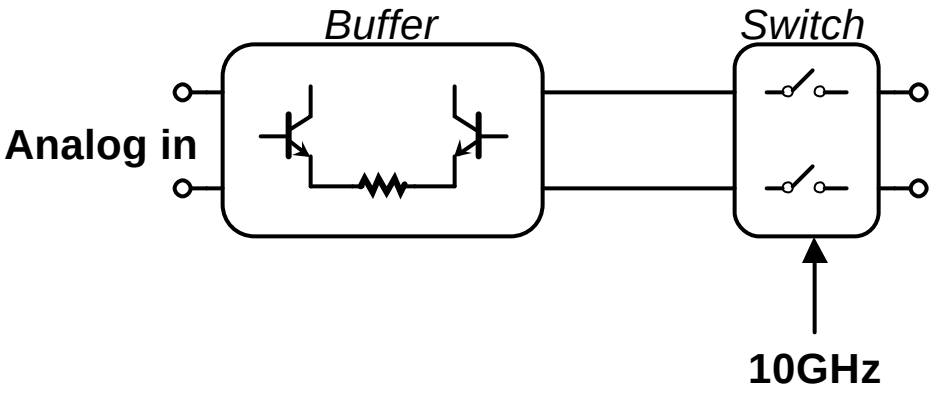
6-bit, Interleaved ADC



- **First T/H determines the dynamic performance of the ADC**
  - ➢Samples at 10GHz.
  - ➢Need at least 6-bits of precision.
- **Gain and offset errors between the channels are digitally corrected.**

10-GHz Track & Hold

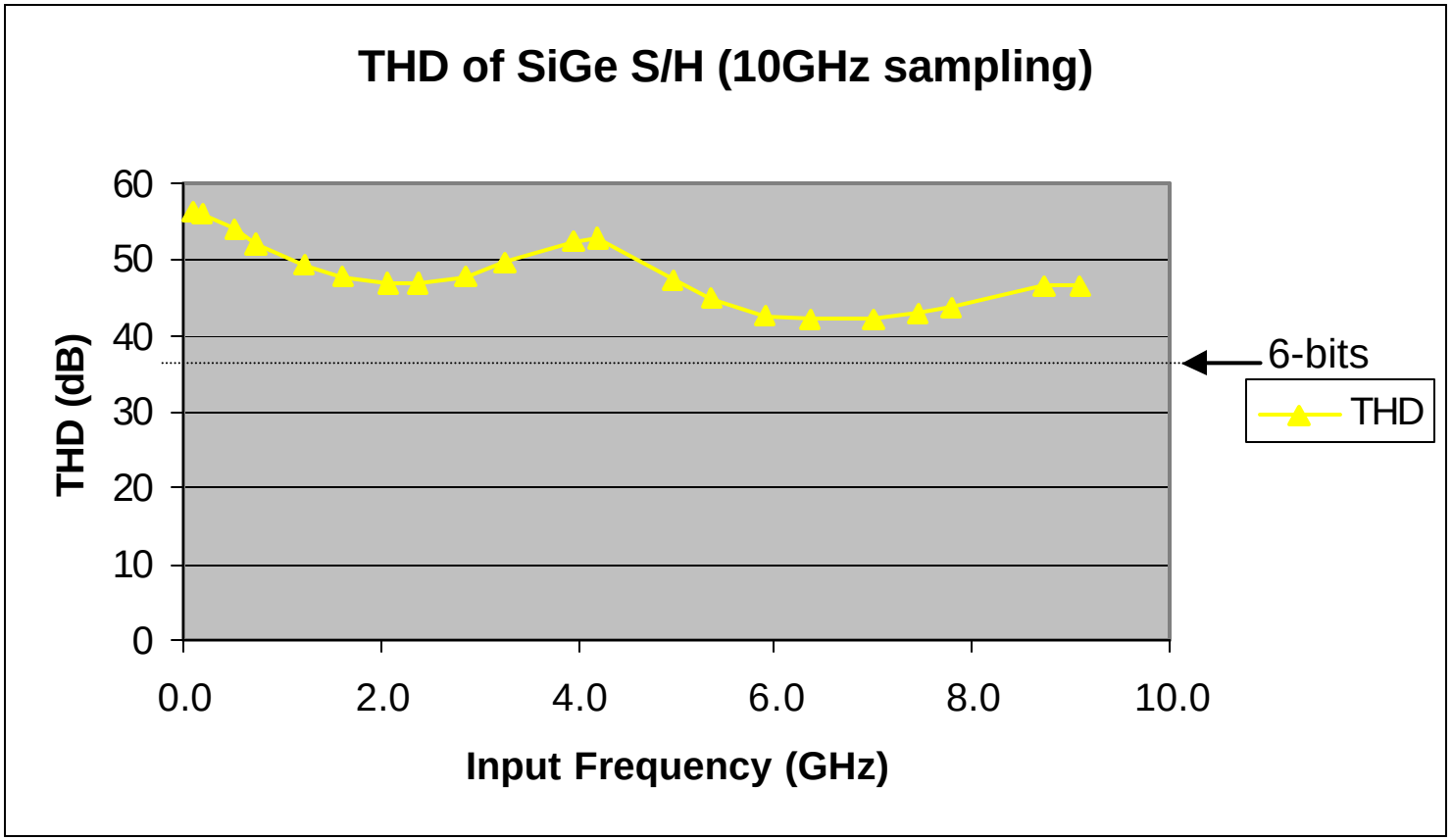
- **Required 6bits of S/(N+D)**
- **Makes the ADC sample a 'held' signal**
  - ➢Significantly relieves the dynamic requirements of the ADC.



Technology:

- **90GHz peak-f_T SiGe technology**
- **0.18u linewidth**
- **1.8V supply**

Simulated Performance



- **6-bit THD for 10GHz sampling of a full-scale (800mVp-p) signal.**

Area and Power Estimates
(10-Gig Serial)

- Assumed technology: Digital 0.13µm CMOS, Analog 0.18µm SiGe
- Receiver uses 8-tap FFE and 6-tap DFE (same as in simulations)
- DSP parallelization factor 8 (1.25 GHz clock speed)
- ADC parallelization factor 8

Component	Area	Power
Analog	----	0.45 Watts
DSP	$1mm^2$	0.80 Watts
Total	----	~ 1.25Watts

- 16-Parallel Implementation requires more area but slower clock and lower clock power.

Conclusions

- Digital equalization has potential to overcome DMD problems in multimode fibers and extend link range
- Parallel processing makes it possible to implement advanced digital equalization at symbol rates as high a 10GBaud
- Advanced CMOS and SiGe technologies offer great promise for interleaved A/D converters at the required sampling rates
- In addition, advanced VLSI technologies offer potential for low cost, low power implementations
- However, more studies are needed to conclusively establish the feasibility of equalization for optical channels

References

1. S.D.Personick, “Baseband Linearity and Equalization in Fiber Optic Digital Communication Systems,” *Bell System Technical Journal*, Vol.52, No.7, Sept.1973, pp.1175-1194

2. K.K.Parhi, “Pipelining in Algorithms with Quantizer Loops,” *IEEE Transactions on Circuits and Systems*, Vol.38, No.7, July 1991, pp.745-754

3. S.Kasturia and J.H.Winters, “Techniques for High-Speed Implementation of Nonlinear Cancellation,” *IEEE Journal on Selected Areas in Communications*, Vol.9, No.5, June 1991, pp.711-717

4. E.A.Lee and D.G.Messerschmitt, “Digital Communication,” 2nd edition, Kluwer Academic Publishers, 1994