PMC-Sierra, Inc.
MAKING GLOBAL NETWORKS WORK

XGMII Timing

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IEEE 802.3ae September Interim

New Orleans, LA

Review of Current Proposal

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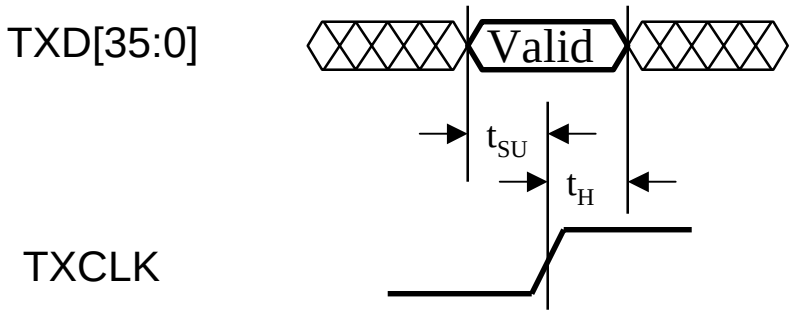

- **TX Direction (from MAC to XGXS)**
- **TXCLK is forwarded along with data**
  - **t_{SU} = t_H = 960ps at source**

Current Implementation, TX Side

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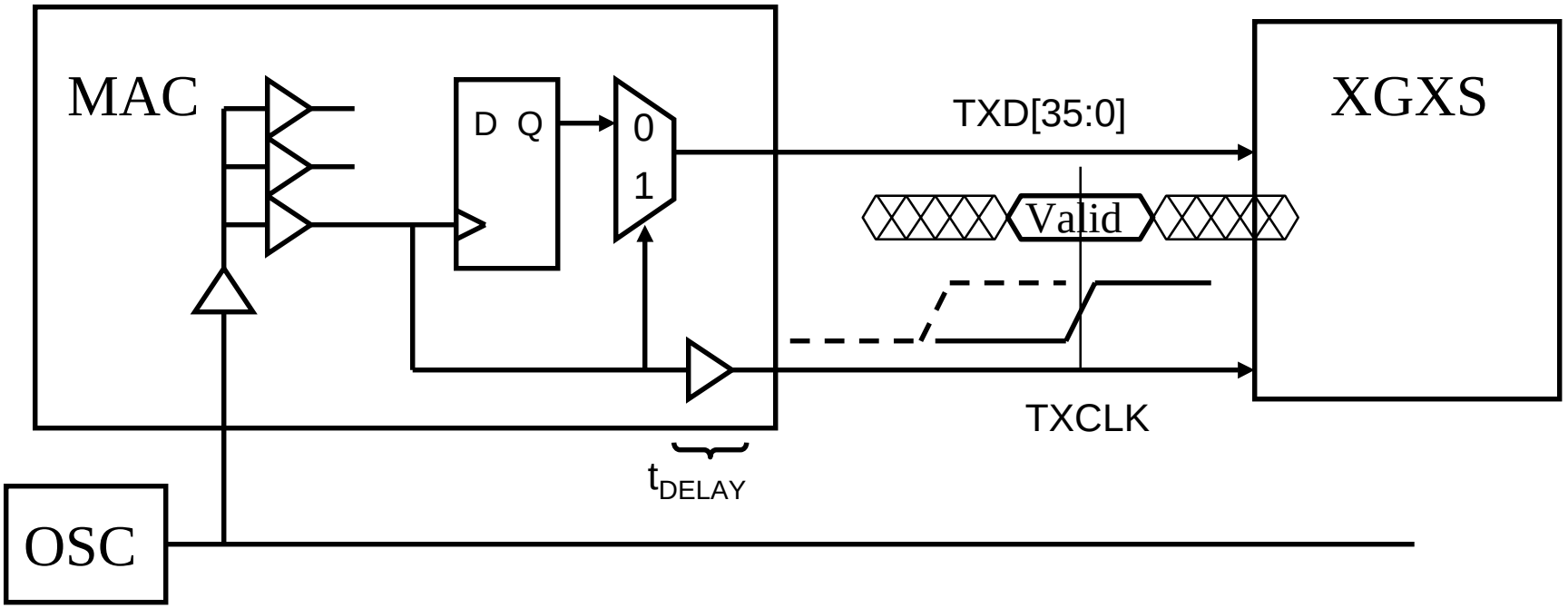

- **To get 960 ps. setup time requires t_{DELAY} of > 960 ps.**
- **But any delay in CMOS varies about 2.5x from fast corner process/voltage/temp to slow corner**
- **To guarantee 960 ps. fast corner requires >2.5 ns. slow corner**
- **But a delay of 2.5 ns. leaves only 700ps. hold time (broken)**
- **The situation is really worse, since data skew must increase t_{DELAY}**

Proposed TX Implementation

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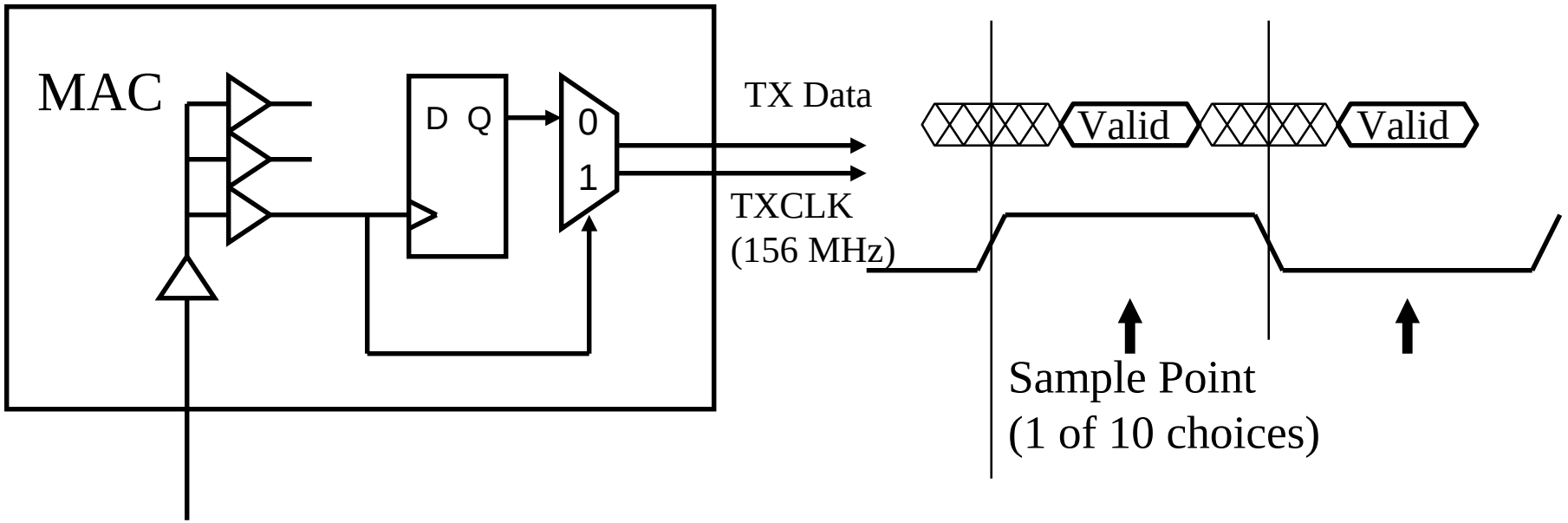

- **TX Direction - MAC: Source-simultaneous DDR clock**
  - **Trivial to generate, even with ASIC toolflow**
  - **Best skew match with data, since it's just another data bit**
- **XGXS: Locally generated sample clock**
  - **XAUI bit clock gives 10 sample points per half period (320 ps. quantization error)**
  - **Adapts to changing process, temperature, etc.**

Proposed RX Implementation

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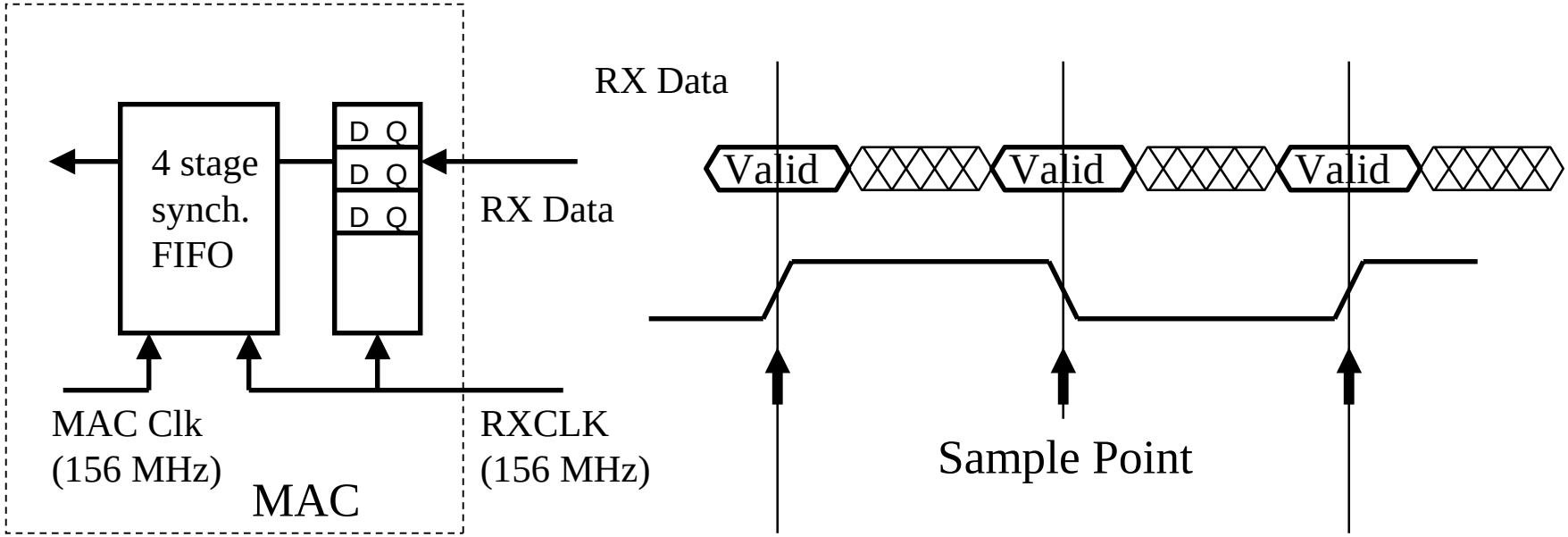

- **XGXS: Source-centered DDR clock**
  - **XAUI bit clock provides a way to generate RXCLK at a precise timepoint, without resorting to delay buffers**
- **RX Direction - MAC: Direct capture**
  - **Trivial to use; directly sample the data, then FIFO to local phase domain**
  - **Simplest implementation for the MAC designer**

Proposed Timing

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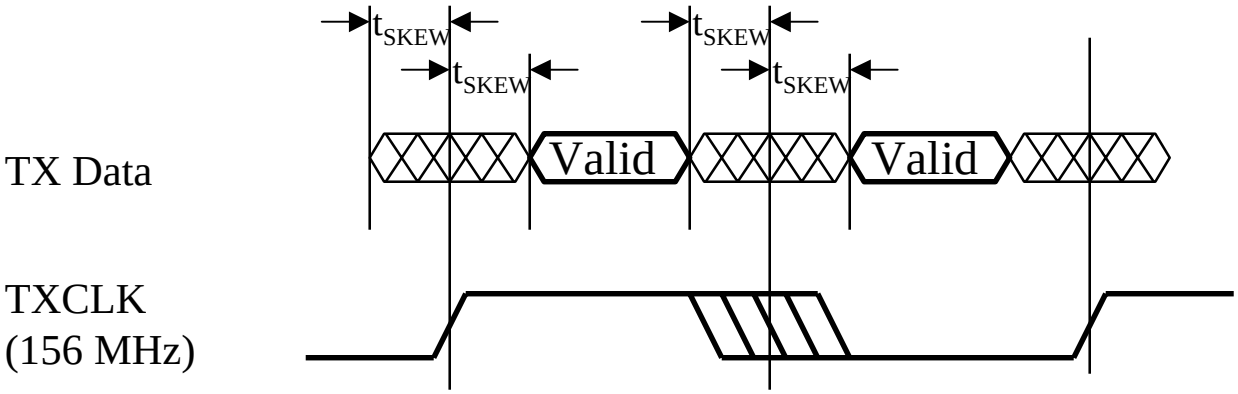

- **Transmit direction**
  - **Tskew (any data transition to TXCLK rising edge) < +/- 800ps.**
  - **Tskew (any data transition to nominal location of TXCLK falling edge) < +/- 800 ns.**
- **Receive direction**
  - **No change**

Summary & Rationale

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- **Adopt source-synchronous clocking in the transmit direction**
- **Retain source-centered clocking in the receive direction**
- **This puts the workload of making precise delays where the “tools” are -- in the XGXS**
  - **XAUI bit clock locked to TXCLK is there already**
- **Simplifies the MAC implementation**
  - **ASIC toolflow, no custom/matched I/O cells required**