MIB, Registers and Function

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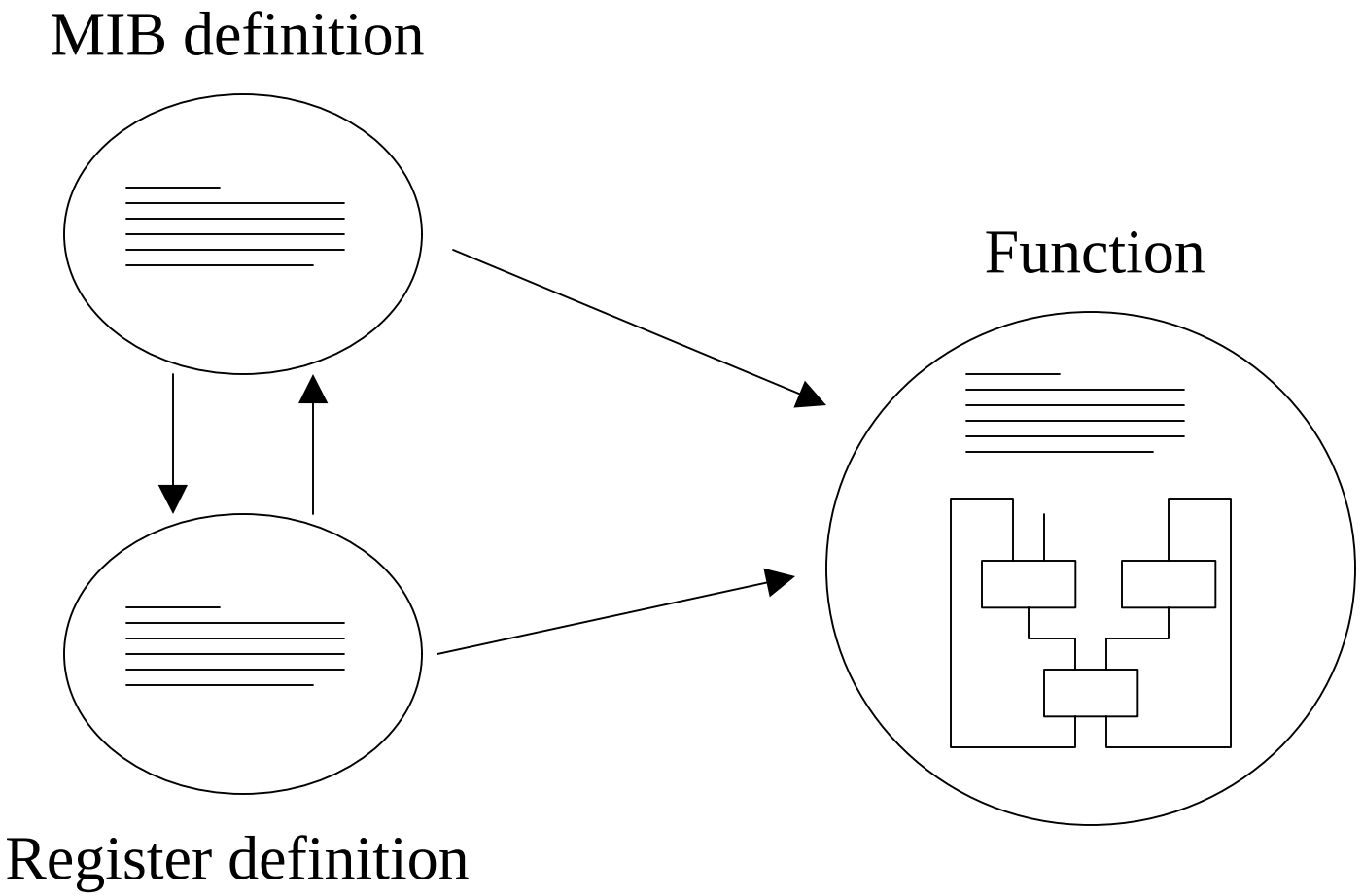

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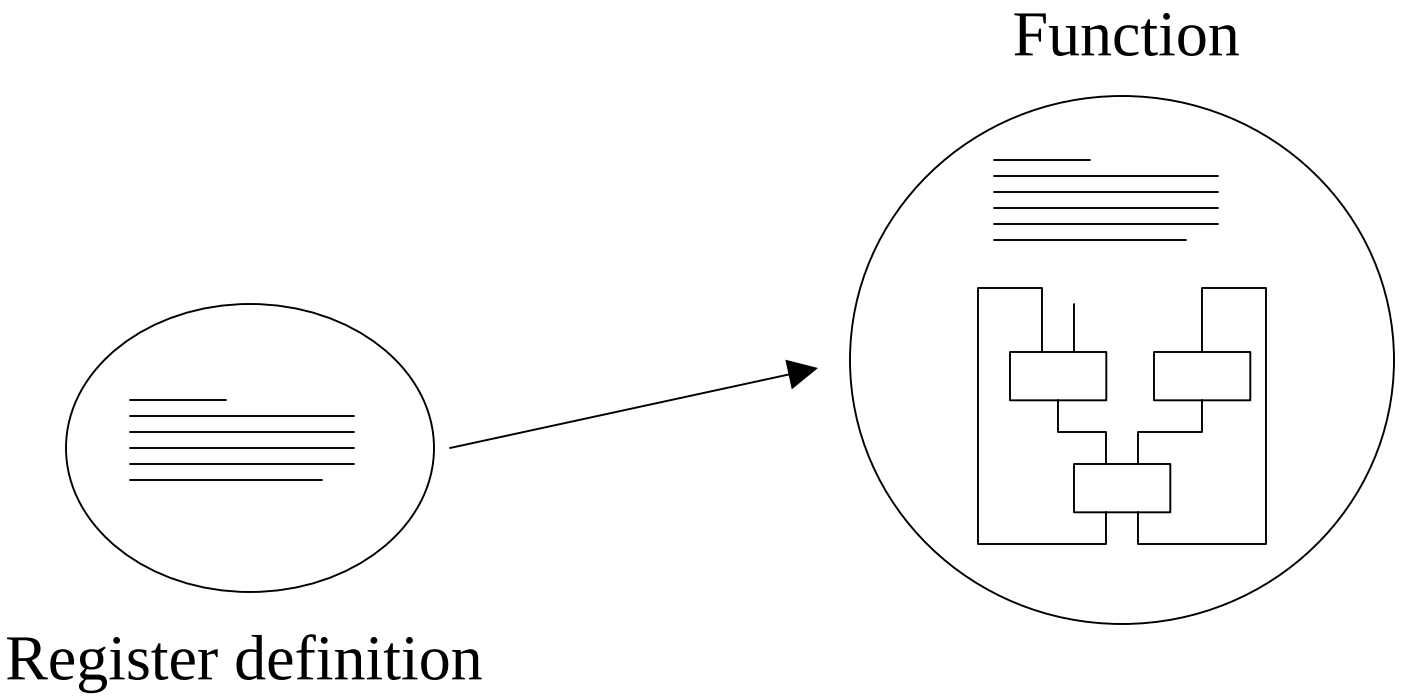

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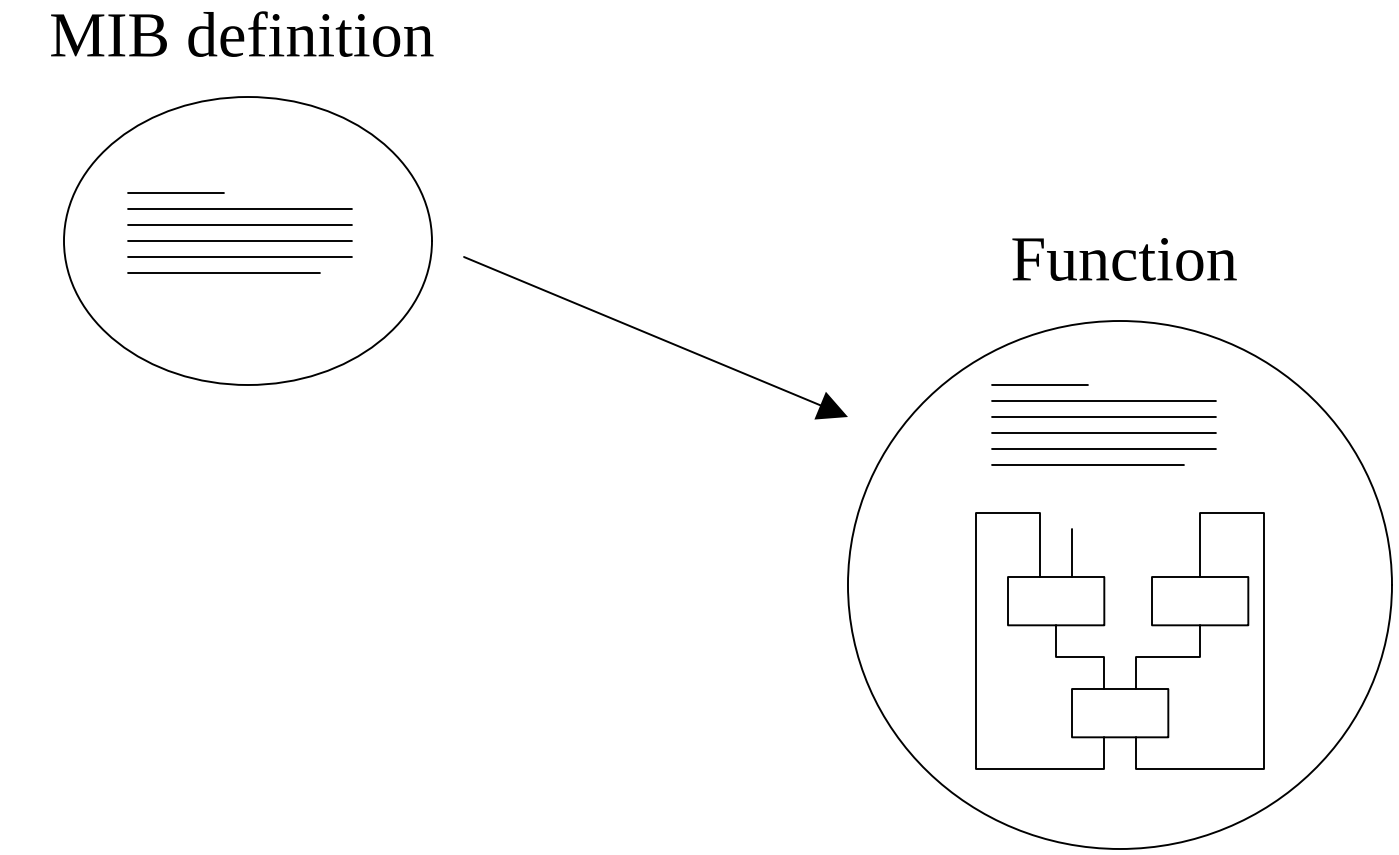

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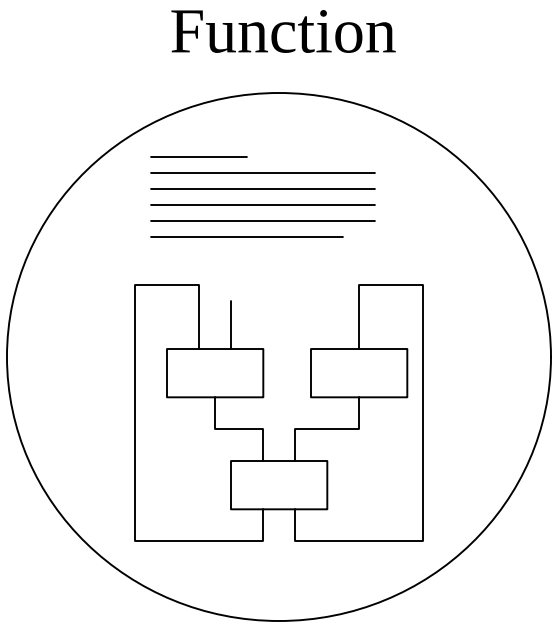

Clause 22 - Link Status

22.2.4.2.13 Link Status

When read as a logic one, bit 1.2 indicates that the PHY has determined that a valid link has been established. When read as a logic zero, bit 1.2 indicates that the link is not valid. **The criteria for determining link validity is PHY specific.** The Link Status bit shall be implemented with a latching function, such that the occurrence of a link failure condition will cause the Link Status bit to become cleared and remain cleared until it is read via the management interface. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

Clause 30 - Link Status

30.5.1.1.4 aMediaAvailable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED value list that has the following entries:

other	undefined
unknown	initializing, true state not yet known
available	link or light normal, loopback normal
not available	link loss or low light, no loopback
remote fault	remote fault with no detail
invalid signal	invalid signal, applies only to 10BASE-FB
remote jabber	remote fault, reason known to be jabber
remote link loss	remote fault, reason known to be far-end link loss
remote test	remote fault, reason known to be test
offline	offline, applies only to Clause 37 Auto-Negotiation
auto neg error	Auto-Negotiation Error, applies only to Clause 37 Auto-Negotiation

BEHAVIOUR DEFINED AS:

If the MAU is a link or fiber type (FOIRL, 10BASE-T, 10BASE-F), then this is equivalent to the link test fail state/low light function. For an AUI, 10BASE2, 10BASE5, or 10BROAD36 MAU, this indicates whether or not loopback is detected on the DI circuit. The value of this attribute persists between packets for MAU types AUI, 10BASE5, 10BASE2, 10BROAD36, and 10BASE-FP.

Clause 28 - Auto-Negotiation

28.2.4 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. If an MII is physically implemented, then management access is via the MII Management interface. **Where no physical embodiment of the MII exists, an equivalent to MII Registers 0, 1, 4, 5, 6, and 7 (Clause 22) are recommended to be provided.**

Test mode (1000BASE-T)

40.6.1.1.2 Test modes

The test modes described below shall be provided to allow for testing of the transmitter waveform, transmitter distortion, and transmitted jitter. For a PHY with a GMII interface, these modes shall be enabled by setting bits 9.13:15 (1000BASE-T Control Register) of the GMII Management register set as shown in Table 40-7. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. **PHYs without a GMII shall provide a means to enable these modes for conformance testing**.