

Clause 33 update - MDIO/MDC management interface

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Clause status

- Clause 33 draft based around the register requirements of the Blue Book proposals
- Additional ‘obviously needed’ bits added
 - Details to be given during Logic Track meeting
- MDIO/MDC device types and access types enhanced

Clause status

- Finalised device types and allocated address
 - Slight change from Blue Book presentation

Blue Book device addresses

Value	Device
00000	Reserved
00001	PMD
00010	XGXS PHY
00011	XGXS DTE
00100	WIS
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D1.0 device addresses

Value	Device
00000	Reserved
00001	PMA/PMD
00010	WIS/PCS
00011	XGXS PHY
00100	XGXS DTE
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Clause status

- MDIO/MDC access type enhancement
 - Allows burst writes, burst reads and write/verify bursts

Blue Book access types

OP	Access Type
00	Address
01	Write
10	Read
11	Post Read Inc Address

D1.0 access types

OP	Access Type
00	Address
01	Write
10	Post Read Inc Address
11	Post Write Inc Address

Assumptions

- PMA combined with PMD into one ‘device’
- PCS combined with WIS into one device
 - May have a PCS without a WIS, but will never have a WIS without a PCS
 - No one could build a WIS only chip as the WIS - PCS interface is not exposed
- Separate PHY and DTE XGXS devices
 - As in Blue Book

Major issues

- How optional is the MDIO/MDC interface ?
 - Previously part of *optional* MII / GMII
 - If you did implement the MII (or GMII) interface you *had* to implement MDIO/MDC
 - Under what conditions is it mandatory in 10G ?
 - Further discussion at the logic track meeting
- Definition of an electrical interface
 - Is a new low voltage spec required ?

Minor issues

- WIS error monitoring
 - Which flags and counters to report ?
- Provide a Link OK bit ?
- Provide an Isolate bit ?
- Editorial - move Clause 22 MDIO/MDC material over to Clause 33

Summary

- Minor modifications to MDIO/MDC addressing
- Blue Book register requirements included
 - Consensus required on WIS error reporting
- Additional ‘obvious’ bits added
- Ready for Task Force review