Clause 33 logic track report

Edward Turner - 3Com

edward_turner@eur.3com.com

What is the point of MDC/MDIO ?

- It '.. provides access to management parameters and services.'
  - Peeking at the internal status of sublayers and state machine variables
- It is not used for passing real time information between sublayers and their state machines
  - That function is carried out by defined primitives
    - e.g. PMD_SIGNAL.indicate (SIGNAL_DETECT)

What is the point of MDC/MDIO ?

- Primitives and variables do not **have** to be accessible through MDIO/MDC
- Selected primitives and variables are made accessible to allow device management

Clause status

- Clause 33 draft based around the register requirements of the Blue Book proposals
- Additional ‘obviously needed’ bits added
  - Detailed in following slides
- MDIO/MDC device types and access types enhanced

Device types

- Finalised device types and allocated address
  - Slight change from Blue Book presentation

Blue Book device addresses

Value	Device
00000	Reserved
00001	PMD
00010	XGXS PHY
00011	XGXS DTE
00100	WIS
-------	----------

D1.0 device addresses

Value	Device
00000	Reserved
00001	PMA/PMD
00010	WIS/PCS
00011	XGXS PHY
00100	XGXS DTE
-------	----------

Device bits

- All devices given some basic bits
  - Reset
  - Loopback
  - Power down
  - Two device present bits
    - Always return <1 0> and allow a device to be polled to check if it is present
  - Two ‘identifier’ registers
    - Same as unique PHY identifier registers in Clause 22

Device bits

- PMA combined with PMD into one ‘device’
  - Bits : optical interface type (1550nm/1310nm), optical power detect, 9.58Gbps capable, 10Gbps capable
- PCS combined with WIS into one device
  - WIS bits : WIS enable, WIS status, WIS capable, WIS bypass capable, error bytes from Blue Book
  - PCS bits : sync done, high BER

Device bits

- PCS / WIS combined into one device
  - May have a PCS without a WIS, but will never have a WIS without a PCS.
  - No one could build a WIS only chip as the WIS - PCS interface is not exposed.

Device bits

- PHY XGXS
  - New bits : TX path link status, TX path lane sync <3..0>
- DTE XGXS
  - New bits : RX path link status, RX path lane sync <3..0>

Access enhancements

- MDIO/MDC access type enhancement
  - Allows burst writes, burst reads and write/verify bursts

Blue Book access types

OP	Access Type
00	Address
01	Write
10	Read
11	Post Read Inc Address

D1.0 access types

OP	Access Type
00	Address
01	Write
10	Post Read Inc Address
11	Post Write Inc Address

Issues to resolve

- Definition of an electrical interface
  - Is a new low voltage spec required ?
- WIS error monitoring
  - Which flags and counters to report ?
  - Discuss in WIS discussion session
- Provide Link OK and Isolate bits ?
- Editorial - move Clause 22 MDIO/MDC material over to Clause 33

Issue - register bit definitions

- Allocate registers, provide top level description and link to variable names
- Propose that detailed definitions of behaviour are not given in Clause 33
- Reference out to Clauses for functionality
  - MDIO/MDC is optional, but functionality is mandatory

Major issue - optionality

- Is the MDIO/MDC interface optional ?
  - The MDIO/MDC interface is now separate from the XGMII interface
  - Previously part of *optional* MII / GMII
  - You did not *have* to implement the MDIO/MDC interface
    - e.g. a PHY without an MII did not require an MDIO/MDC interface. Could use a processor interface.

Example from auto-negotiation

28.2.4 Management function requirements

The management interface is used to communicate Auto-Negotiation information to the management entity. If an MII is physically implemented, then management access is via the MII Management interface. **Where no physical embodiment of the MII exists, an equivalent to MII Registers 0, 1, 4, 5, 6, and 7 (Clause 22) are recommended to be provided.**

Major issue - optionality

- Possible solutions
  - Make the XGMII and MDC/MDIO interfaces independently optional
    - Then you don't have to implement either
  - Make MDIO/MDC part of each optional interface (XGMII, XAUI, XSBI, SUPI)
    - Any device with one of these interfaces would have to also implement MDIO/MDC
  - Make the MDIO/MDC mandatory for 10G
    - How do you conformance test it ?

Summary

- Minor modifications to addressing
- Blue Book register requirements included
  - Consensus required on WIS error reporting
- Additional ‘obvious’ bits added
- Issues of optionality and electrical interface remain outstanding
- Ready for Task Force review

Discussion items

- Electrical interface
- Optionality
  - Mandatory
  - Independently optional
  - Mandatory part of each optional interface (XGMII, XAUI, XSBI, SUPI)