Major capabilities/options

Item	Feature	Sublcause	Status	Support	Value/comment
CL	Implementation supports classification	33.2.6	O		N/A
MC	Classification uses the measured Current method	33.2.6.2	O		N/A
MV	Classification uses the measured Voltage method	33.2.6.3	O		N/A
PA	Implement a PSE which does not contain a power supply capable of supplying maxi-mum power to all the devices that could possibly connect to it.	33.2.9	O		N/A
MDL	The PSE may monitor the PD data link and create a value, PD_DATA_LINK	33.2.10	O		N/A
PCA	Pair control ability - PSE supports the option to control which PSE Pinout is used	33.6.1.1.8	O		N/A

Power sourcing equipment

Item	Feature	Sublcause	Status	Support	Value/comment
1	Implement alternative A, alternative B, or both	33.2.1	M		N/A
2	Current difference between conductors of the same pair	33.2.1	M		N/A
3	Voltage between two shorted pairs of power component conductors	33.2.1	M		N/A
4	Not operate both alternative A and alternavive B on the same link simultaneously	33.2.1	M		N/A
5	Requirements of midspan and PSE location	33.2.2	M		N/A
6	Midspan PSE use alternative B	33.2.2	M		N/A
7	Apply power only after PD detection	33.2.3	M		N/A
8	PD operate without regard to data link status	33.2.3	M		N/A
9	Detect PD by probing via the PSE MDI interface	33.2.4	M		N/A
10	Open circuit voltage	33.2.4	M		N/A
11	Short curcuit current	33.2.4	M		N/A
12	Output capacitance	33.2.4	M		N/A
13	Exibit one of the detection circuits in all detection states	33.2.4	M		N/A
14	Detection voltage V_{detect} with a valid PD signature connected	33.2.4.1	M		N/A

15	Two measurements with V_{detect}	33.2.4.1	M		N/A
16	Control rise and fall time when switching detections voltages	33.2.4.1	M		N/A
17	PSE implement proper detection algorithm	33.2.5	M		N/A
18	Probe link to detect all PDs which present a valid signature: (19K to 26.5K Ω DC resistance) * (100nF capacitance or less) * (Voltage offset of at least 2.0 volts DC) * (Current offset of a least 12mA)	33.2.5.1	M		N/A
19	Reject PDs which present an invalid signature: (Less than 15K Ω DC resistance) + (More than 33K Ω DC resistance) + (More than 10μF capacitive load)	33.2.5.2	M		N/A
20	Complete detection of a valid signature in less than 500ms	33.2.5.3	M		N/A
21	Turn on power after a valid detection in less 400ms if power is to be applied	33.2.5.3	M		N/A
22	Turn on power on the same pairs as those used for detection	33.2.5.3	M		N/A
23	Classify PDs as class 0 if classification is not implemented	33.2.6	!CL:M		N/A
24	Provide V_{Class} between 15 and 20 volts, limited to less than 100 ma	33.2.6.2	MC:M		N/A
25	Measure I_{Class} and classify PD according to Table 3	33.2.6.2	MC:M		N/A
26	Provide I_{Class} limited to less that 47mA, with V_{Class} limited to less than 30 volts	33.2.6.3	MV:M		N/A
27	Measure V_{Class} and classify PD according to Table 4	33.2.6.3	MV:M		N/A
28	Complete detection, classification (if implemented and power PD in time interval $t_{on\_nominal}$	33.2.7	M		N/A
29	$t_{on\_nominal}$ less than 1 second after PD is attached to PSE	33.2.7	M		N/A
30	Wait at least 2 seconds before attempting another detection	33.2.7.1	M		N/A
31	Not apply voltage greater than 1 volt backoff period	33.2.7.1	M		N/A
32	Not wait detection backoff period if open circuit (resistance > 1MΩ) is detected	33.2.7.1	O		N/A
33	PSE provide power to MDI according to Table 5	33.2.8	M		N/A
34	PSE max current less than 350mA	33.2.8	M		Table 5, item 4a
35	Must disconnect for t >T_{UDL}	33.2.8	M		Table 5, item 6a
36	The power must be disconnected from the port within T_{LIM}	33.2.8	M		Table 5, item 10

37	PSE comply with applicable local and national codes	33.2.8	M		N/A
38	PSE implement a power allocation algorithm	33.2.9	PA:M		N/A
39	Not supply power if unable to provide maximum requested by PD	33.2.9	PA:M		N/A
40	Remove power from a port when PD is removed or no longer requesing power	33.2.10	M		N/A
41	Create and monitor PD_DATA_LINK	33.2.10	MDL:M		N/A
42	A PD that does not maintain: (minimum current draw defined in Table 12) + (active PD_DATA_LINK) will remove power within limits ot T_{PMDO}	33.2.10	M		N/A

Powered Devices

Item	Feature	Sublcause	Status	Support	Value/comment
1	Accept power on either sets of MDI conductors	33.3.1	M		N/A
2	MDI implementation: Pair (1,2) at a lower potential than pair (3,6)	33.3.1	M		N/A
3	MDI-X implementation: Pair (1,2) at a higher potential than pair (3,6)	33.3.1	M		N/A
4	Operate with polarites shown in table 6	33.3.1	M		N/A
5	Present valid detection signature on each set of pairs defined in 33.3.1 if not powered via the MDI	33.3.2	M		N/A
6	Present an invalid signature on each set of pairs defined in 33.3.1 if not powered via the MDI and will not accept power via the MDI	33.3.2	M		N/A
7	When powered present an invalid signature on the set of pairs not drawing power	33.3.2	M		N/A
8	Valid PD detection signature conforms to Table 7	33.3.2	M		N/A
9	PD resistance and capacitance not effected by extended probe voltages up to 57 volts	33.3.2	M		N/A
10	Invalid detections signatures have at least one characteristic described in Table 8	33.3.2	M		N/A
11	Implement classification selection according to maximum power draw specified in Table 9	33.3.3	CL:M		N/A
12	Implement classification signatures according to Tables 10 and 11	33.3.3	CL:M		N/A
13	Present only one set of classification characteristcs	33.3.3	CL:M		N/A
14	Implement identical classification for each PSE mode	33.3.3	CL:M		N/A
15	Implement PD power accroding to Table 12	33.3.4	M		N/A

16	Input current (startup mode) limited by PSE for 50mS if Cport < 180uF. Limited by PD if Cport > 180uF	33.3.4	M		Table 12, item 5b
17	10mA minimum current maintained	33.3.4	M		Table 12, item 5b
18	Implement PD maintenance signal (current draw specified in Table 12, item 5) * (maintain PD_DATA_LINK at the PSE)	33.3.5	M		N/A
19	Remove both components of the power maintenance signal when power is no longer required	33.3.5	M		N/A

Electrical Specifications

Item	Feature	Sublcause	Status	Support	Value/comment
1	Implement electrical specifications to the cabling side of mated connections where power is supplied or received	33.4	M		N/A
2	Requirements of electrical specifications apply to transmit and receive pairs	33.4	M		N/A
3	Operating condition requirements apply while transmitting data or when power is applied	33.4	M		N/A
4	Provide electrical isolatioin between port device circuits, frame ground and MDI leads	33.4.1	M		N/A
5	Withstand at least one electrical strenght tests specified 33.4.1	33.4.1	M		N/A
6	No insulation breakdown during electrical strength tests	33.4.1	M		N/A
7	Resistance after electrical strength test $\geq 2M\Omega$, measured at 500 Vdc	33.4.1	M		N/A
8	Any wire pair will withstand any short cirucit to any other pair for an infinite amount of time	33.4.2	M		N/A
9	Removal of a short circuit between wire pairs will allow normal operation of the link	33.4.2	M		N/A
10	Magnitude of short circuit current not to exceed 500ma	33.4.2	M		N/A
11	Any wire pair will withstand a 1000V common-mode impulse applied at Ecm of either polarity without damage	33.4.2	M		N/A
12	The shape of the impulse shall be 0.3/50 µ S for item 12	33.4.2	M		N/A
13	Impeadance balance for transmit and receive pairs: - 29-17 log 10 (f/10)dB from 2.0 to 20MHz for 10Mbit/s PHYs - 34-19.2 log 10 (f/10)dB from 1.0 to 100MHz for 100Mbits/s or greater PHYs.	33.4.3	M		N/A

14	When pair (1,2) is looped back to pair (3,6) at the PD the absolute resistance at the PSE connector will be less than 3.5%.	33.4.4	M		N/A
15	Magnitude of common-mode output voltage while transmitting data and with power applied will not exceed 50mV peak when operating at 10Mbits/s and 50mV peak-to-peak when operating at 100Mbits/s or greater	33.4.5	M		N/A
16	Magnitude of common-mode AC voltage at all other ports will not exceed 50mV peak-to-peak.	33.4.5	M		N/A
17	Frequency when measureing AC voltage at all other ports will be from 0.15 MHz to 100MHz	33.4.5	M		N/A
18	A PSE will comply with applicble local and national codes for the limitation of electromagnetic interference	33.4.6	M		N/A
19	Noise from an operating PSE to the differential transmit and receive pairs will not exceed 10mV peak-to-peak measured from 0.15MHz to 100MHz	33.4.7	M		N/A
20	Return loss at least 15dB below incident signal over the frequencey range 5MHz to 10MHz for 10Mbit/s PHYs	33.4.8	M		N/A
21	Return loss at least 16dB below incident signal over the frequencey range 1.0MHz to 40MHz and 10-20 log 10 (f/80)dB from 40MHz to 100MHz for 100Mbit/s or greater PHYs	33.4.8	M		N/A
22	Connector when mated meet or exceed ANSI/TIA/EIA-568-B.2	33.4.9	M		N/A
23	PSE cabling channel not alter transmission requeirment of cabling channel specified in ISO/IEC 11801-2000	33.4.10	M		N/A
24	Insertion of PSE not increase length of cabling channel beyone 100 meters as defined in ISO/IEC 11801-2000	33.4.10	M		N/A
25	All connections in cabling channel meet requirements of IEEE 802.3 clause 33 and ISO/IEC 11801-2002 for insertion loss, NEXT, FEXT, return loss and delay for all transmit and receive pairs	33.4.10.1	M		N/A
26	All cables in cabling channel meet requirements of IEEE 802.3 clause 33 and ISO/IEC 11801-2002 for insertion loss, NEXT, FEXT, return loss and delay for all transmit and receive pairs	33.4.10.2	M		N/A

Environmental

Item	Feature	Sublcause	Status	Support	Value/comment
1	All equipment conform to IEC publication 60950:1991	33.5.1	M		N/A

2	Electrical safety hazards avoided or protected against	33.5.2	M		N/A
3	Application of telephony voltages described in 33.5.5 not result in any safety hazard	33.5.5	M		N/A
4	PD and PSE powered cabling comply with local and national codes for the limitation of electromagnetic interference	33.5.6	M		N/A

Management function requirements

Item	Feature	Sublcause	Status	Support	Value/comment
1	Register 11 for PSE control and status functions	33.6.1	M		N/A
2	Register 12 for PD control and status functions	33.6.1	M		N/A
3	A write to bits 11.15:13 ingnored and a value zero returned on a read	33.6.1.1.1	M		N/A
4	Overcurrent condition detected	33.6.1.1.2	M		N/A
5	Overcurrent bit implemented with a latching function and remain set until cleared	33.6.1.1.2	M		N/A
6	Overcurrent bit cleard when read by management interface	33.6.1.1.2	M		N/A
7	Overcurrent bit cleard by a PHY reset	33.6.1.1.2	M		N/A
8	Undercurrent condition detected	33.6.1.1.3	M		N/A
9	Undercurrent bit implemented with a latching function and remain set until cleared	33.6.1.1.3	M		N/A
10	Undercurrent bit cleared when read by management interface	33.6.1.1.3	M		N/A
11	Undercurrent bit cleard by a PHY reset	33.6.1.1.3	M		N/A
12	Detection control bit 11.4 set to '1' allows normal operation except power not applied to valid detected PDs	33.6.1.1.6	M		N/A
13	Detection control bit 11.4 set to '1' causes power to be removed if applied to a valid PD previously detected	33.6.1.1.6	M		N/A
14	Ignore writes to bits 11.3:2 if Pair Control Ability is not supported	33.6.1.1.7	!PCA:M		N/A
15	Return supported PSE pinout alternative if Pair Control Ability is not supported and bits 11.3:2 are read	33.6.1.1.7	!PCA:M		N/A
16	Bits 11.3:2 set to '01' forces the PSE to use Alternative A	33.6.1.1.7	PCA:M		N/A
17	Bits 11.3:2 set to '10' forces the PSE to use Alternative B	33.6.1.1.7	PCA:M		N/A
18	Bit 11.1 read a logic one idicates the PSE supports pair control ability	33.6.1.1.8	O		N/A

19	PSE function enabled by setting bit 11.0 to a logic one	33.6.1.1.9	M		N/A
20	PSE function disabled by setting bit 11.0 to a logic zero	33.6.1.1.9	M		N/A
21	Bit 11.0 set to logic zero will cause the MDI to function as if there was no PSE present	33.6.1.1.9	M		N/A
22	A write to bits 12.15:3 ingnored and a value zero returned on a read	33.6.1.2.1	M		N/A