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PSE-PD Inter-operate - Stability Analysis

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Objectives

- Specify the requirements to ensure PSE - PD stability at Normal Powering Mode

- Strategy

- Using Impedance Design Criteria
  - Specify PD input impedance without input filter
  - Specify PD input filter output impedance
  - Specify PSE power supply output impedance

System Description at Normal Powering Mode

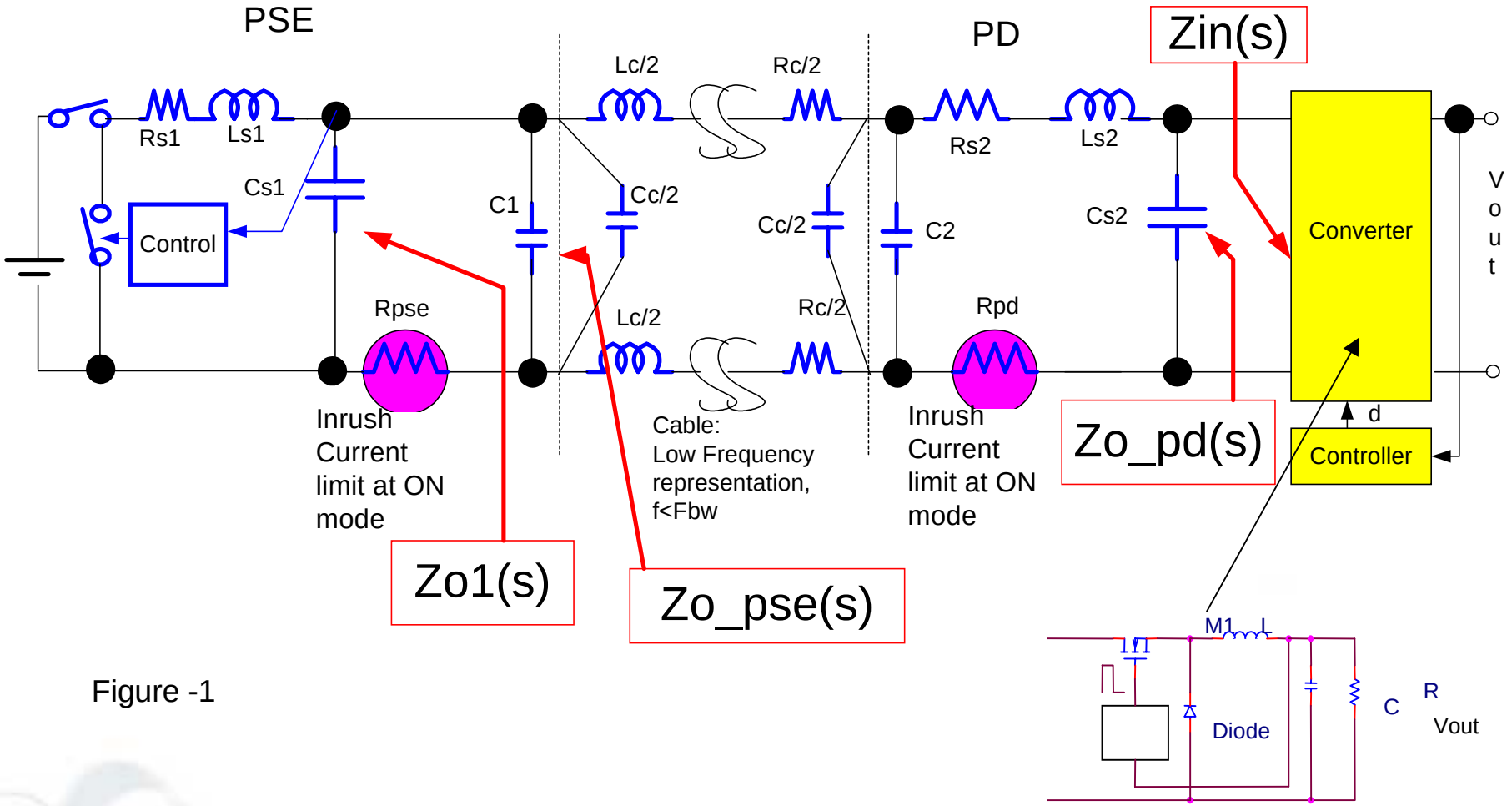


Figure -1

Problem Definition

- Under Specific Combinations of PSE output impedance and PD input Impedance
  - PSE - PD stability at Normal Powering Mode may be impaired
  - PD Power Supply Dynamic Performance will be changed

The reason:

- PD Power Supply Close Loop Transfer Function

  May be Impaired if Additional Frequency Dependent Elements are Connected From the Power Source (PSE) to the Load (PD's DC/DC converter)

Impedance Allocation Map Measured from PSE Port to PD DC/DC converter input

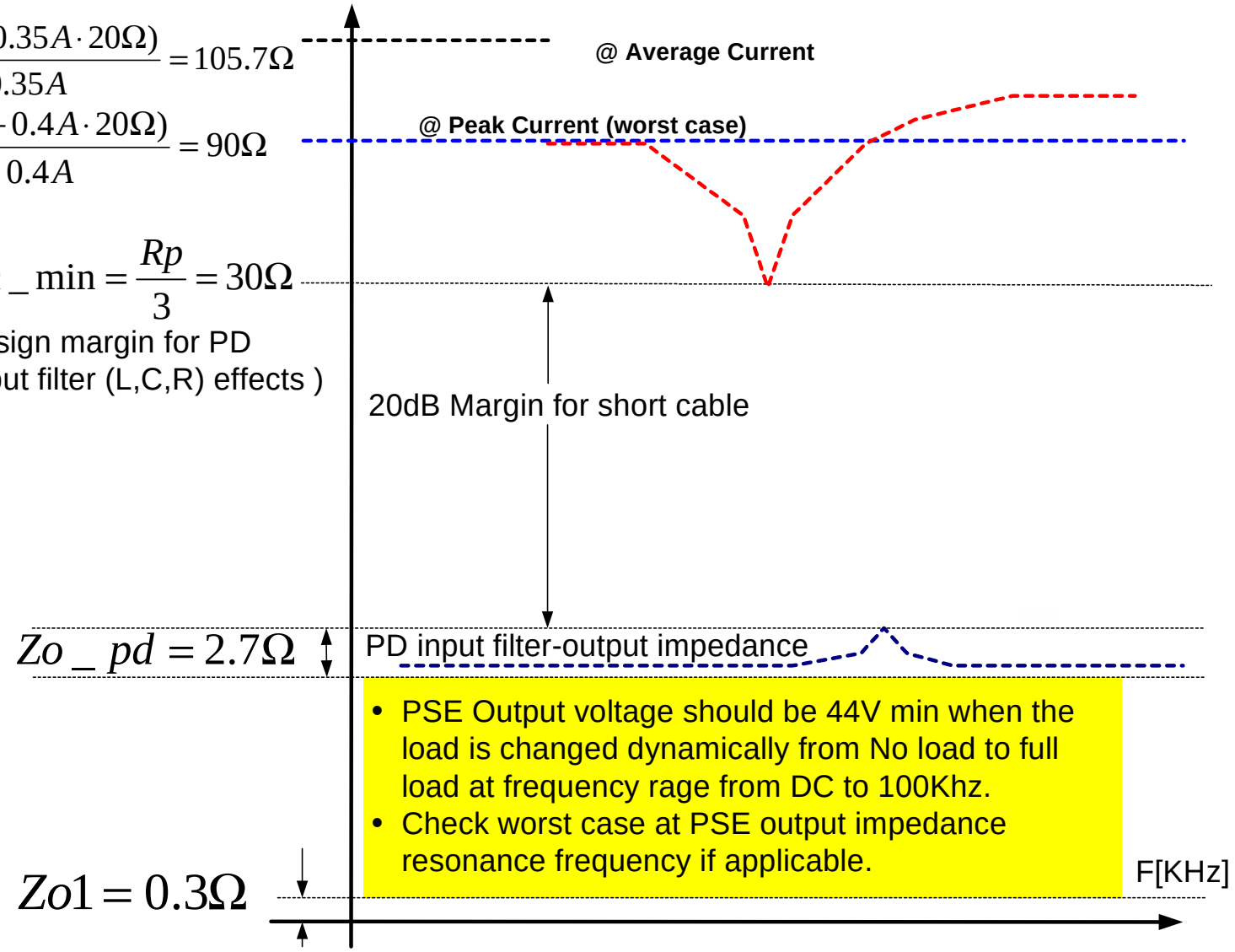
Zin, Zo, Zo1

$$Ra = \frac{(44V - 0.35A \cdot 20\Omega)}{0.35A} = 105.7\Omega$$

$$Rp = \frac{(44V - 0.4A \cdot 20\Omega)}{0.4A} = 90\Omega$$

$$Zin\_\min = \frac{Rp}{3} = 30\Omega$$

(to allow design margin for PD DC/DC output filter (L,C,R) effects)



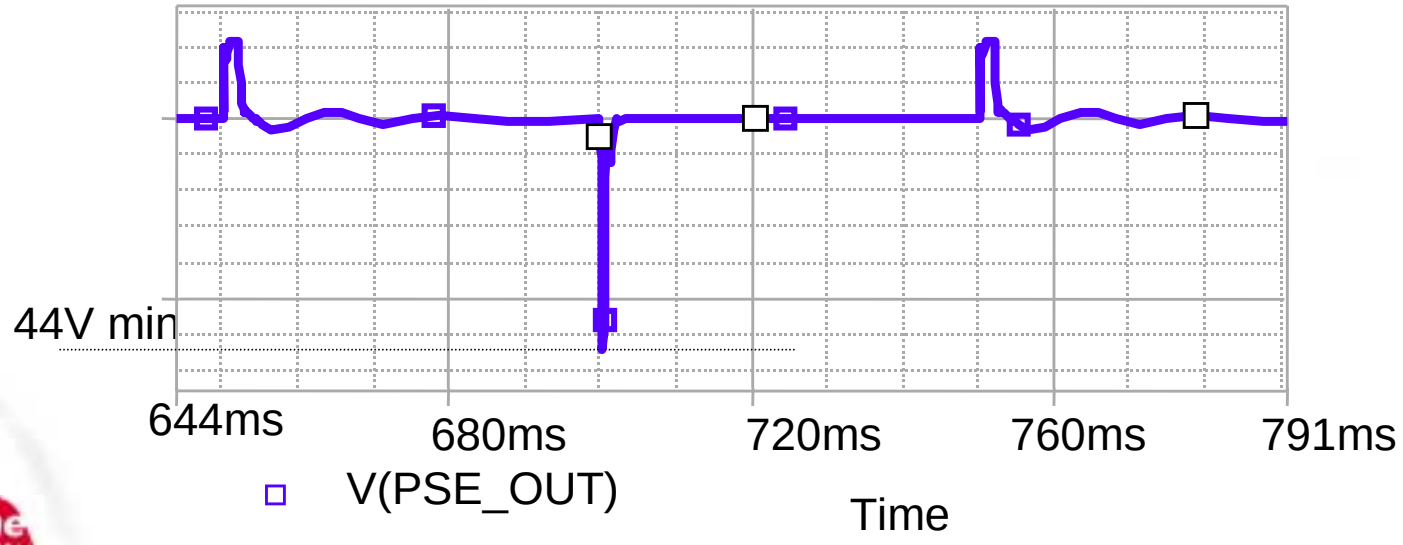
- PSE Output voltage should be 44V min when the load is changed dynamically from No load to full load at frequency rage from DC to 100Khz.
- Check worst case at PSE output impedance resonance frequency if applicable.

Proposed Requirements for PD

- PD converter input EMI filter or Cable inductance followed by capacitor
  - PD designer will ensure stable operation of its DC/DC converter in a presence of an input filter powered through short cable (<1m) and long cable (>100m).
  - Input filter cutoff frequency << Averaging LC filter cutoff frequency. (See Annex A)
  - The absolute value of the filter output impedance (Zo_pd) will not exceed 2.7Ω with short cable (<1m) for Pmax=12.95W assuming PSE output impedance <0.1Ω.
  - For Pmax< 12.95W, Zo_pd min will be Zo_pd= 2.7Ω*12.95/Pmax.
- PD converter input impedance (without input-filter output impedance effect), Zin
  - PD converter input impedance (Zin) will be 30Ω min at max. load condition, Pmax. (12.95W avg, 14.8W peak)
  - For loads Pmax< 12.95W, Zin_min will be Zin_min= 30Ω*12.95/Pmax.
- All the above requirements should be met well above Fbw.
- Fbw=DC/DC converter closed loop cross over frequency.

Proposed Requirements for PSE Output Port

- PSE PS output impedance (Zo1) shall be 0.3Ω max from DC to 100KHz at full load (Pmax=15.4W).
  - For Pmax<15.4W, Zo1= 0.3Ω*15.4/ Pmax
- PSE Port Output voltage should be 44V min when the load is changed dynamically from No Load to Full Load at frequency range from DC to 100KHz. (Compensating for Rpse)
- Check worst case at PSE output port impedance resonance frequency if applicable.



Proposed Requirements for PSE and PD - Summary