IEEE 803.af Management clause 33

33.22 Management function requirements

The MII Management Interface (see 22.2.4) is used to communicate PSE and PD information to the management entity. If a Clause 22 MII or a Clause 35 GMII is physically implemented, then management access is via the MII Management interface. Where no physical embodiment of the MII or GMII exists, an equivalent to PSE and PD MII Registers are recommended to be provided.

33.22.1 PHY specific registers for PSE and PD

Some of the extended registers (registers with addresses 2 to 15) are used as PHY specific registers as described in 22.2.4.3.A PSE shall use register address 11 for its control and status functions. A PD shall use register address 12 for its control and status functions.

Comments:
Is PHY for the physical interface in the PSE and PD ???

33.22.1.1 PSE control and status register (Register 11)(R/W)

The assignment of bits in the PSE Status and Control register is shown in Table 33–22 below. The default value for each bit of the PSE Control and Status register should be choose so that the initial state of the PSE upon power up or reset is a normal operational state without management intervention.

Table 33–22—PSE Status and Control register bit definitions

Bit(s)	Name	Description	R/W 1
11.15:13	Classification	11.15 11.4 11.13 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Reserved 1 0 0 = class 5 0 1 1 = class 4 0 1 0 = class 3 0 0 1 = class 2 0 0 0 = class 1	RO
11.12	Over voltage	1 =Over voltage condition detected 0 =No over voltage condition detected	RO/LH WRITE to Clear
11.11	Under voltage	1 =Under voltage condition detected 0 =No under voltage condition detected	RO/ LH WRITE to Clear
11.10	Over Current	1 =Over current condition detected 0 =No over current condition detected	RO/LH WRITE to Clear
11.9	Under current	1 =Under current condition detected 0 =No under current condition detected	RO/ LH WRITE to Clear
11.8:7:6	Detection Status	11.8 11.7 11.6 1 1 1 = Reserved 1 1 0 = No Valid PD 1 0 1 = PD detected 1 0 0 = test 0 1 1 = Fault condition detected 0 1 0 = PD detected and supplying power 0 0 1 = Searching for PD 0 0 0 = PD Detection disabled	RO
11.5:4	Detection Control	11.5 11.4	R/W

	(11.5:4)	1 1 = Reserved 1 0 = PD Detection test mode 0 1 = PD Detection enabled 0 0 = PD Detection disabled reserve	
11.3:2	Pair Control (11.3:2)	11.3 11.2 1 1 = PSE pinout alternative A and B 1 0 = PSE pinout alternative B 0 1 = PSE pinout alternative A 0 0 = Reserved	R/W
11.1	Pair Control Ability	1 =PSE pinout controllable by Pair Control bits 0 =PSE pinout alternative fixed	RO
11.0	Power Enable (11.0)	1 =Enable PSE functions 0 =Disable PSE functions	R/W

1 R/W =Read/Write, RO =Read Only, LH =Latching High

33.22.1.1.1 Clasification (11.15:13)

Bits 11.15:12 when read describes the different terminal on the Power Over MDI Network . The enumerated type “class0” (Default) indicates that the max Power levels at output of PSE 0.5 - 15.0 Watt. The enumerated type “class1”,indicates that the max Power levels at output of PSE 0.5 - 4.0 W. The enumerated type “class2” indicates that the max Power levels at output of PSE 4.0 - 7.0 W The enumerated type “class3”,indicates that the max Power levels at output of PSE 7.0 - 15.0 W. The enumerated type class4 and class5 Future Use.

33.22.1.1.2 Over Voltage (11.11)

When read as a logic one, bit 11.11 indicates that a over voltage condition has been detected. A over voltage condition shall be detected when the voltage measured at the PSE is greater than Over voltage limit for a duration greater that the Over voltage time limit (see Table 33-5).The Over voltage bit shall be implemented with a latching function, such that the occurrence of a over voltage condition will cause the Over voltage bit to become set and remain set until it is cleared. The Over Voltage bit shall be cleared each time Register PSE is WRITE Clear via the management interface, and shall also be cleared by a PHY reset.

33.22.1.1.3 Under Voltage (11.10)

When read as a logic one, bit 11.10 indicates that a under voltage condition has been detected. A under voltage condition shall be detected when the voltage measured at the PSE is less than under voltage limit for a duration less that the under voltage time limit (see Table 33-5).The Under voltage bit shall be implemented with a latching function, such that the occurrence of a under voltage condition will cause the Under voltage bit to become set and remain set until it is cleared. The Under voltage bit shall be cleared each time Register PSE is WRITE Clear via the management interface, and shall also be cleared by a PHY reset.

33.22.1.1.4 Over Current (11.9)

When read as a logic one, bit 11.9 indicates that a over current condition has been detected. A over current condition shall be detected when the current drawn from the PSE at the MDI is greater than Over load cur-rent limit for a duration greater that the Over load time limit (see Table 33-5).The Over Current bit shall be implemented with a latching function, such that the occurrence of a over current condition will cause the Over Current bit to become set and remain set until it is cleared. The Over Current bit shall be cleared each time Register PSE is WRITE Clear via the management interface, and shall also be cleared by a PHY reset.

33.22.1.1.5 Under Current (11.8)

When read as a logic one, bit 11.8 indicates that a under current condition has been detected. A under current condition shall be detected when the current drawn from the PSE at the MDI is less than Off mode current 2 for a duration greater that the Under load time limit (see Table 33-5).The Under

Current bit shall be implemented with a latching function, such that the occurrence of a under current condition will cause the Under Current bit to become set and remain set until it is cleared. The Under Current bit shall be cleared each time Register PSE is WRITE Clear the management interface, and shall also be cleared by a PHY reset.

Comments:
1 It is assumed that the definition of a underCurrent event and a overCurrent event given above is correct.
2 It would seem to be better if these definitions where moved to within the PSE Power Supply function definition.

33.22.1.1.6 Detection Status (11.8:7:6)

Bits 11.8:7:6 report the current state of the PD Detection function specified in 33.2.3.When read as '000'bits 11.8:7:6 indicates that the PD Detection function has been disabled. When read as '001'bits 11.8:7:6 indicates that the PD Detection function is enabled but has not detected a valid PD. When read as '010'bits 11.8:7:6 indicates that the PD Detection function is enabled, has detected a valid PD and is delivering power. When read as '011'bits 11.8:7:6 indicates that the PD Detection function is enabled but has detected a fault, faults reported are vendor-specific. When read as '100'bits 11.8:7:6 indicates that the PD detection is in test mode power is not delivered to the PD . When read as '101'bits 11.8:7:6 indicates that a valid PD has been detected . When read as '110'bits 11.8:7:6 indicates that a NOT valid PD has been detected .

33.22.1.1.7 Detection Control (11.5:4)

Bits 11.5:4 control the current mode of operation of the PD Detection function specified in 33.2.3. Setting bits 11.5:4 to '00'disables the PD Detection function. Disabling the PD Detection function shall also remove power from a valid PD that has already been detected. Setting bits 11.5:4 to '01'enables that PD Detection function to operate normally. Setting bits 11.5:4 to '10'places the PD Detection function in a test mode. When placed in this test mode the PD function shall operate normally with the exceptions that power shall not be supplied if a valid PD is detected and power shall be remove from a valid PD that has already been detected. The combination '11'has been reserved for future use.

Comments:
1 Is the assumption that power should be removed from a valid PD that has already been detected correct in the case of PD Detection being disabled or being placed in test mode. This would seem to be logical as once the PD detection function is disabled PD disconnect can no longer be detected.
2 It may be better to specify the exact behavior of these modes fully in subclause 33.2.3 and reference them here.

33.22.1.1.6 Pair Control (11.3:2)

Bits 11.3:2 report the supported PSE Pinout Alternative specified in 33.2.1.A PSE may also provide the option of controlling the PSE Pinout Alternative through these bits.Provision of this option is indicated through the Pair Control Ability (11.1) bit. A PSE that does not support this option shall ignore writes to these bits and shall return the value that reports the supported PSE Pinout Alternative. When read as '01'bits 11.3:2 indicates that only PSE Pinout Alternative A is supported by the PSE. When read as '10'bits 11.3:2 indicates that only PSE Pinout Alternative B is supported by the PSE. When read as '11'bits 11.3:2 indicates that PSE Pinout Alternative A and B are used for PD detection however only PSE Pinout Alternative A or PSE Pinout Alternative B is used to supply power once a valid PD is detected. Where the option of controlling the PSE Pinout Alternative through these bits is provided setting bits 11.3:2 to '01'shall force the PSE to use only PSE Pinout Alternative A, setting bits 11.3:2 to '10'shall force the PSE to use only PSE Pinout Alternative B and setting bits 11.3:2 to '11'shall force the PSE to use both PSE Pinout Alternative A and B for PD Detection but only Pinout lternative A or B to supply power. The combination '00'has been reserved for future use.

33.22.1.1.7 Pair Control Ability (11.1)

When read as a logic one,bit 11.1 indicates that the PSE supports the option to control which PSE Pinout Alternative (see 33.2.1)is used for PD detection and power through the Pair Control (11.3:2)

bits. When read as a logic zero, bit 11.1 indicates that the PSE lacks support of the option to control which PSE Pinout Alternative is used for PD detection and power through the Pair Control (11.3:2)bits.

33.22.1.1.8 Power Enable (11.0)

The PSE function shall be enabled by setting bit 11.0 to a logic one. The PSE function shall be disabled by setting bit 11.0 to logic zero. When the PSE function is disabled by this bit the MDI shall function as it would if it had no PSE function.

Note -This bit can not be used to force power onto the MDI, merely to enable the PSE to provide power onto the MDI if a valid PD is detected.

33.22.1.2 PSE Usage power register (Register 12) (R)

This Register is a read-only indicates the measurement power expressed in Watt for a specific port.

33.22.1.3 PSE Usage Current register (Register 13) (R)

This Register is a read-only indicates the measurement current expressed in mA for a specific port.

33.22.1.4 PSE Usage Voltage register (Register 14) (R)

This Register is a read-only indicates the measurement voltage expressed in Volt for a specific port.

33.22.1.5 PD status and control register (Register 15)(R/W)

The assignment of bits in the PD Status and Control register is shown in Table 33–23 below. The default value for each bit of the PD Control and Status register should be chosen so that the initial state of the PD upon power up or reset is a normal operational state without management intervention.

33.22.1.5.1 .Reserved bits (15.15:6)

Bits 15.15:3 are reserved for future standardization. A write shall be ignored and the value zero returned on a read. It is recommended that these bits should be written as zero and ignored when read, this will ensure compatibly with future standardization.

33.22.1.5.2 Clasification (15.5:3)

Bits 15.5:3 when read describes the different terminal on the Power Over LAN Network . The enumerated type “class0” (Default) indicates that the max Power levels at output of PD 0.44 – 12.95 Watt. The enumerated type “class1”,indicates that the max Power levels at output of PD 0.44 - 3.84 W. The enumerated type “class2” indicates that the max Power levels at output of PD 3.84 – 6.49 W The enumerated type “class3”,indicates that the max Power levels at output of PD 6.49 – 12.95 W. The enumerated type class4 and class5 Future Use.

33.22.1.5.3 Pair Status (15.2:1)

Bits 15.2:1 report the supported PD Pinout Mode specified in 33.3.1.When read as ‘01’bits 15.2:1 indicates that only PD Pinout Mode A is supported by the PD. When read as ‘10’bits 12.2:1 indicates that only PD Pinout Mode B is supported by the PD. When read as ‘11’bits 15.2:1 indicates that both PD Pinout Mode A and B are supported by the PD.

Table 33–23—PD Status register bit definitions

Bit(s)	Name	Description	R/W [1]
15.15:6	Reserved	Ignore when read	RO
11.5:3	Classification	15.5 15.4 15.3 1 1 1 = Reserved 1 1 0 = Reserved 1 0 1 = Reserved 1 0 0 = class 5 0 1 1 = class 4 0 1 0 = class 3 0 0 1 = class 2 0 0 0 = class 1	RO
15.2:1	Pair Status	15.2 15.1 1 1 = PD pinout alternative A and B 1 0 = PD pinout alternative B 0 1 = PD pinout alternative A 0 0 = Reserved	RO
14.0	Power Status	1 =PD sourcing power 0 =PD not sourcing power	RO

[1] RO =Read Only

33.22.1.5.4 Power Status (15.0)

When read as a zero, bit 12.0 indicates that the PD is drawing a current less than I_{Port} as specified in Table 33-10.When read as a logic one, bit 15.0 indicates that the PD is drawing a current greater than I_{Port} as specified in Table 33-10.

Comments:
1 The exact definition of the Power on and Power off states for a PD may be better placed in the PD subclause.