# **Coupled Diode Discovery Protocols and Prototypes**

Rick Brooks ribrooks@nortelnetworks.com Larry Miller Idmiller@nortelnetworks.com IEEE802.3af Plenary Meeting, July, 2000

#### **Discovery Process Goals**

- identify appropriate power hungry devices
- identify cable and connection problems
- avoid powering legacy equipment
- minimize the probability of a false detection
- provide a robust system solution
- practicable at a relatively low cost
- allow transparent use of straight and crossover cables
- enable powering without the need for management
- allow for the use of multiple DTE power sources
  - want to be independent of power sequencing
  - discovery method needs to be independent of data transmission



# **Common Mode Discovery Block Diagram**

- uses an AC coupled diode network for polarity sensitive detection
- transformer coupled common mode technique provides 2200 VDC isolation
- pulses and synchronous detection are digitally controlled,
- pseudo random idle spaces are used: lower radiated emissions, harder to fool



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# **Common Mode Discovery, coupled diode network**

- Diode detection modified to allow either polarity of DTE power
- allows for low voltage, polarity sensitive discovery using low duty cycle 5us pulses
- with high duty cycle discovery pulses, can be made to look like an open circuit
  - provides a higher level of discovery confidence
- becomes high impedance at +/- 48 VDC
  - resistors can be small size, or integrated
- easily handles 48 volt transients (intermittent contacts, etc...)







# General timing during discovery phase

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# **Synchronous Detection Scheme**

- Discovery requires a set of consecutive successful discovery cycles
  - the prototype requires 256 consecutive discovery cycles







#### **Basic Flow Diagram, Discovery and Power Control Protocols**

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### **Typical Discovery Pulse Generation Protocol**





# Midspan Power Insertion Prototype Block Diagram

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- Prototype finds powerable DTE devices and automatically powers them •
- Midspan configuration for power insertion, can be used to put power on an existing link
- 48VDC/48VDC isolated power module with status and control signals
- Verilog code implemented in a PLD for discovery and power control





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#### Midspan Prototype Measurements, 120 meter CAT 5 cable

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# Midspan Prototype Measurements, 181 meter CAT 5 cable

#### diode non-conducting direction



diode conducting direction



#### **Midspan Prototype Measurements - Discovery Sequence**

A successful set of 256 consecutive discovery cycles, total discovery time is 203ms, the lower trace is n\_turn\_power\_on



close up of the alternating pattern of drive #1 and drive #2, the higher amplitude pulses are the transmit, the lower amplitude pulses are receive (120m. Cable)



### Summary

- The Midspan prototype demonstrates that the common mode discovery mechanism, using the coupled diode identity performs well for discovery and power control
  - the digital technique is robust, works with 180 meters of cable
  - automatically powers up when a successful detection is made
  - automatically powers down when the cable is unplugged
  - does not power legacy equipment
  - Verilog code and prototype schematics are available

#### • more investigation and testing are needed:

- further developments:
  - reduce to single coupling transformer
  - cost reduction: investigate whether the coupling transformer saturation due to DC load current is a viable way of detecting when the cable is unplugged
- need to do the "three fingers" tests
- need to see if power and data are really independent from each other
- need to find if the discovery method can be fooled, ESD, radiated emissions...
- we are looking for people who are interested in performing some tests, we can provide some more prototypes

#### • acknowledgements:

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