IEEE 802.3af DTE Power via MDI
Enhanced I/V Detection Method

Presented by PowerDsine:

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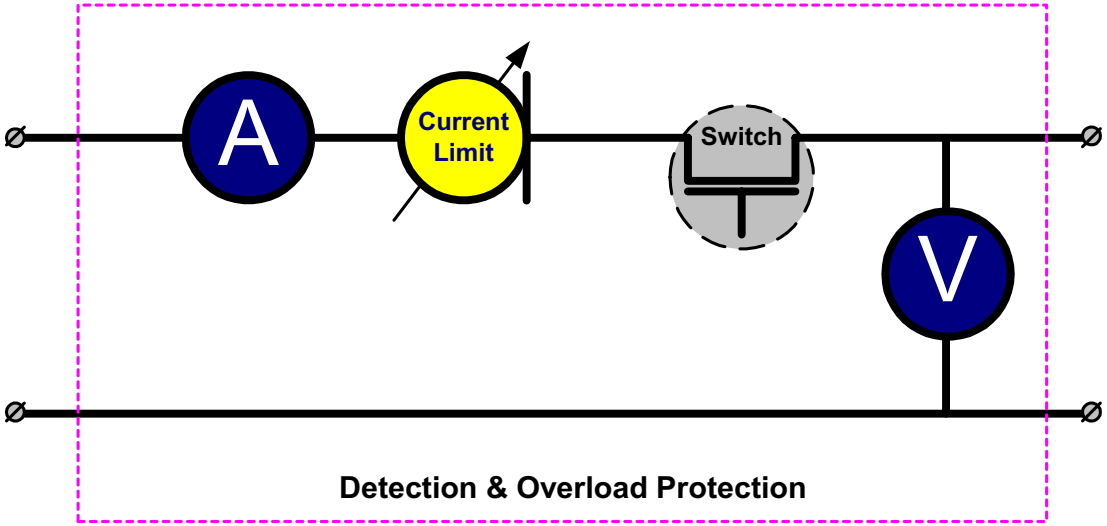
Enhanced Non-Linear PDTE Signature Concept

- PDTE power supply input Capacitor as the signature ID element
- Input Capacitor has to be within a predetermined value range for valid signature (suggested range: 47-470uF)
- Power supply input capacitance >> than capacitance of a non-powered DTE, existence of capacitance in this value range is unique
- PTDE features low leakage current when input voltage is lower than Von (Vs<Von)

Detection & Operation Process

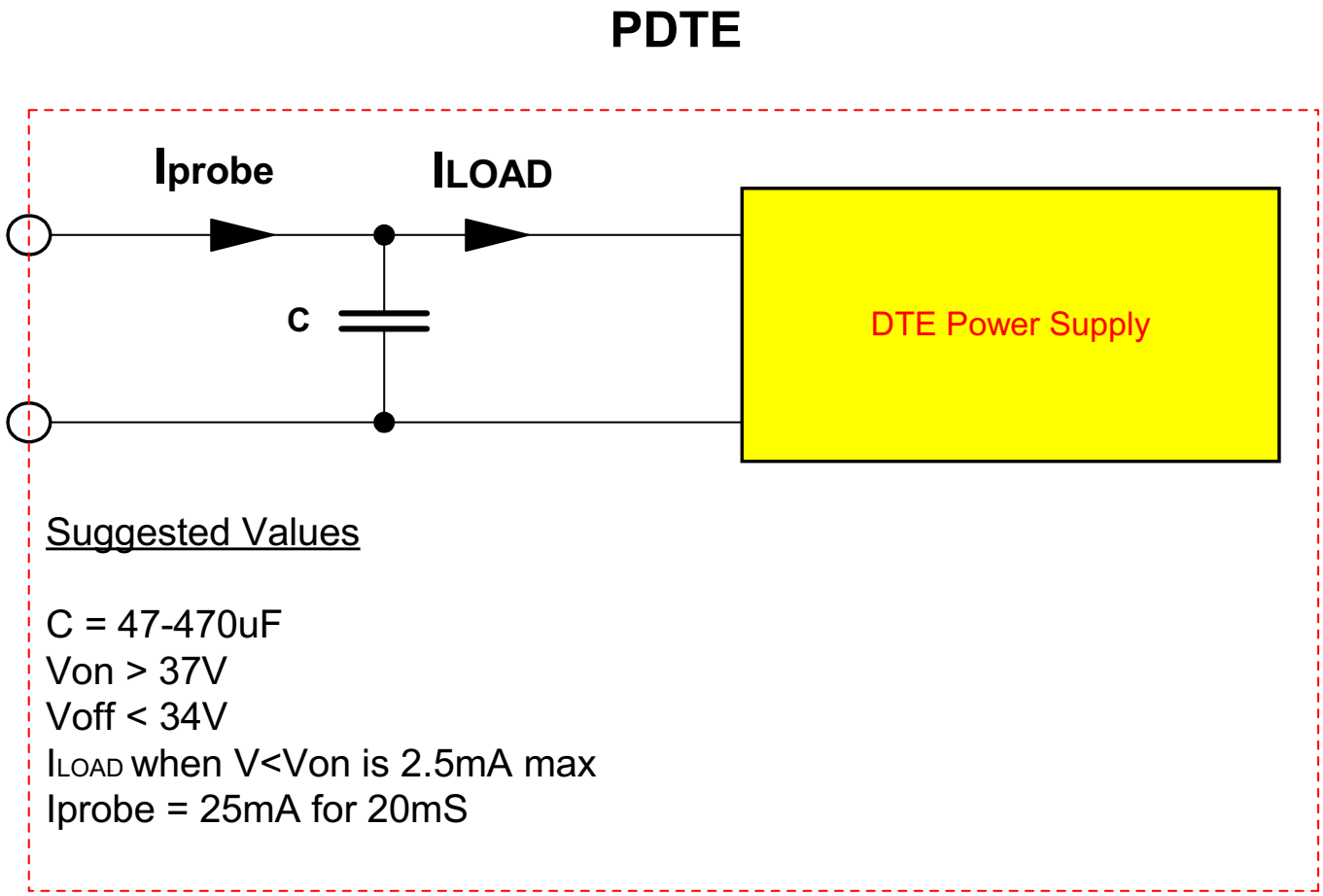
- Probing current limited to 25mA for 20mS
- Measure the developed voltage at start and end
- Calculate voltage change and map results
- If voltage rise within range - activate power
- Deactivate power if I_{LOAD} > Imax or I_{LOAD} < Imin for longer than set interval

Detection & Overload Protection Circuit



Detection pulse (Iprobe) is current limited to 25mA for 20mSec - Average signal power < 3mW

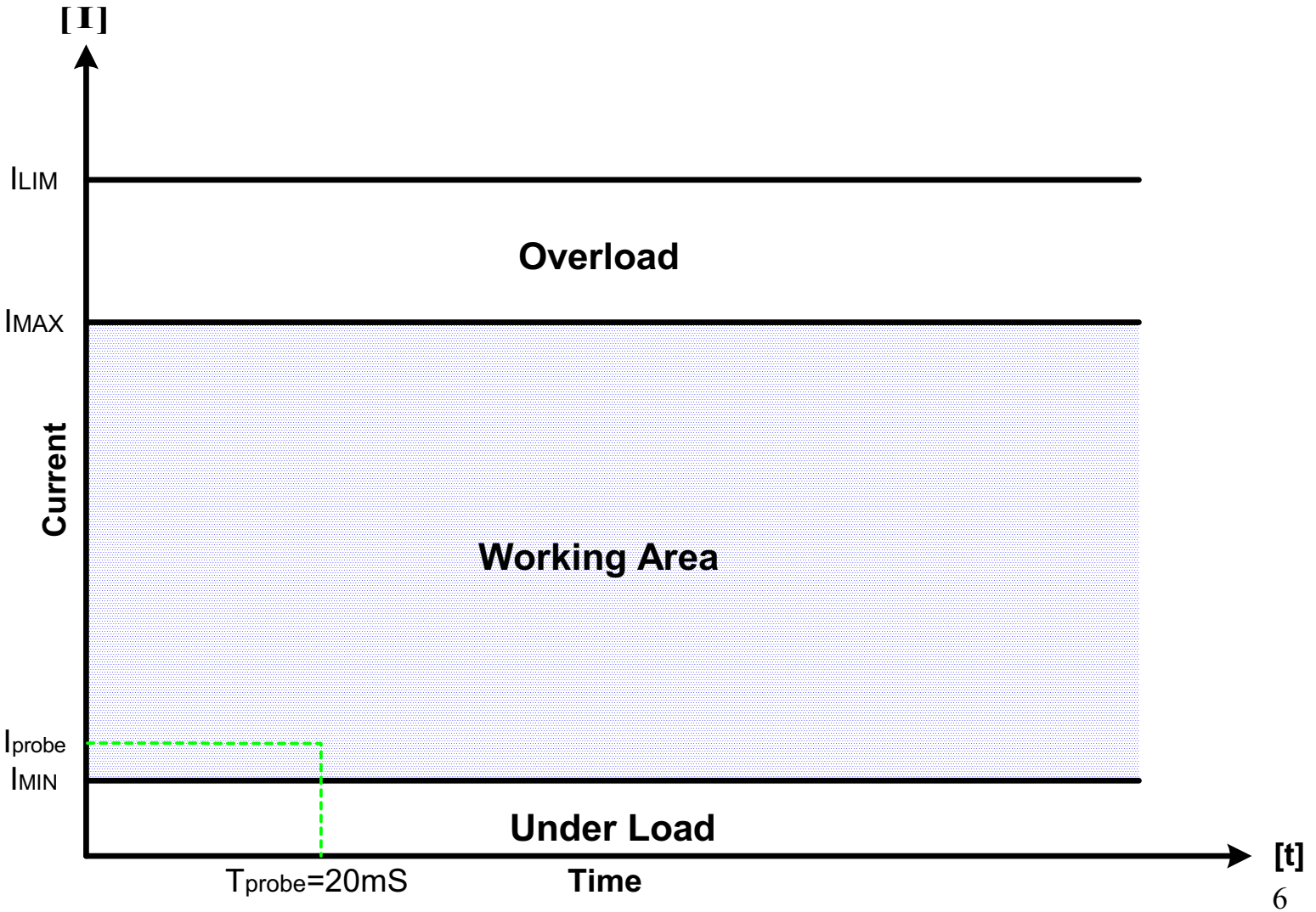
DTE Signature Element



Suggested Values

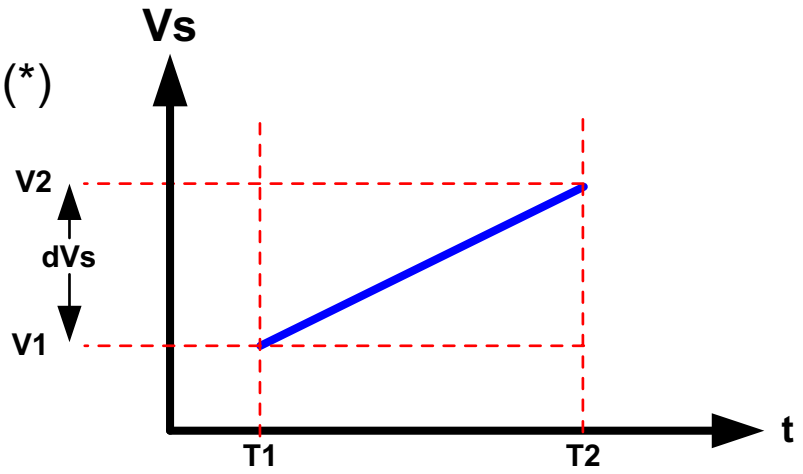
C = 47-470uF
Von > 37V
Voff < 34V
I_{LOAD} when V<Von is 2.5mA max
Iprobe = 25mA for 20mS

Normal Operation Conditions



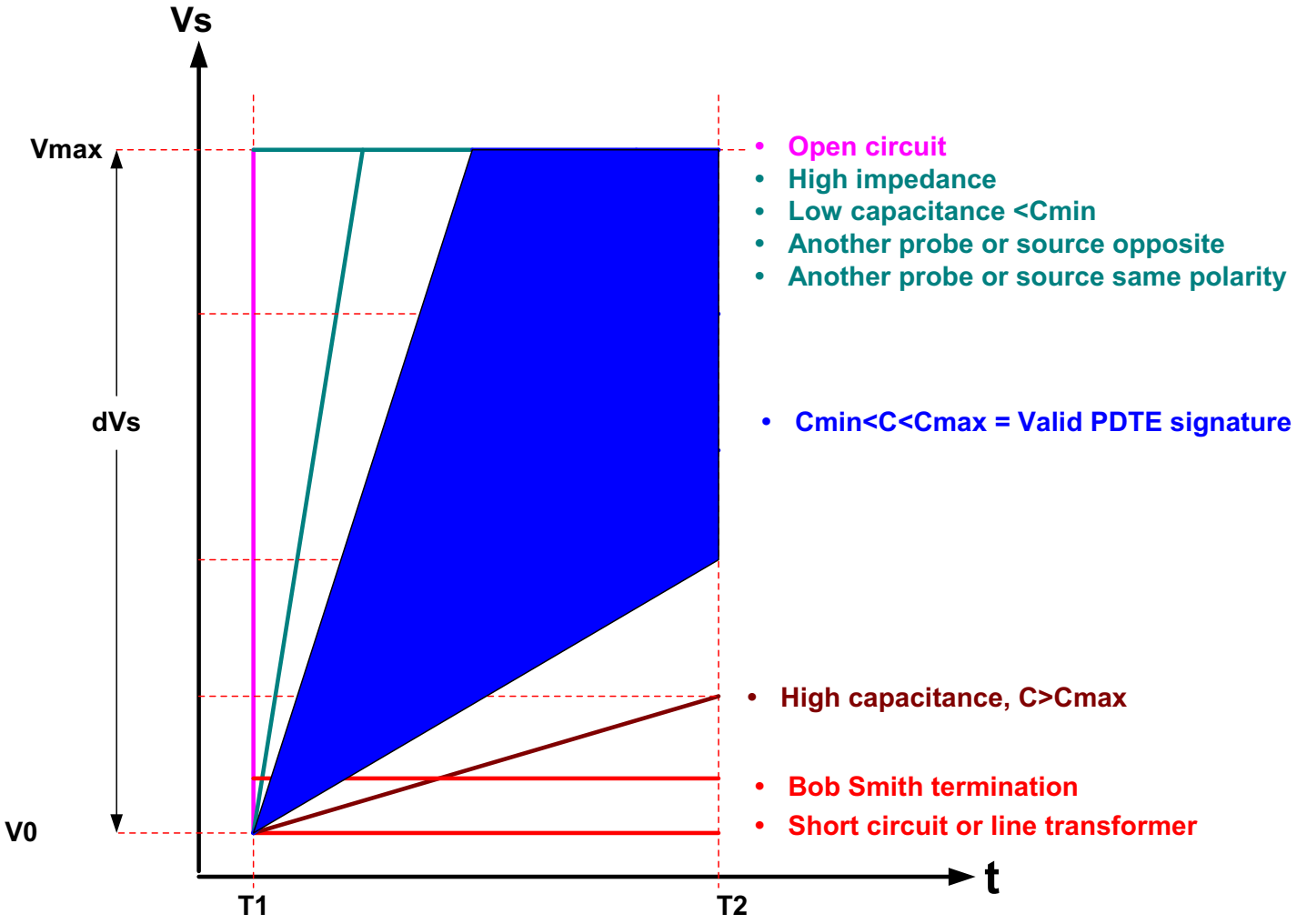
Signature Validation Process

- Measuring the voltage change resulting from charging a capacitor with constant current for predetermined duration
- Measuring Voltage rise, dVs on power source output
- Calculating Cm=Iprobe*dT/dVs
- Signature is valid if 47uF<Cm<470uF (*)



(*)Cmin=47uF to ensure Cmin>>C_{NON_PDTE} (C_{NON_PDTE} may reach 0.1uF), Cmax=470uF, practical input capacitor for 15W DC/DC converter.

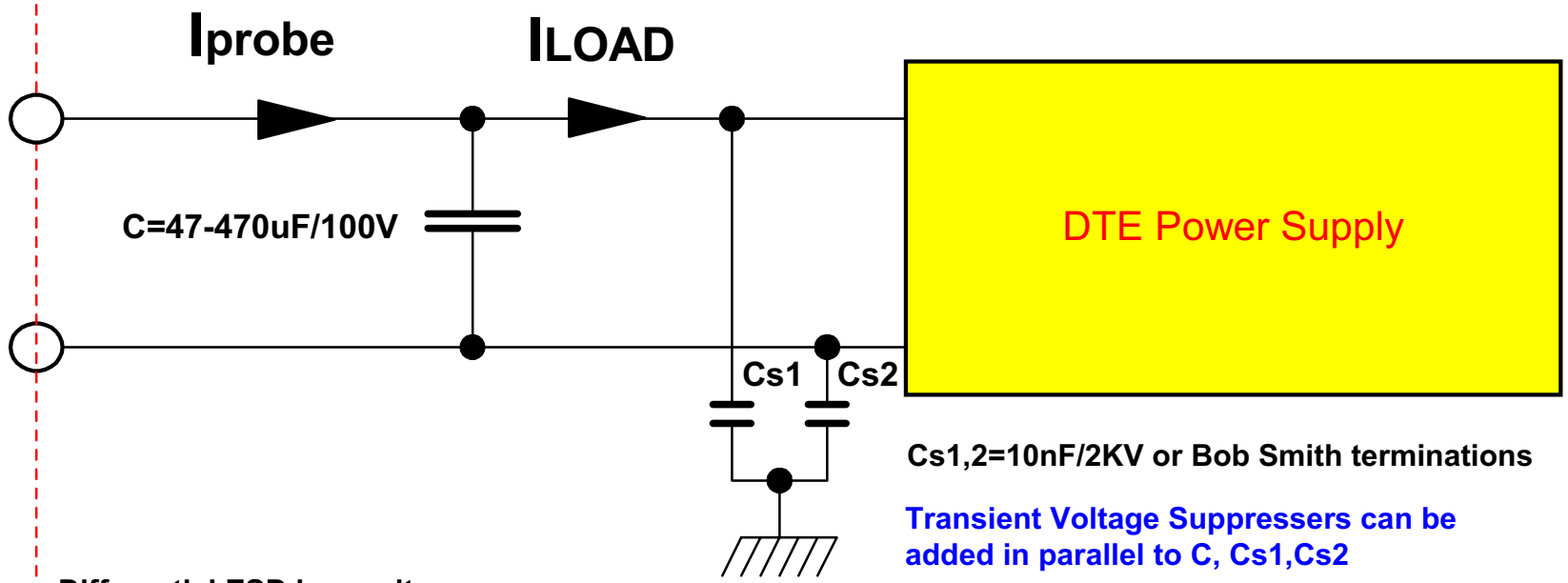
Responses to Detection Probing Signal



Detection Algorithm will reject:

- Open circuits
- Short circuits
- Bob Smith terminations
- Line transformers
- Feeding port with identical or opposite polarity
- Anything that does not present voltage rise within range

ESD Immunity



Cs1,2=10nF/2KV or Bob Smith terminations

Transient Voltage Suppressers can be added in parallel to C, Cs1,Cs2

Differential ESD immunity:
E = Vesd through Cesd discharged by 47uF cap
Ed=k*Vesd*(Cesd/C)^0.5, 0.1<k<1

Common Mode ESD immunity:
E = Vesd through Cesd
discharged by Cs1/2 caps
Ed=k*Vesd*(Cesd/Cs1)^0.5 0.1<k<1

Advantages

- Both the detection & the signature elements are inherent components in existing overload protection and DTE input power supply
- Silicon based solution without magnetics can be easily integrated in existing hardware
- Low AC-impedance ID element functions as noise suppressor
- Voltage rise on 47-470uF cap is higher than on 25KOhm resistor with 25mA @ 20mS signal. Thus the leakage current into the PDTE can be as high as 2.5mA and the use of standard power controllers is possible (I.e. TI/Unitrode, Motorola, etc. 1mA off current)
- Compatible with PDTE Diode Bridge for reversed polarity correction

Operation Flow Chart