IDLE PAIR Discovery Process

Robert Muir

IEEE 802.3af – March 2000

Bringing Intelligence to the Network.

Agenda

- Conclusions from the Dallas meeting
- Open Issues
- MDI Link DC model
- IDLE PAIRS Discovery Process
  - General Description
  - Hardware
  - Pulse Generation and Reception
  - Discovery verification Algorithm
- Conclusions

Conclusions from Last meeting

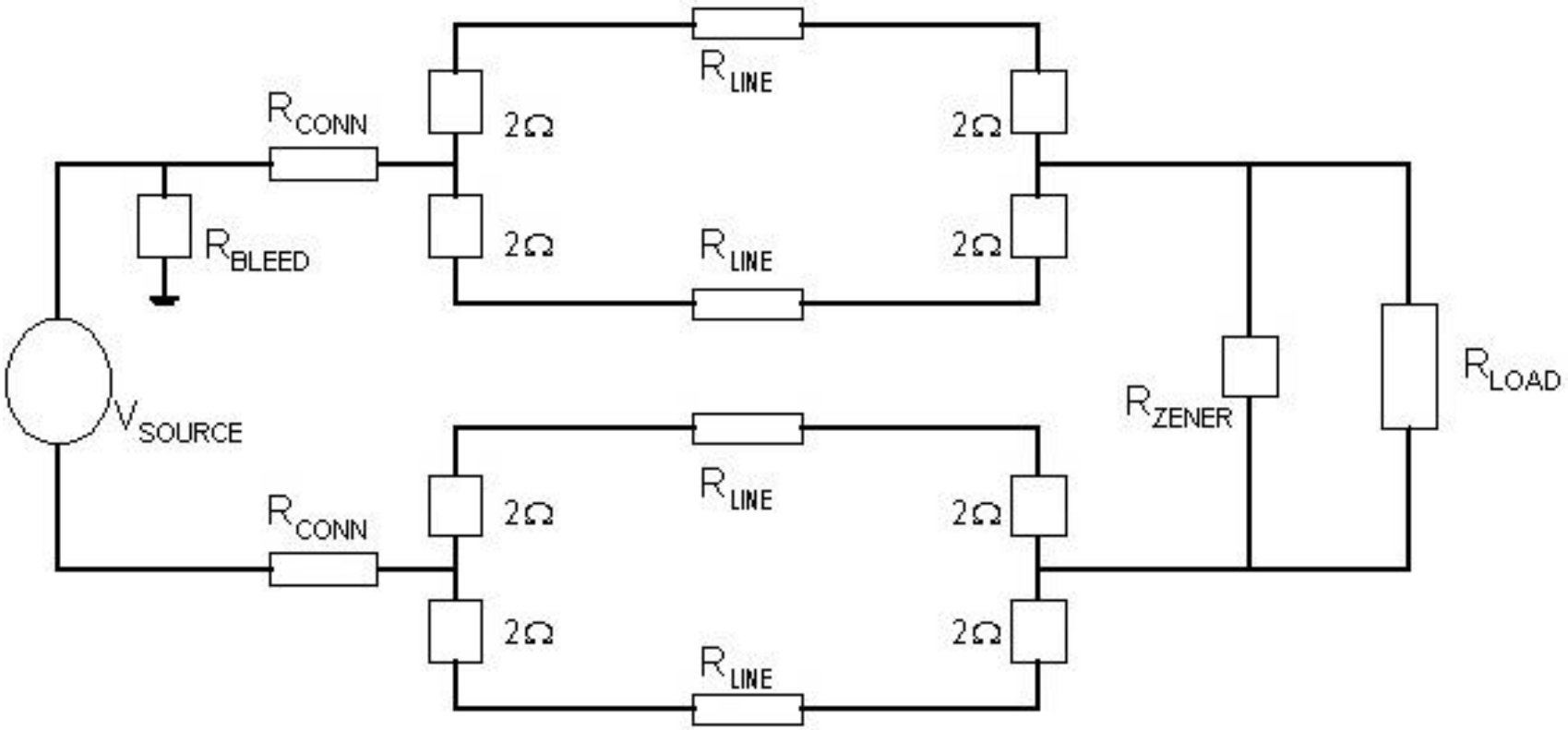
- The following proposal is based on meeting at least the following criteria which were agreed at the last meeting in Dallas.

- The power will be supplied on the Idle pairs or the Data pairs but not both.
- The maximum Voltage will be 60V DC (SELV)
- The discovery process must be robust both in normal operation and in fault condition.
- The discovery process must operate on the pairs that will provide the power feed.
- The link should maintain, if possible, its differential characteristic. (Minimize connector imbalance).
- The minimum power requirement is 8 Watts delivered to the DTE.
- The maximum power requirement is 15 Watts delivered to the DTE.

Open Issues

- Which pair should carry power?
  - All new installations deploy 4 pairs, most existing 2 pair implementations are being retro-fitted.
  - Need to support Mid-Span Power
  - It seems that the IDLE PAIRS are the best choice.
- Reducing the Connector Imbalance.
  - Use 2 ohm resistors at either end of the link as referenced in the draft of 802.9f
- Select the maximum current to flow in the MDI link.
  - Based on the tests carried out by Pulse Engineering and the desire to support 1000Base-T if possible. We need to set this current within the range that today's magnetics can support.
  - A good value would seem to be 350mA.

MDI Link DC Schematic



Equivalent DC circuit for the MDI link while delivering power.

R_{ZENER} and R_{BLEED} are specific to this implementation of the discovery process

MDI Power Capabilities

Case	Watts sourced @ DTE	Current Sourced @DTE	Voltage @DTE	Voltage Drop	Watts required from source
nom	15w	350mA	42.86v	6.18v	17.24w
nom	8w	350mA	22.86v	6.18v	10.19w
wcs	15w	350mA	42.86v	6.94v	17.51w
wcs	8w	350mA	22.86v	6.94v	10.46w

Approximate figures to compare the load and source power

The nominal (nom) figures were found with: R_{BLEED}=47k, R_{CONN}=0.08Ω (4 connectors on each line with a resistance of 0.02 Ω each), R_{LINE}=13.47 Ω , R_{ZENER}=100k.

The worst case figures (WCS) were found with: R_{BLEED}=44.65k, R_{CONN}=0.084 Ω, R_{LINE}=15.43 Ω, R_{ZENER}=95k.

The line and connection resistances are taken from an example in the draft standard of IEEE 802.9f.

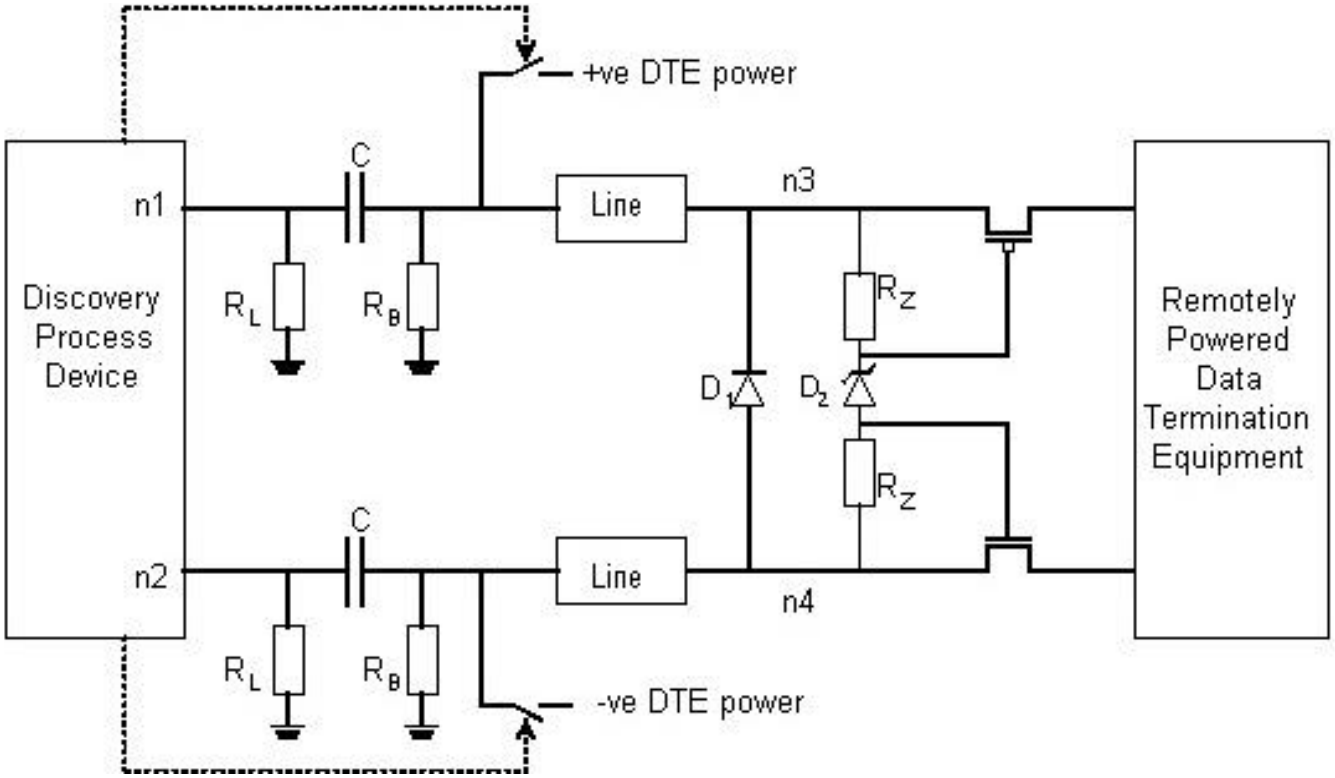
IDLE PAIRS Discovery Process

General Description

- This proposal is based on the presentation given by Dan Dove at the last meeting.
- The scheme attempts to send a pulse both ways through a diode, one will be successful and one will fail.
- The discovery process device is used to both send and receive the pulses and so it knows when it should (and should not) receive pulses.
- If the line is not correctly terminated in a diode then this can be detected. A short circuit will pass both polarities of pulses while an open circuit will pass no pulses

IDLE PAIRS Discovery Process

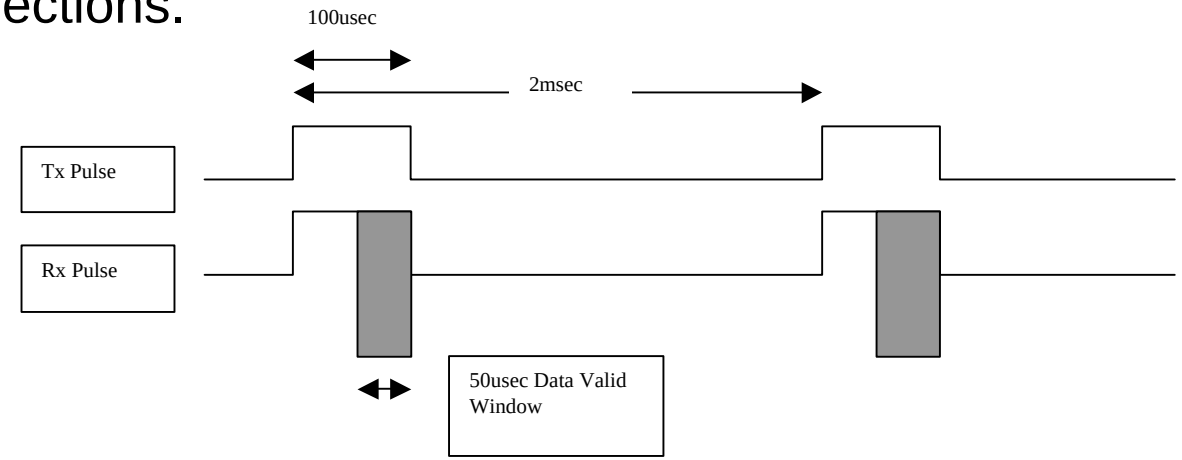
Schematic Diagram



IDLE PAIRS Discovery Process

Pulse Generation and Detection

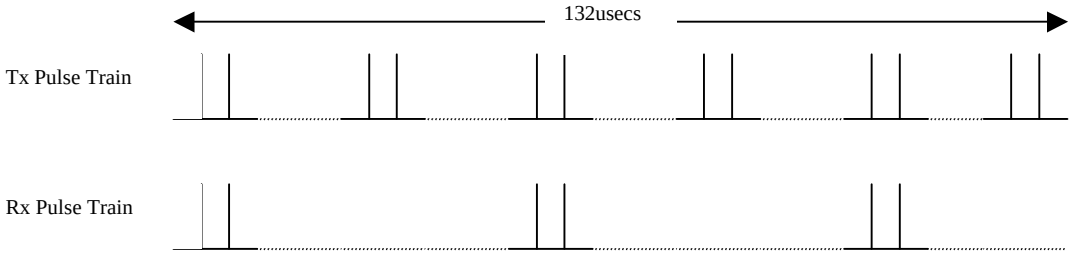
- Each pulse is 100usecs wide and has an amplitude of 2.5V approx.
- These pulses are sent in a group consisting of 11 individual pulses. Each pulse is separated by 1.9msecs.
- The receiver looks at the pulses during the second half of the transmitted pulse and over samples it to ensure that we are receiving valid data. This also eliminates any near end coupling or reflections.



IDLE PAIRS Discovery Process

Discovery Algorithm

- Each 11 pulse word contains a coded random number which changes on every transmit cycle. Eliminate the possibility of two discovery devices applying power to each other.
- The received word is compared to the transmitted word for a match or a ZERO. (A ZERO result is received when the diode is reversed biased because no transmitted pulses are able to pass).
- The transmit direction is reversed every transmit cycle. This is repeated 3 times giving 6 separate transmissions 3 in each direction.
- Only a result of 3 alternating matches and zeros (can begin with either) will give a positive result and apply power. (This also allows us to determine the polarity of the DTE).



IDLE PAIRS Discovery Process

Conclusions

- Low power, low cost solution – low component count
- Allows either Mid-Span or switch based discovery with a single process and a single detector in the DTE.
- Does not require any changes to existing PHY or MAC silicon. Will operate with existing NIC's and Switches.
- Discovery process uses AC coupling on to the link. This removes the need for High voltage MOSFETs on the outputs of the discovery controller and eliminates the need for an extra pin on the controller device to switch them.
- This process is able to detect the polarity of the power required by the DTE. This allows us to interoperate with any type of cable.
- A robust detection algorithm allows us to invariably correctly identify a DTE requiring power.