### Update on Diode Discovery Process

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## Agenda

- Changes made to the Diode Discovery Process
- Simulation Results
- Lab test Results
- Control and Management
- Implementation Options
- Bill of Materials
- Conclusions

- There have been several changes made to the Diode Discovery Process following issues and concerns raised at the last meeting in Albuquerque.
  - The Driver and receiver are now both transformer coupled
  - The Diode Detector is now AC coupled
  - The FET device used to isolate the DTE power supply have been removed and replaced with a diode bridge and series feed diodes
  - The pulse width has been reduced to 4us with a 1us rise time. The pulses are now 50us apart.

- The Driver and Receiver are now both transformer coupled.
  - Meets all isolation criteria for port to port and port to chassis requirements.
  - Use low cost, proven, off the shelf technology.



- The Diode Detector is now AC coupled.
  - The detector is now tolerant any polarity of power supply.
  - The detector is now tolerant of all standard cables found in compliant cable plants.



- FET's replaced by Diode bridge
  - The diode bridge corrects the power supply polarity for connection to the DTE power supply as required.
  - The series feed diodes provide the increased voltage drop to ensure that the discovery pulses never reach the DTE power supply.
  - Series feed diodes also allow for the possibility of OR ing individual channels to provide more power.



- Pulse width had been reduced.
  - Each Pulse is now 4us wide with a 1us rise time
  - The pulses are now 50us apart
  - This has reduced the total time for the discovery process to 3.6ms.





- The schematic above models the simplest implementation for a Mid-Span power solution.
- The results are shown on the next side.

Note that the components to the left of D11 and D12 are only used to mimic those require for the prototype board testing.



- This simulation shows two pulses being generated and received in each direction. The simulation is run as follows:
- P-source (green) generated two 4usec pulses spaced 50usecs apart.
- These pulses are seen across both P\_load (blue) and N\_load (yellow).
- As we are only looking for a signal at the P\_load during a P\_source event we can ignore N\_load in this case.
- The pulse has passed around the circuit through the diode and arrived at P\_load.
- The process above is repeated again but this time with N\_source generating the pulse and N\_load being the load of interest. As can be seen the pulse does not pass through the diode.
- As can be seen from the results there is over a volt of margin between desired signal and no signal. This allows a large noise margin that will improve the robustness of the discovery process.



• The schematic above is the same as in the previous simulation except that it is now coupled to the line through the line side centre taps of the 10/100 magnetic.



 The simulation results show that the Diode Discover process will operate equally well on any of the wire pairs on the MDI link.

## Lab Test Results

- Several test have been carried out on the prototype demo board in the lab.
  - The demo board is built using a PIC micro-controller.
- Pulse response for various cable lengths
- Bit Error Rate test for 10, 100 and Auto Neg
- Testing against the matrix of cases from Kuwai
- Cross talk to data pairs from Discovery pulses

### Lab Test Results Pulse response for 10m and 125m cables In the 125m cases the line is made of 5 25m cables connected through in-line couplers. Pulses are loped back over the cable thus the pulse travels 250m in the 125m cable test and through 16 RJ45 connectors Run: 25.0MS/s Envelope un: 25.0MS/s Envelope ...Ţ... ∆: 640mV @: 940mV M 1.00µs Ch1 J 870mV 10 May 2000 500mV 500mV M 1.00µs Ch1 J 870mV 10 May 2000 Ch1 Ch3 Chil 500mV Ch3 500mV 06:39:44

Bringing Intelligence to the Network.

∆: 640mV @: 940mV

06:21:32

## Lab Test Results

### Bit Error Rate tests (In all the tests below the cable length was 125m).

- In this case there were 3 sets of tests run. •
- **SET #1** •
- i) Two PHYs set at 100 FD to transfer data between them for several million packets. ۲
- ii) Two PHYs set at 100 FD to transfer data between them for several million packets with a • continuous streams of discovery pulses running on the idle pair (4+5, 7+8).
- SET #2 ۲
- i) Two PHYs set at 10 FD to transfer data between them for several million packets.
- ii) Two PHYs set to 10 FD to transfer data between them for several million packets with a • continuous stream of discovery pulses running on the idle pair (4+5, 7+8).
- **SET #3** •
- i) Two PHYs set to run Auto Neg. with changing speed and duplex settings. Repeated over • 100 Auto Neg. cycles. Each cycle consisting of starting Auto Neg., selecting common ability, establishing link, short data transfer at the selected speed and duplex setting and finally bringing the link down.
- ii) Parallel Detect was tested by setting one PHY at a known speed and not enabling Auto ۲ Neg. the other has Auto Neg. enabled but not the same abilities as the first PHY.
- - In All Cases above there were no errors found

## Lab Test Results (Test Requirements Matrix from Kuwai)

Test Condition	Test Result		Comments			
	Spice simulation	Proto Board testing				
Loop Back	Detect	Detect	No power applied			
Full Short	Detect	Detect	No power applied			
Partial Short			Need to define 'partial short'			
Legacy	Detect	Detect	No power applied			
Powering Device	Detect	Detect	No power applied			
Cross talk	Detect	Detect	No power applied – Need to look at 25 pair bundle			
Random Plug	Detect	Detect	Operates correctly			
Telephone	Detect	Detect	No power applied			
ISDN			Not tested			
Test Equipment		Detect	SmartBits, handheld cable tester and HP protocol analyzer/snooper			
Isolation	ОК	ОК	Meets all isolation requirements			
Digital Phone		Detect	Bench tested with a Lucent (Index DT4) phone			
T1/E1	Detect		No power applied			
ATM 25.6						
ATM 155						
Firewire UTP						
Digital PBX			IT would not allow bench test			
Token Ring 4/16		Detect	No power applied – tested with an Olicom card			
Token Ring 100	Detect	Detect	No power applied – tested with an Olicom card			
POTS						





- The state diagram above shows the top-level behaviour of the DTE Diode Discovery Process
- It attempts to show the interaction between the managing system device, the discovery process controller and the power supply fault management controller
- System control is achieved via the 'DTE\_Dis\_En' signal and status is reported via the 'DTE\_discovered' signal. These could be hardware pins or register bits depending on implementation
- The Discover state is where the actual Diode Discovery Process would sit

### Diode Discovery Process Pulse Generation and Detection

- Each pulse is 4us wide and has an amplitude of 2.5V approx.
- These pulses are sent in a group consisting of 11 individual pulses. Each pulse is separated by 50us.
- The receiver looks at the pulses during the second half of the transmitted pulse and over samples it to ensure that we are receiving valid data. This also eliminates any near end coupling or reflections.



# Diode Discovery Process

### **Discovery Algorithm**

- Each 11 pulse word contains a coded random number which changes on every transmit cycle. Eliminate the possibility of two discovery devices applying power to each other.
- The received word is compared to the transmitted word for a match or a ZERO. (A ZERO result is received when the diode is reversed biased because no transmitted pulses are able to pass).
- The transmit direction is reversed every transmit cycle. This is repeated 3 times giving 6 separate transmissions 3 in each direction.
- Only a result of 3 alternating matches and zeros (can begin with either) will give a positive result and apply power. (This also allows us to determine the polarity of the DTE).



## Implementation Options

- The results obtained from both simulation and lab testing suggest the diode discovery process could be implemented in several ways.
  - Wire pairs 4+5, 7+8 both Mid-Span and Switch based
  - Wire pairs 1+2, 3+6 Switch based (support 10% of market which has two cable plant – declining market)
  - Wire pairs 1+2, 3+6, 4+5, 7+8 would allow two level power supply to a DTE. Supports max. possible power transfer over a single MDI link. Permits use of single protocol and detector type on all wire pairs
  - Wire pairs 1+2, 3+6, 4+5, 7+8 would allow support or 1000BaseTfor future requirements.
- The following slide shows a BOM and cost comparison for some of the options above.





Bill of Materials

		Mid Span (4,57,8)		Signal Pair (1,23,6)		1000BaseT (1-8)	
Diode Detector Circuit (in DT)	E)						
	Unit \$	Qty	Ext Cost	Qty	Ext Cost	Qty	Ext Cost
Diode – BAT 85	0.03	1	0.03	1	0.03	2	0.06
Diode – 1N4002	0.01	6	0.06	6	0.06	12	0.12
Capacitor – 1uF 100V	0.10	1	0.10	1	0.10	2	0.20
Resistor – 100k	0.01	1	0.01	1	0.01	2	0.02
Resistor – 2k	0.01	1	0.01	11	0.01	2	0.02
Total			0.21		0.21		0.42
Power Supply Based Controller	<u> </u>						
Control IC / port (8 ports)	0.40	1	0.40				
Isolation Transformer	0.80	1	0.80				
Capacitor - 22uF 100V	0.14	1	0.14				
Resistor - 20k	0.01	1	0.01				
Resistor – 100R	0.01	1	0.01				
Resistor – 1R	0.01	1	0.01				
Total Per Port			1.37				
Switch Based Controller							
Controller in PHY	0.00			1	0.00	2	0.00
Transformer in 10/100 mag 0.40				1	0.40	2	0.80
Capacitor - 22uF 100V	0.14			1	0.14	2	0.28
Resistor - 20k	0.01			1	0.01	2	0.02
Resistor – 100R	0.01			1	0.01	2	0.02
Resistor – 1R 0.01				1	0.01	2	0.02
Total per Port					0.57		1.14
Total System per Port			1 58		0.78		1 56

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### Conclusions

- Diode Discovery Process does not degrade the data carrying capability of the MDI link
- Robust detection algorithm ensures against false detection
- Support 10, 100, 1000 Mbit Ethernet with a single process
- Flexible implementation supports Mid-Span and Switch based DTE discovery and power supply
- Discovery Process operates even on an already powered DTE. Allows redundant power supply
- All for wire pairs can be used in any combination. Supports max. power transfer on the MDI link
- Transformer isolation allows management (if any) to remain on the common side of the isolation barrier
- Low power, low cost solution low component count