Detection Ad Hoc

May 24 and 25, 2001
Work Session Results

Don Stewart
Avaya Inc.

Detection Ad Hoc Attendance May 24, 2001

(No attendance list was circulated. Please check your name for accuracy)

Bachand, Jerry	Avaya
Brooks, Rick	Nortel
Brown, Kevin	Broadcom
Burton, Scott	Mitel
Darshan, Yair	PowerDsine
Diab, Wael	Cisco
Dwelley, Dave	Linear Tech
Heldman, Ronen	PowerDsine
Hemmah, Steven	TI
Hinrichs, Henry	Pulse
Huynh, Thong	Maxim
Inn, Bruce	Micrel
Ish Shalom, Ran	Avaya
Jetzt, John	Avaya
Karam, Roger	Cisco
Kohl, David	SEI
Leo, Lisa	Tyco
Levy, Avinoam	PowerDsine
Lynch, Brian	TI
Rasimas, Jennifer	Nortel
Schwartz, Peter	Micrel
Stewart, Don	Avaya

Detection Ad Hoc Attendance May 25, 2001

(No attendance list was circulated. Please check your name for accuracy)

Bachand, Jerry	Avaya
Brown, Kevin	Broadcom
Burton, Scott	Mitel
Darshan, Yair	PowerDsine
Diab, Wael	Cisco
Dwelley, Dave	Linear Tech
Heldman, Ronen	PowerDsine
Hemmah, Steven	TI
Hinrichs, Henry	Pulse
Huynh, Thong	Maxim
Inn, Bruce	Micrel
Ish Shalom, Ran	Avaya
Jetzt, John	Avaya
Jackson, Steve	Nortel
Karam, Roger	Cisco
Kohl, David	SEI
Leo, Lisa	Tyco
Levy, Avinoam	PowerDsine
Lynch, Brian	TI
Rasimas, Jennifer	Nortel
Schwartz, Peter	Micrel
Stewart, Don	Avaya
Vergnaud, Gerard	Alcatel

Target Work Item List and Status

- Need to discuss/agree on current bands/levels
  - *75% vote accomplished*
- Discuss/agree on timing limits
  - *75% vote accomplished on classification time*
- Refine thoughts around the “attempted” part of: “The standard should require that base detection shall be attempted before optional classification”
  - *75% vote accomplished*
- Discuss ideas on PSE-PSE-PD detection
  - *~ 75% vote accomplished*
- Walk through Detection source material
  - *Did not get to*

Classification Currents, Voltages - Voting

Stage 1 Voting

CLASS	**Proposal 1**	**Proposal 2**	**Proposal 3**	**Proposal 4**	**Proposal 5**
Volt range	18-24v	19-21	19-21	TBD	TBD
0 (25K ohm)	(na)	(na)	(na)	(na)	(na)
1	12.5-14.5ma	2-3	8-10	11.1-13.0	8.6-10.75
2	16.5-18.5	4-5	12-14	15-17.5	11.94-14.93
3	20.5-22.5	6-7	16-18	20.1-23.4	16.59-20.74
4	24.5-26.5	8-9	20-22	27.0-31.3	23.04-28.8
5	28.5-30.5	10-11	24-26	36.0-41.7	32-40
For	3	0	2	10	11
Against	7	12	5	2	0
Abstain	2	0	4	0	2

Current the PD Exhibits

Classification Currents - Voting

CLASS	Proposal 1	Proposal 2		Proposal
Volt range	TBD	TBD		TBD
0 (25K ohm)	(na)	(na)		(na)
1	11.1-13.0ma	8.6-10.75ma		9-11ma
2	15-17.5	11.94-14.93		12-15
3	20.1-23.4	16.59-20.74		17-21
4	27.0-31.3	23.04-28.8		23-29
5	36.0-41.7	32-40		32-40
For	6	7		
			For	15
			Against	0
			Abstain	0

Current the PD Exhibits

Significant Result

Stage 2 Voting
(vote for one)

Stage 3 Voting

Classification Voltages - Voting

CLASS	Proposal 1	Proposal 2	Proposal 3
Volt range	**19-21**	**18-24**	**15-20**
0 (25K ohm)	(na)	(na)	(na)
1	9-11 ma	9-11 ma	9-11 ma
2	12-15	12-15	12-15
3	17-21	17-21	17-21
4	23-29	23-29	23-29
5	32-40	32-40	32-40
For	**1**	**5**	**10**
Against	**12**	**7**	**1**
Abstain	**1**	**1**	**3**

⇦ Voted on this row

Significant Result

Timing Limits for Single Jack Insertion (May 24)

- #1 -Time from jack insertion to reaching > 44*volts available to standard load: <1.0 sec
  - Complete 25K ohm basic detection: < 500 ms
  - Complete Class 2-5 classification: < 100 ms (from completion of discovery method)
  - For__2___, Against__13___,Abstain_1____

Eliminated

- #2 -Time from jack insertion to reaching > 44* volts available to standard load: <1.0 sec
  - Complete 25K ohm basic detection: < 500 ms
  - Complete Class 2-5 classification: < 50 ms (from completion of slope method)
  - For____7_, Against____2_,Abstain__7____

- #3 -Time from jack insertion to reaching > 44* volts available to standard load: <1.0 sec
  - Total duration must be <= 1.0 sec with maximum PD capacitance attached
  - Duration of class 2-5 phase classification is < 50 ms
  - For___10__, Against__5___,Abstain__1____

- #4 -Time from jack insertion to reaching > 44* volts available to standard load: <3.0 sec
  - Total duration must be <= 3.0 sec with maximum PD capacitance attached
  - Duration of class 2-5 phase classification is < 50 ms
  - For___4__, Against__6___,Abstain_5_____

No clear mandate

* 44 v as measured as PSE terminals

Timing Limits - Single Jack Insertion (May 25 Vote)

- #1 -Time from jack insertion to reaching > 44*volts available to standard load: <1.0 sec
  - Complete 25K ohm basic detection: < 500 ms
  - Complete Class 1-5 classification: < 75 ms (from completion of discovery method)
  - For___7__, Against___8__,Abstain_7___

- #2 -Time from jack insertion to reaching > 44* volts available to standard load: <1.0 sec
  - Total duration must be <= 1.0 sec with maximum PD capacitance attached
  - Duration of class 1-5 phase classification is < 75 ms
  - For___11__, Against__4___,Abstain___6___

- #3 -Time from jack insertion to reaching > 44* volts available to standard load: <1.0 sec
  - Total duration must be <= 1.0 sec with maximum PD capacitance attached
  - Duration of class 1-5 phase classification is < 50 ms
  - For__3___, Against__9___,Abstain___9___

Withdrawn

- #4 -Time from jack insertion to reaching > 44* volts available to standard load: <3.0 sec
  - Total duration must be <= 3.0 sec with maximum PD capacitance attached
  - Duration of class 1-5 phase classification is < 75 ms
  - For___6__, Against___9__,Abstain___6___

* 44 v as measured as PSE terminals

Timing Limits - Single Jack Insertion (May 25 Vote)

- #1 -
  - Complete 25K ohm basic detection: < 500 ms
  - Complete Class 1-5 classification: < 75 ms (from completion of discovery method)
  - For___6__, Against__7___,Abstain_7___

- #2 -
  - Total duration must be <= 1.0 sec with maximum PD capacitance attached
  - Duration of class 1-5 phase classification is < 75 ms
  - For__10___, Against__5___,Abstain____6__

- #3 -
  - Total duration must be <= 3.0 sec with maximum PD capacitance attached
  - Duration of class 1-5 phase classification is < 75 ms
  - For___5__, Against___6__,Abstain___8___

* 44 v as measured as PSE terminals

Timing Limits - Single Jack Insertion (May 25 Vote)

- #1 -
  - Complete Class 1-5 classification: < 75 ms (from completion of discovery method)
  - For___15__, Against__1___,Abstain__5__

Significant Result

* 44 v as measured as PSE terminals

Clarification of a May 23 Vote

- On May 23, we approved (>75%): “The standard should require that base detection shall be attempted before optional classification”
- We refined thoughts around the “attempted” part of this; what are the requirements on the result of the attempt?
- Base detection shall be successful before optional classification is attempted
  - For___17__, Against__0___,Abstain__1___

Significant Result

Clarifying Vote on Class Definitions

Note: Maximum Power levels at input to PD

CLASS	#1
0 (25K ohm)	0.44 - 12.95 W
1	0.44 - 3.84 W
2	3.84 -6.49 W
3	6.49 - 12.95 W
4	Future Use
5 (new)	Future Use
For	18
Against	1
Abstain	1

Tries to mimic earlier approved definitions

Significant Result

PSE-PSE-PD (May 25th)

- Option 1: Continue pursuit of solution in PD.
  - For__3___, Against___14_,Abstain__5___

- Option 2: Pure cadence fix. Spare pair PSE must have a new "no-voltage-applied" wait-state between each detection attempt with duration of > 2x and < 2.5x the specified maximum detect time (TBD).
  - For___6__, Against__7___,Abstain_9____

- Option 3: Cadence fix with open-circuit escape. Same as option 2, but optionally the PSE does not do a wait-state after an open-circuit result of a detection attempt. NOTE: Tmax would be relaxed for this contingency.
  - For__16___, Against___0__,Abstain_8____

Significant Result

Remaining Work Items

- How to give PSE-PSE-PD detection “guarantee”
  - *Have agreement on concept. People must verify.*
- Timing for single jack detection - total time
- Walk through Detection source material
  - Useful but optional. Could (will) incorporate agreements to best ability and give to Editor