

AC Disconnect & more...

Roger Karam

Las Vegas Interim

May 2002

Testing Summary

- **Tests covered AC Disconnection and DC Detection**
- **No Apparent Show Stoppers**
- **Biggest Concern is Noise Affecting Ethernet's Integrity and Interoperability**

Standard does not define the AC component of the "dc detection" or Disconnection signals

Standard does not define how to test PSE or PD

- **Recommend a More Conservative Spec. that Keeps the feel of an Ethernet port the same, (PSE Vs Legacy) and makes Interoperability testing a Low Entropy process.**

Tests conducted

Test No.

- 1. Economic Feasibility**
 - **Shared AC Vs single-port AC implementation**
- 2. Noise Immunity**
 - **EFTB, Radiated, AC line coupling**
 - **PD (powered) tolerance to AC signal**
- 3. Minimum PD load for AC Vs DC schemes**
- 4. Inrush into PSE when PD powered from wall**
- 5. Safety - SELV Requirements**
- 6. Basic confirmation of AC Scheme**
- 7. Interaction of signal rise-time & PD power input load**
- 8. PSE-PSE connections**
 - **DC Detection Signal**
 - **AC Disconnection Signal**

Test 1: Economical Feasibility

Concern:

- **Shared AC scheme is Economically Feasible but I have technical concerns**
- **Single-port AC implementation is technically OK but costs much more -expensive cap per port... More circuitry is need to control the AC signal...**

Recommendation:

- **More work required.**

Yes to v3.1

Test 2: Noise Immunity

Concern:

- PD analog immunity to interference
- This is NOT directly related to the AC disconnect.

Recommendation:

- Revise PSE noise spec?. Or Spec a PD's tolerance to the supply ripple that it can encounter from different Supplies out there and still have a clean analog performance, we worried about data alone so far.
- Need a way to verify compliance?
- Injecting noise from 10's of Hz into Khz a challenge when done on the power supply.

Yes to v3.1 – More work required

Noise Immunity Test Overview

Tests

- **EFTB (Electrical Fast Transient)**
- **Radiated Immunity (preliminary data)**
- **AC line power coupling (preliminary data)**
- **PD Noise tolerance when the PD is powered**

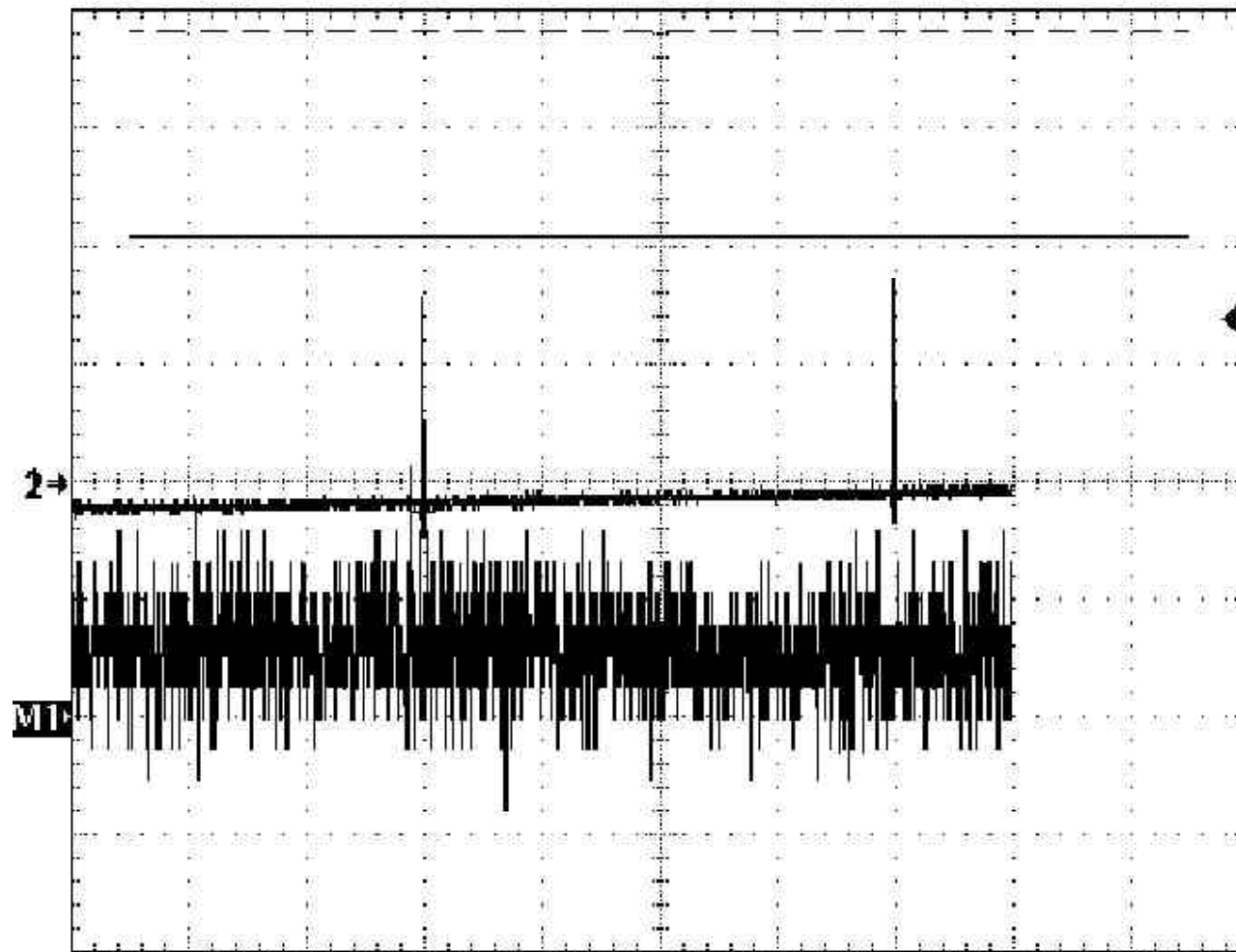
Conclusion

- **AC Disconnection circuit must discriminate based on amplitude and time information**

Noise Immunity EFTB (large time scale)

Tek **Stop** 5.00MS/s

3 Acqs



Δ: 8.7 V
@: 20.4 V

C1 Pk-Pk
220 V

C1 Rise
171ns
Low signal
amplitude

2→

M1

Ch1 100 V Ch2 100 V M 50.0μs Ch1 138 V

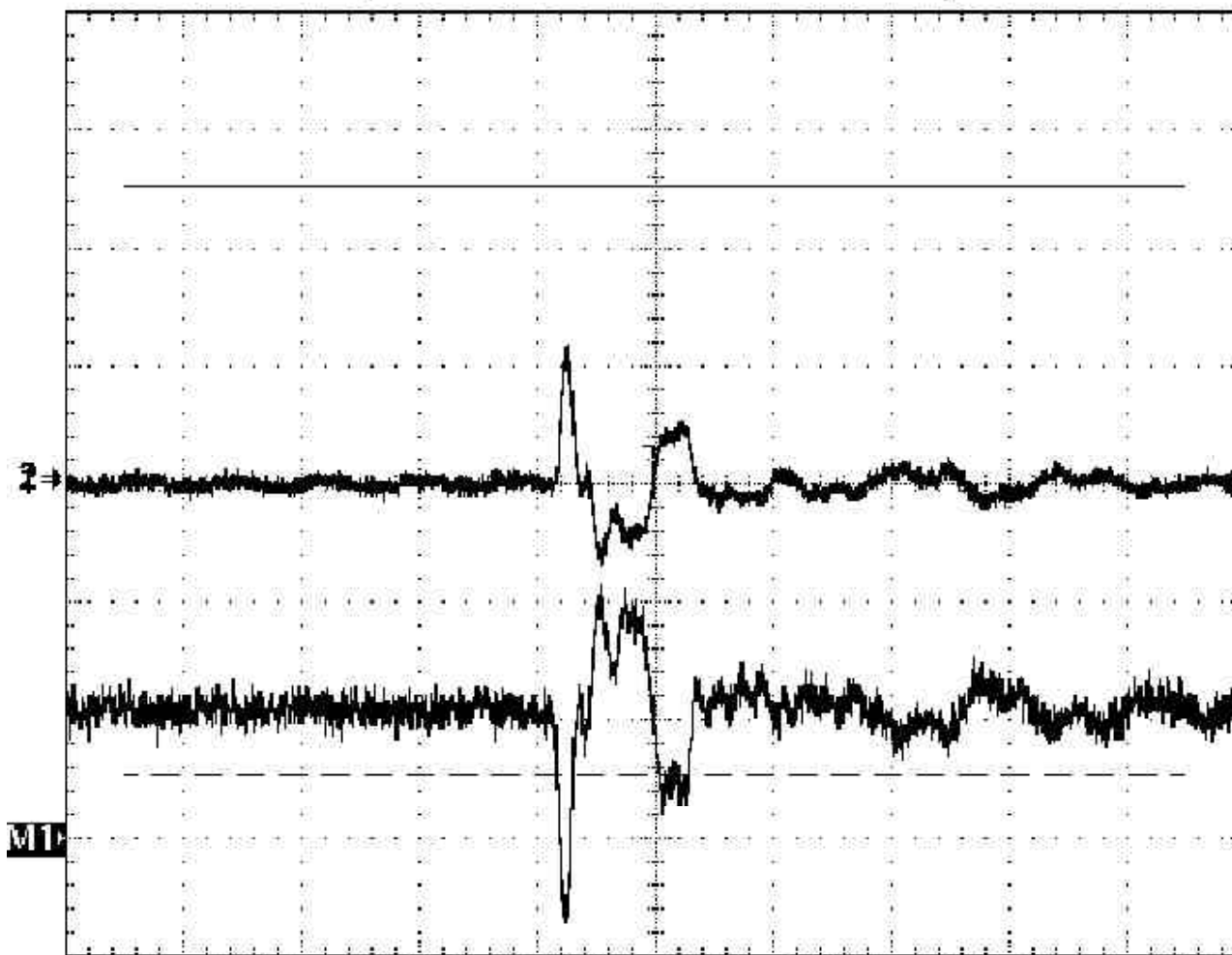
Math 5.00 V 50.0us

22 Mar 2002

12:38:47

Noise Immunity – EFTB Zoom-In

Tek Run: 2.50GS/s Sample



Δ : 10.00 V
@: 11.04 V

C1 Pk-Pk
85 V

C1 Rise
2.795ns
Low signal
amplitude

Ch1 50.0 V Ch2 50.0 V M 100ns Ch1 J -2 V

Math1 2.00 V 100ns

22 Mar 2002

12:45:07

AC-Cord Coupling

- **Preliminary data shows that Line coupling can be as high as 3v differential, into a High impedance “power input”**
- **Used 50ft of cat-3 and a power cord.**
- **With Low impedance it can be in the high 10’s of mv**
- **Again, using a good discriminator to detect the AC signal, and staying away from the line frequency will help**

Radiated Immunity

- **Preliminary results show that a “power Input “ representing a High Impedance could potentially cause a 800 mv peak-peak differential voltage in the 100mhz region**
- **Low Impedance – No diode+cap kind of input, ie standard Ethernet does not do this**
- **So again we bet on a good discriminator here**
- **We may want to spec the DC-detection to tolerate these conditions**
- **Possible alternate fix to this, is dictating a Min Capacitor in the PD (facing the wire)**

Noise Immunity - PD Noise tolerance

Cisco.com

PD is Powered

- No issues related to AC Disconnection Signal
- Draft 3.0 Noise Spec based on Data tolerance
 - Need to consider analog circuitry
- Example: PSE meets .af D3.0 noise spec, but causes the PD grief in analog (I.e. phone audio hum)
- Need to determine appropriate PSE intrinsic noise specs OR spec the PD tolerance. **HAS ANY ONE TESTED THIS?**

(More work required)

Test 3: Minimum PD load

Concern:

- **Minimum load with DC Disc, 10 mA**
- **Minimum load with AC Disc, 0 mA**
- **This will result in different behaviors in the customer's environment**

Recommendation:

- **May need to spec an Min AC load facing the wire to allow the PD to behave as a minimum load under AC disconnect?**

Is this an issue?

Test 4: Inrush back into PSE

Concern:

- If PD is wall powered & and wall power goes away
- PD will generate inrush back into PSE

Recommendation

- Specify that a PD must not cause damage under this condition by imposing a transient back into the PSE upon removal of a secondary power source. And
- Specify that a PD must Not Force DC Voltage on the wire. (possibly state that a current limited $I < ??$ Voltage may be ok)

Is this covered?

Test 5: Safety

Concern:

- **DC + Ripple must be below SELV**

Recommendation:

- **Here are the advised way to spec this**
- **1. max. 4.4 Vpk-pk OR**
- **2. $(0.1 \times V_{dc})$ Vpk-pk, up to 5 Vpk-pk.**

Yes to v3.1 with recommendation

Test 6: Basic Concept of AC Disc.

Concern:

- Under normal conditions (PSE-PD) AC Disc signal is not a concern
- Provided PD draws power – no issue

Recommendation:

- None required

Yes to v3.1

Tests conducted

Test No.

1. Economic Feasibility
 - Shared AC Vs single-port AC implementation
2. Noise Immunity
 - EFTB, Radiated, AC line coupling
 - PD (powered) tolerance to AC signal
3. Minimum PD load for AC Vs DC schemes
4. Place holder – Inrush into PSE when PD powered from wall
5. SELV Requirements
6. Basic confirmation of AC Scheme
- 7. Interaction of signal rise-time & PD power input load**
- 8. PSE-PSE connections**
 - **DC Detection Signal**
 - **AC Disconnection Signal**

Legacy Standard Ethernet

Switch and NIC are the same 99.9% of the time

In the power world the PSE and PD circuits vary

THE STORY OF ETHERNET TO ETHERNET- WHY INTEROPERABILITY AND TESTING WAS 'EASY'
 WE KNEW TO A GOOD DEGREE OF CONFIDENCE WHAT WAS ON THE FAR END

Size: A	No:	Rev: 12
Sheet: 1 of 1	CISCO SYSTEMS	Revised: 24-Apr-2002
Drawn by: ROGER KARAM		Created: 31-Mar-1999
File: D:\Data\docu\Tsw\in32\phn\legacy.sch		

1.70, 2.60 Edit Sheet 1 of 1

Test 7 - Rise Time

Concern

- Interaction of rise-time and PD power input load
- For rise-times of 10's uSec the EMI profile **May be** affected by the load
- so what load does the PSE vendor test to??

Recommendation

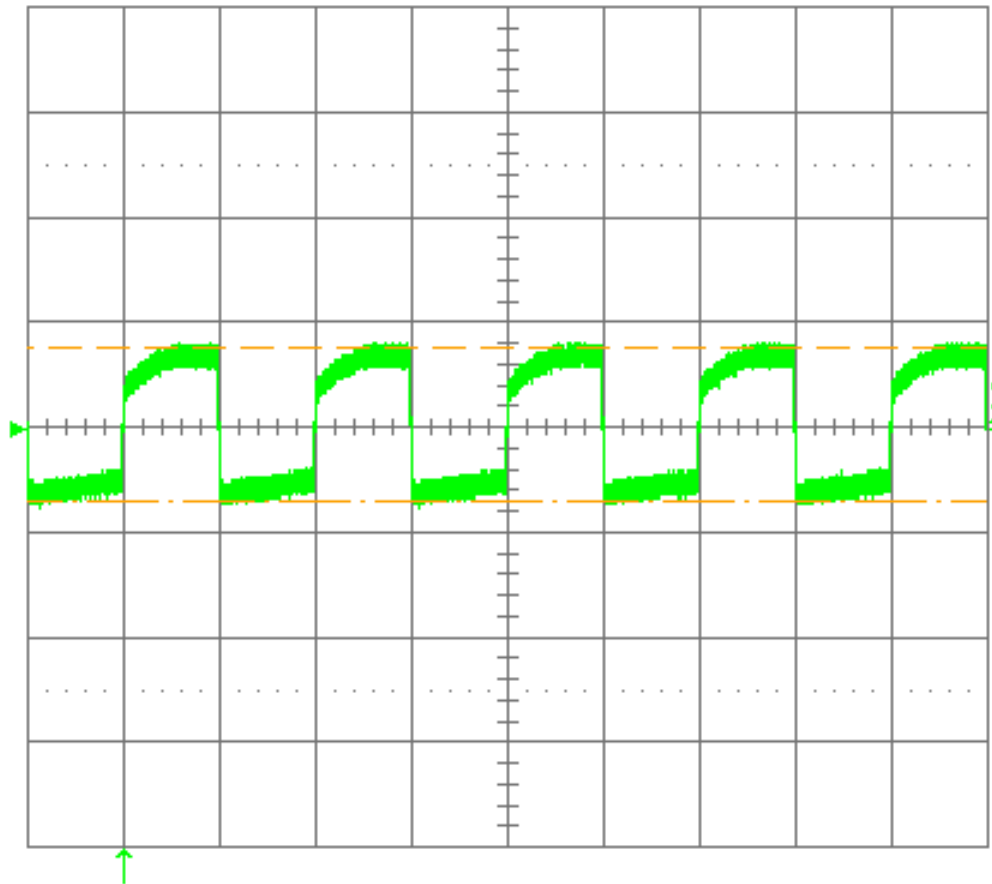
- slow down rise-time to mSec. As large as feasible within the 500mSec detection window

Yes to v3.1 with Recommendation

Rise-time AC Disconnection signal with PD-1

8-Jan-96
6:01:33

3
5 ms
2.00 V
2.92 V



T_{rise} = 150 uSec
PD no. 1 is OFF

5 ms
1 trig only
2 1 V AC $\times \frac{10}{10}$
3 .2 V AC $\times \frac{10}{10}$
4 trig only



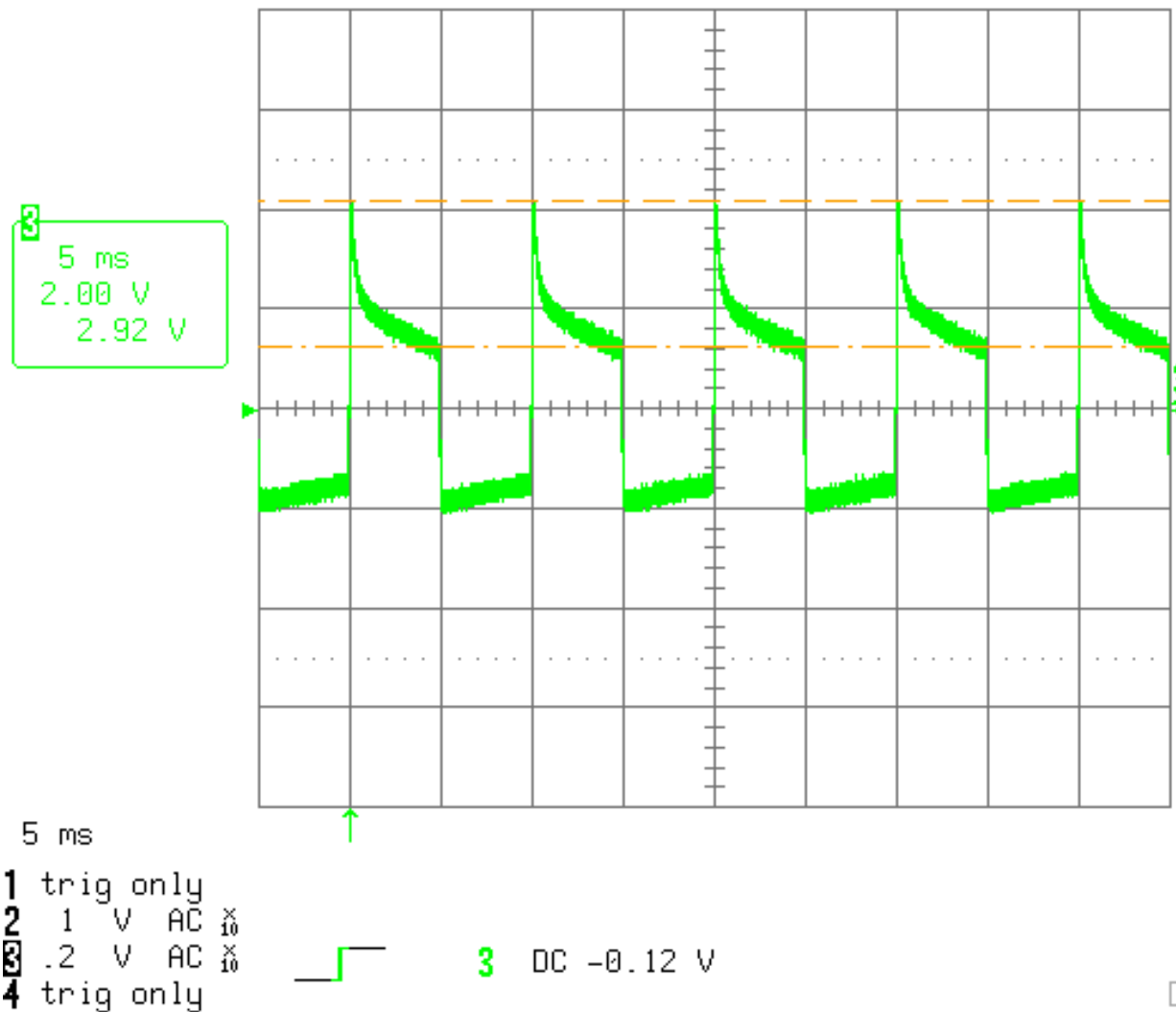
3 DC -0.12 V

20 MS/s

AUTO

Rise-time AC Disconnection signal with PD-2

8-Jan-96
5:59:55

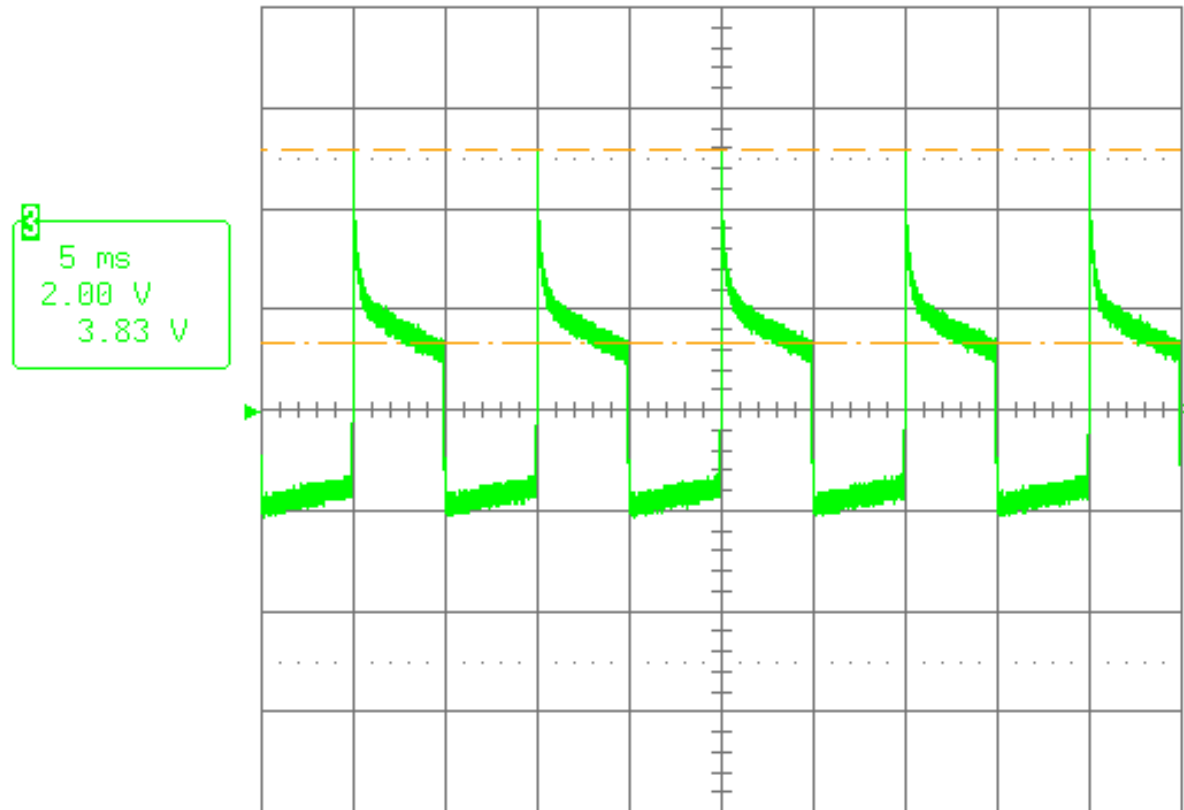


T_{rise} = 150 uSec
PD no. 2 is OFF

**Change in
spectrum due to
PD change**

Rise-time AC Disconnection signal with PD-2

8-Jan-96
5:59:16



T_{rise} = 10 uSec
PD no. 2 is OFF

Spectrum got worse

5 ms
1 trig only
2 1 V AC \times
3 .2 V AC \times
4 trig only



3 DC -0.12 V

20 MS/s

AUTO

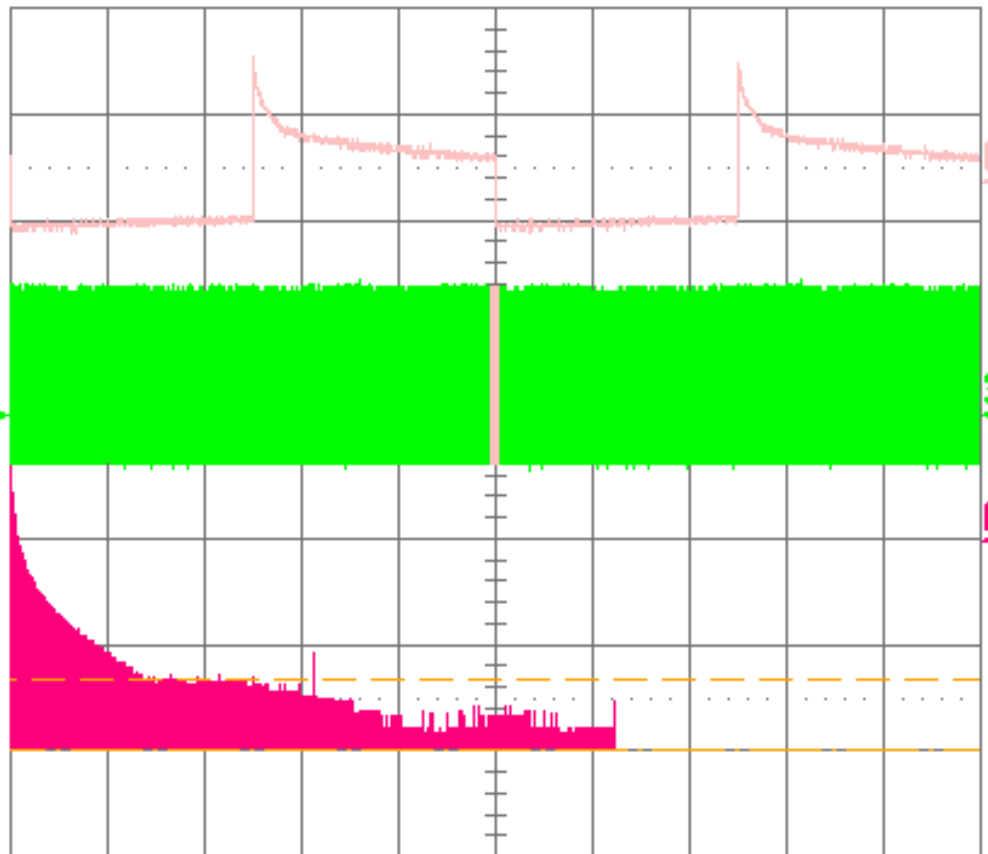
Spectrum for 10us Rise Time

10-Feb-96
0:10:37

3
2 s
5.0 V
3.3 V

A:PS(FFT(3))
10 kHz
20.0 dBm
13.2 dB

3
2 ms
5.0 V
3.3 V



2 s

- 1 trig only
- 2 10 mV 50Ω
- 3 .5 V AC \times
- 4 trig only



3 DC 0.0 V

250 kS/s

STOPPED

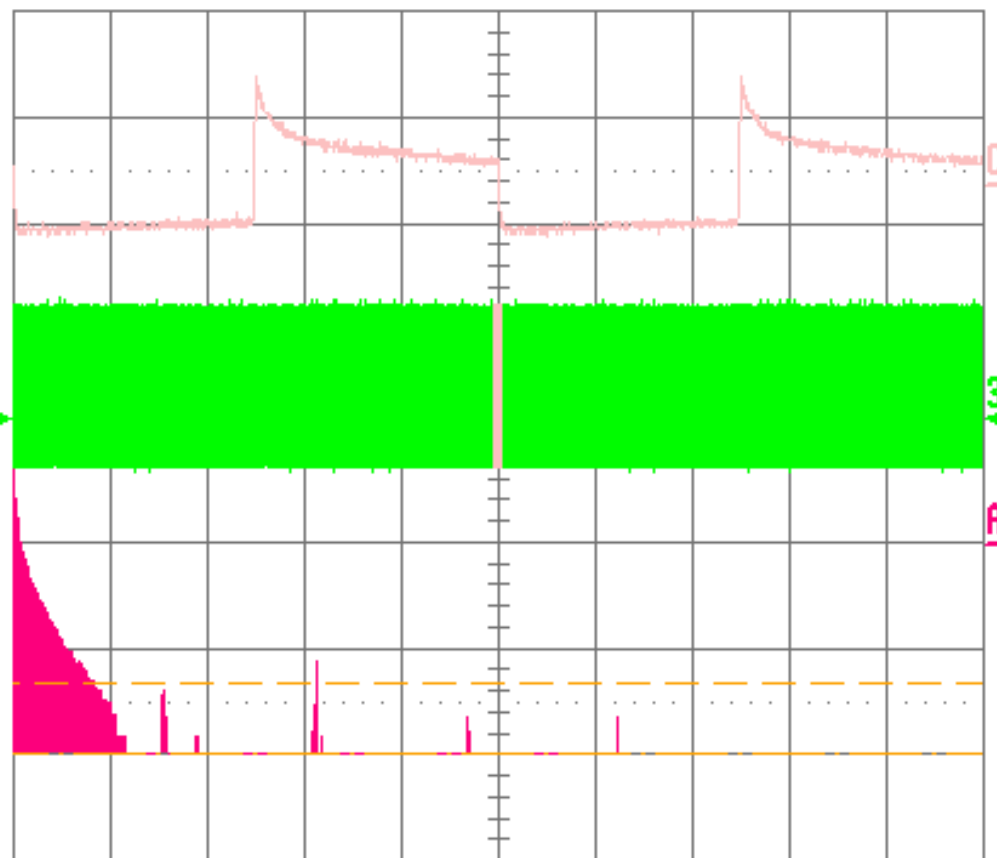
Spectrum for the 150us Rise Time

10-Feb-96
0:30:11

3
2 s
5.0 V
3.3 V

A:PS(FFT(3))
10 kHz
20.0 dBm
13.2 dB

3
2 ms
5.0 V
3.3 V



2 s

- 1 trig only
- 2 10 mV 500
- 3 .5 V AC ∞
- 4 trig only



3 DC 0.0 V

250 kS/s

STOPPED

Spectrum with Trise=1msec

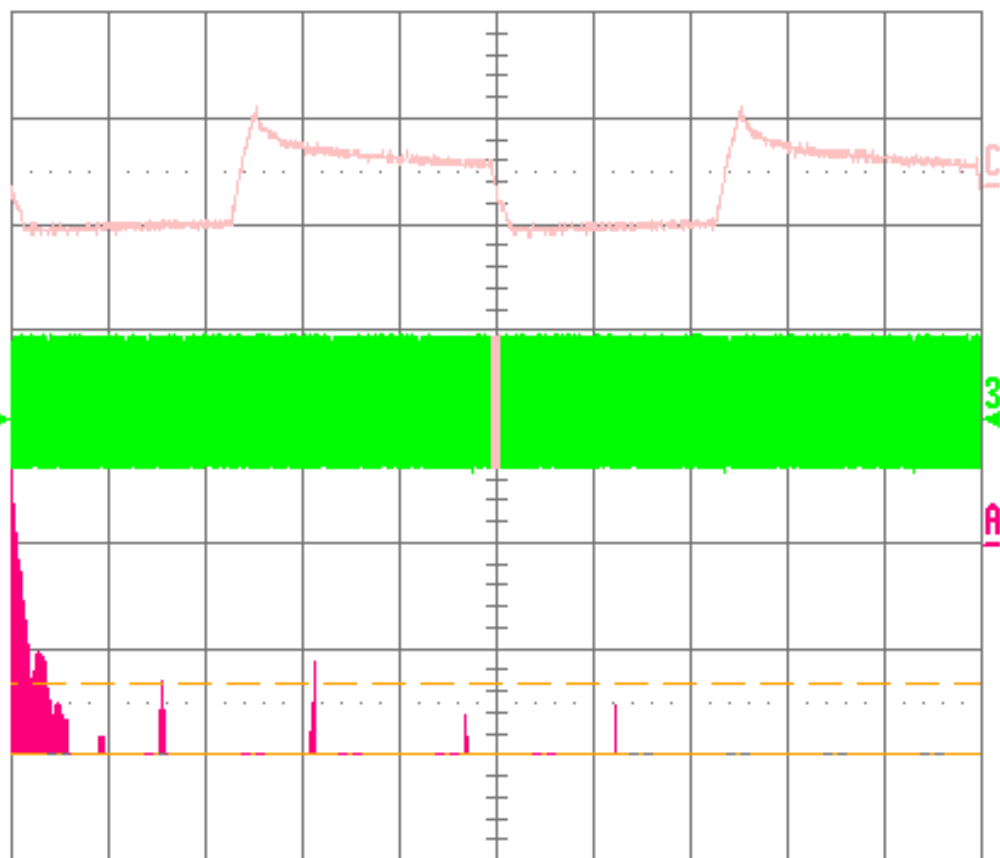
10-Feb-96

0:31:40

3
2 s
5.0 V
3.3 V

A:PS(FFT(3))
10 kHz
20.0 dBm
13.2 dB

3
2 ms
5.0 V
3.3 V



2 s

1 trig only

2 10 mV 50Ω

3 .5 V AC \times

4 trig only



3 DC 0.0 V

250 kS/s

STOPPED

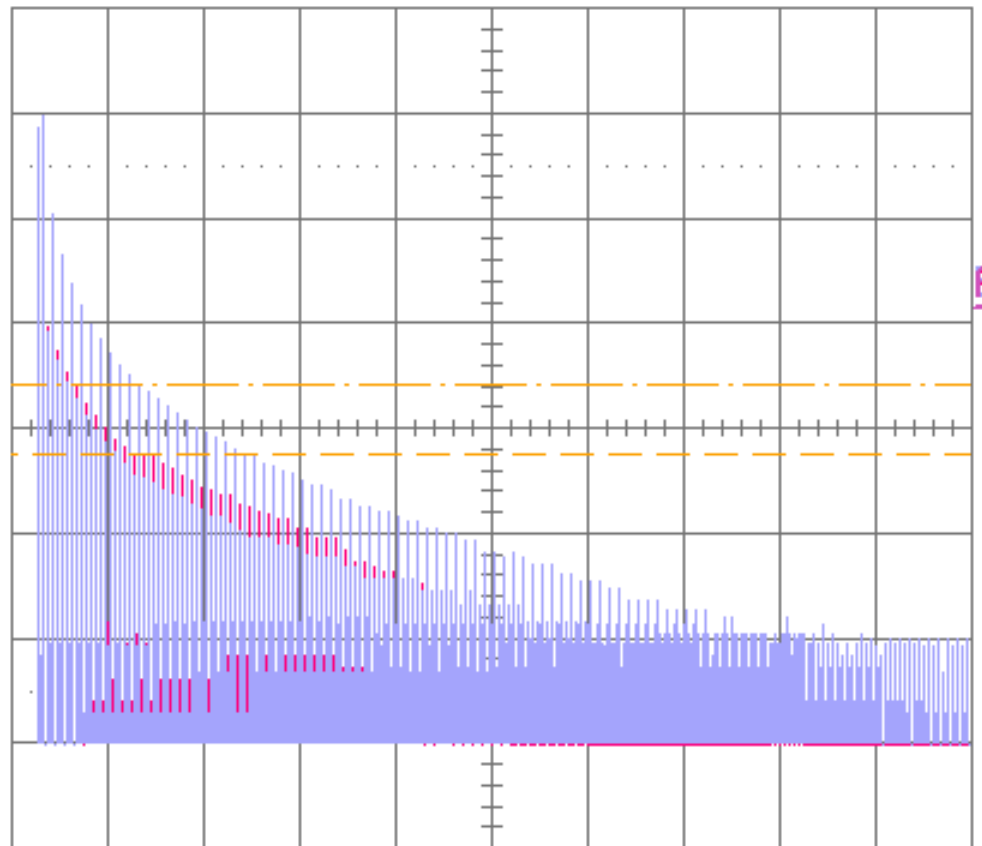
Compare Spectrum for Tr=40us & 150us

10-Feb-96

0:40:34

M1
2 k Hz
9.5 dBm
-6.3 dB

A:PS(FFT(3))
2 k Hz
9.5 dBm
-6.3 dB



2 s

- 1 trig only
- 2 10 mV 50Ω
- 3 .5 V AC \times
- 4 trig only



3 DC 0.0 V

250 kS/s

STOPPED

Rise-time testing summary

- **Draft 3.0 calls for a minimum T_{rise} of 10 uSec**
- **The spec should guarantee interoperability – currently it may not?**
- **Recommend: increase the rise-time to mSec but we need consensus as it affects averaging of detection measurements.**

Test 8 - PSE-PSE DC detection

Concern:

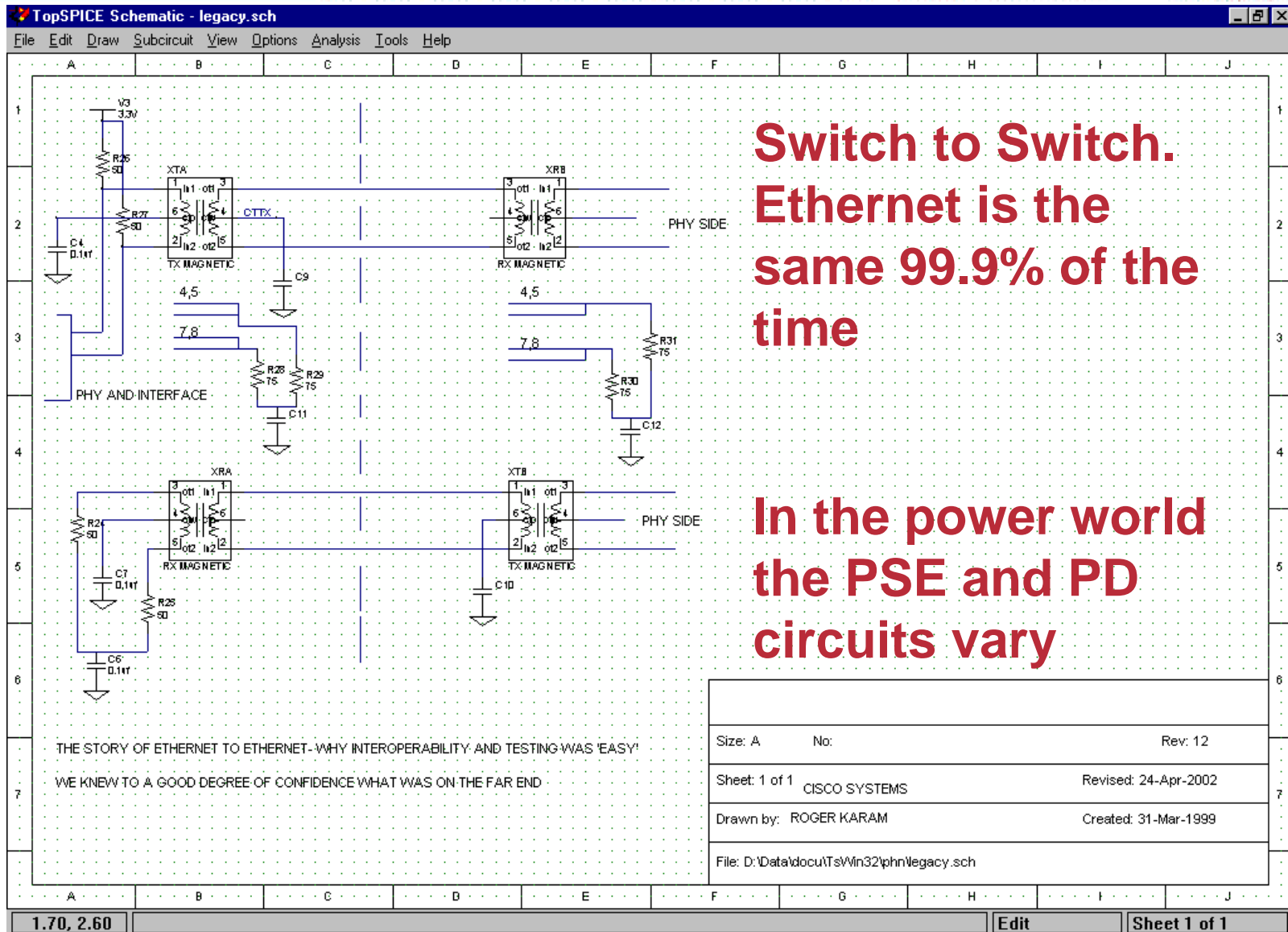
- Is this really a DC detection scheme. It turns out that many implementations are switching rapidly between the two probing voltages (AC) at an unspecified frequency and duty-cycle with aggressive rise-times
- Ethernet interoperability

Recommendation:

- Should not go to 2nd probe voltage until a possible PD is discovered at the 1st probe voltage (preferred solution – real DC)
- Specify the switching rate (not clean)

Yes to v3.1 with Recommendation

PSE – PSE connections Legacy Standard Ethernet



PSE – PSE connections

Legacy Ethernet + power

TopSPICE Schematic - LAGACYPLUS.sch

File Edit Draw Subcircuit View Options Analysis Tools Help

PSE A CASE 7 THE 'LEGACY PLUS' INTEROP QUESTION PSE B CASE 7

PHY SIDE

PHY SIDE

PHY SIDE

PHY SIDE

USING CROSS OVER CABLE OR A STRAIGHT CABLE.

VARYING, AMPLITUDE, FREQ, DELAY, TR - ABOVE ALL CIRCUIT IMPLEMENTATIONS FOR DISCOVERY. WE MUST BE FINE WITH A BUNCH OF CONNECTIONS

CASE 1- PSE TO LEGACY ETHERNET
CASE 2 - PSE TO PSE (ONE IS QUITE)
CASE 3- PSE TO PSE BOTH DETECTING
CASE 4- PSE ONE QUADRANT TO LEGACY.
CASE 5- PSE ONE QUADRANT TO A PSE (QUIET).
CASE 6- PSE ONE QUADRANT TO A SIMILAR PSE BOTH SWITCHING.
CASE 7- PSE ONE QUADRANT TO A HIGH Z PSE BOTH SWITCHING

CASE 8- COMPOUND THIS WITH AC DETECTION LEFT ON!
AND POSSIBLY A FEW MORE CASES ...

PSE's common-mode inputs vary

PSE TO PSE SWITCHING	
Size: A	Rev: 42
Sheet: 1 of 1	Revised: 24-Apr-2002
Drawn by: Roger Karam	Created: 31-Mar-1999
File: D:\Data\docu\Ts\Win32\ac\LAGACYPLUS.sch	

1.65, 2.65

Edit

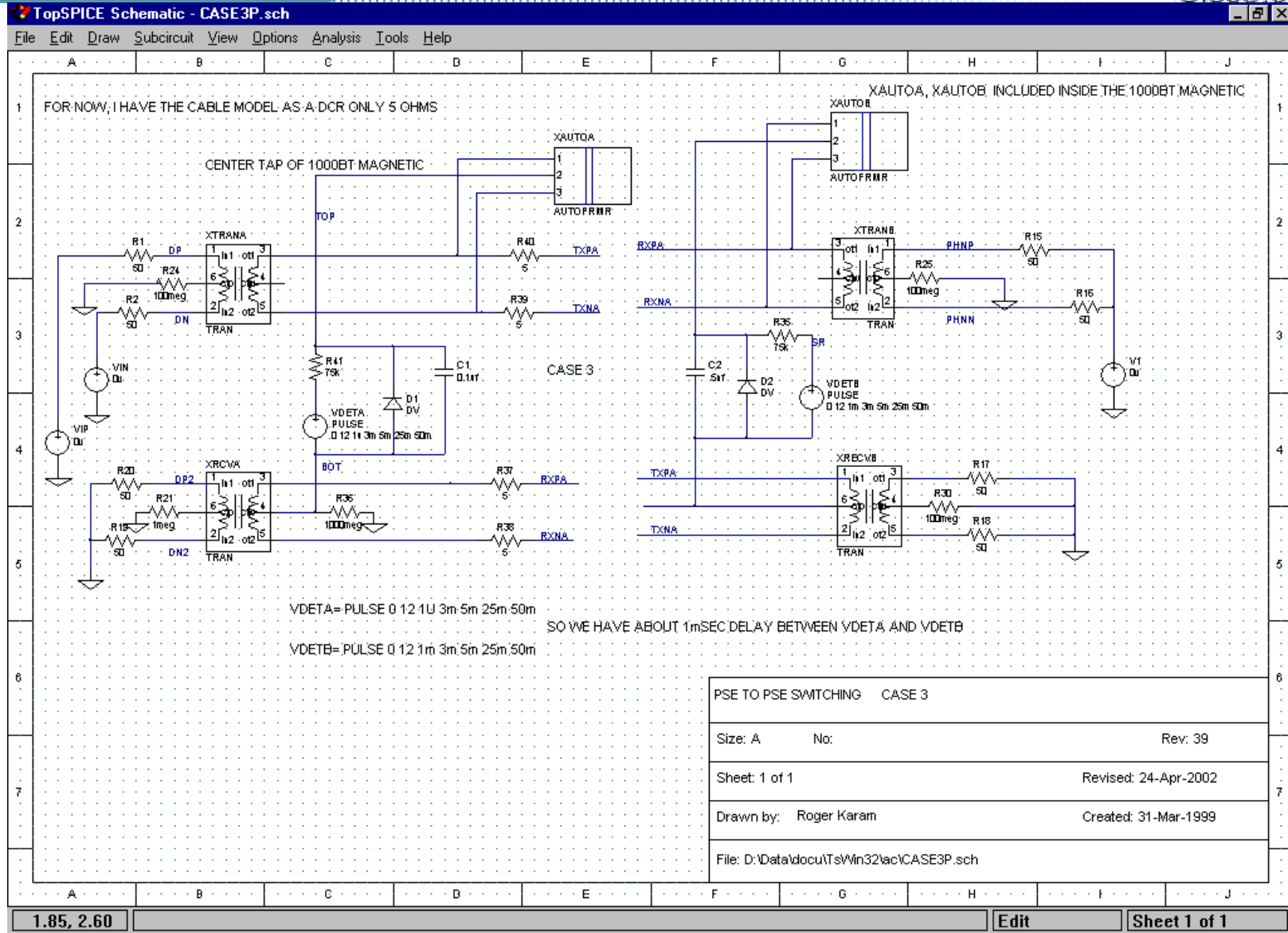
Sheet 1 of 1

PSE – PSE Test Overview

DC detection is actually AC

- **Pick 1 case, two high impedance PSEs**
- **Set frequency and rise-time to mSec (setup 1)**
- **Plotted results (OK)**
- **Changed frequency and rise-time (setup 2)**
- **Plotted results (Big Difference)**

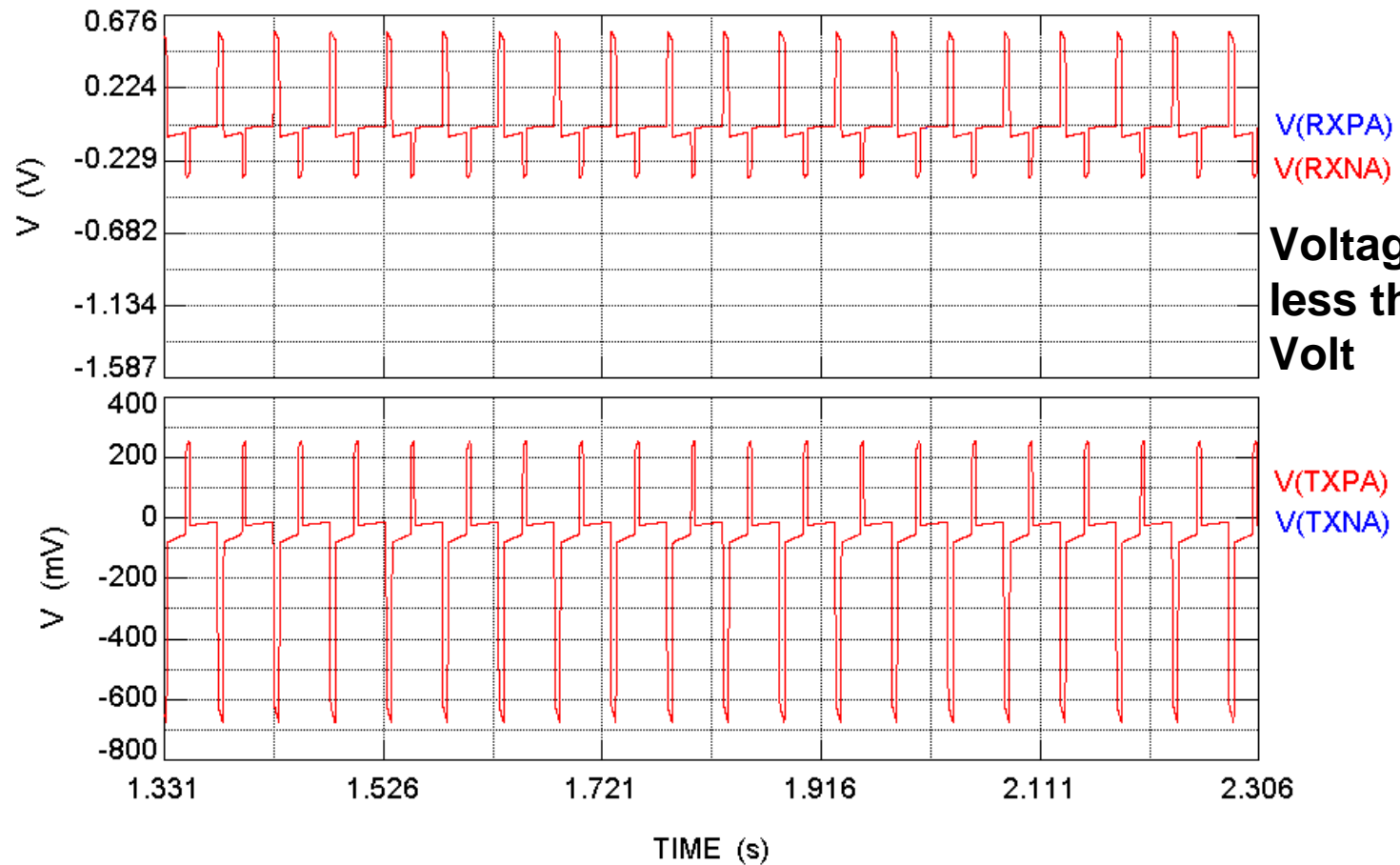
PSE – PSE Both High-Z Test Setup 1



PSE – PSE Setup 1 Test Results

TopVIEW - case3.OUT
File Edit Plot Traces Axis Format View Transform Cursors Tools Help

CASE 3 Both PSEs ARE DETECTING USING A 12V SWING.



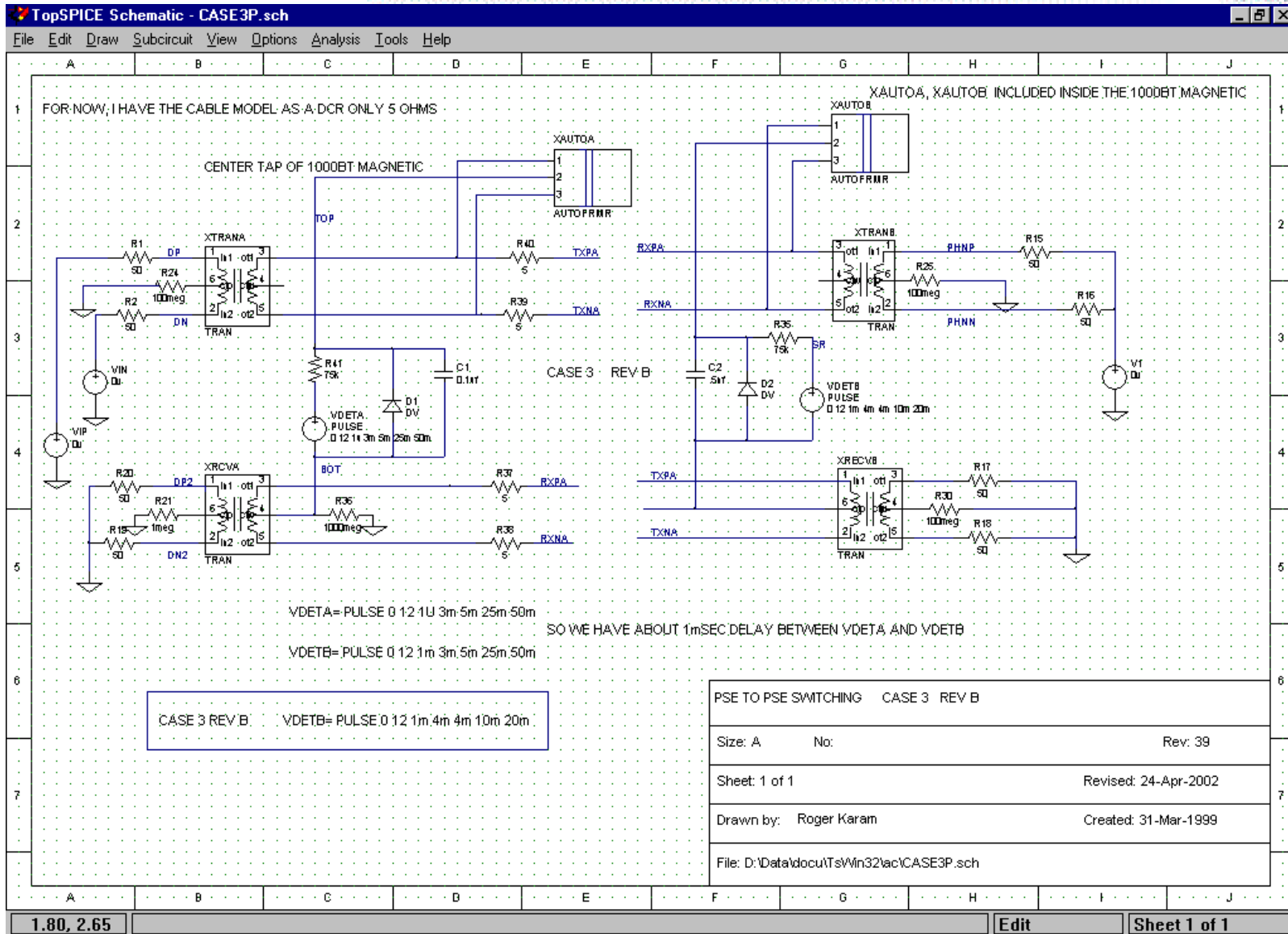
V(RXPA)
V(RXNA)

**Voltage is
less than 1
Volt**

V(TXPA)
V(TXNA)

Plot 1: — V(RXPA) — V(RXNA) Plot 2: — V(TXNA) — V(TXPA)

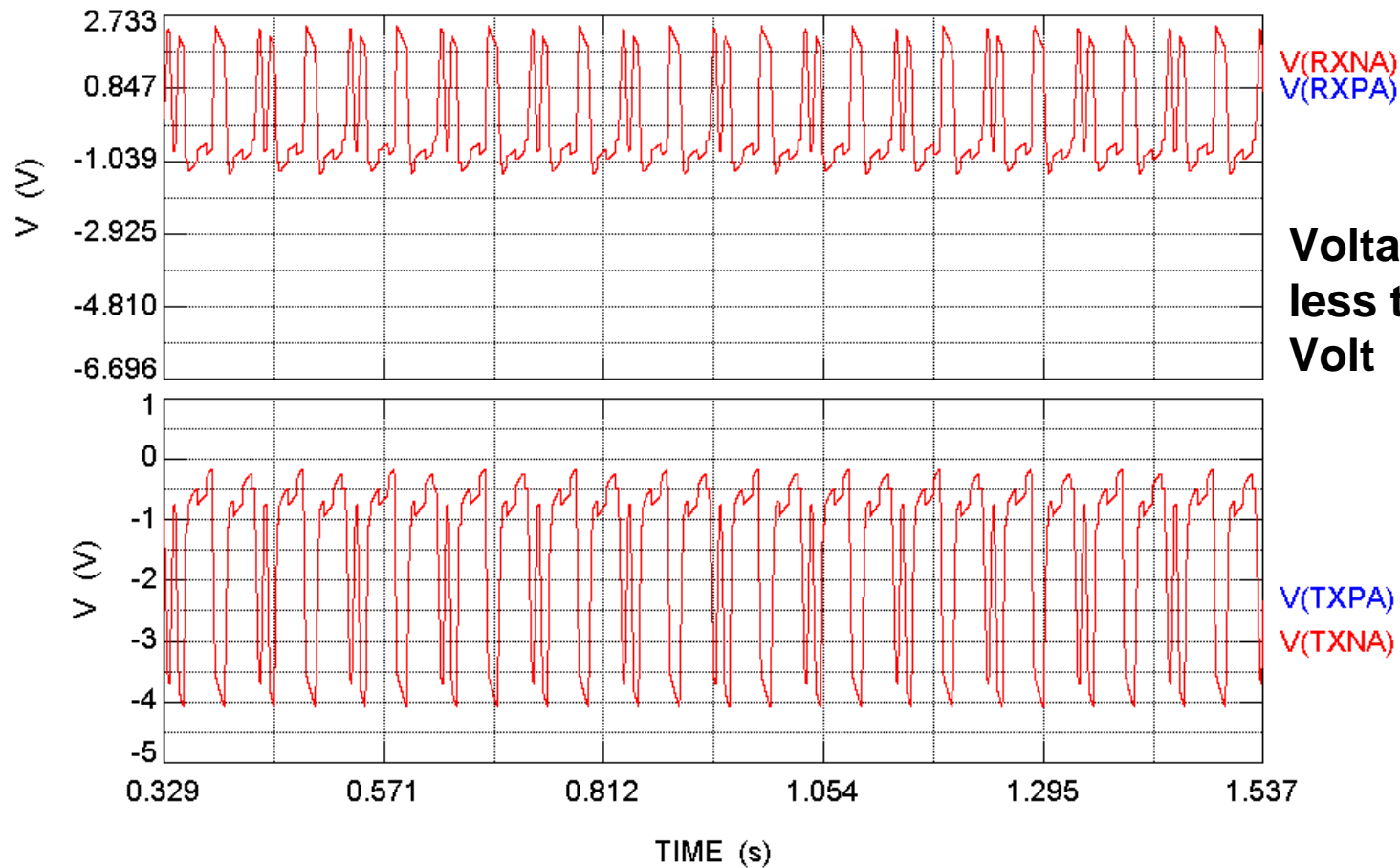
PSE – PSE Setup 2 (change signal- VDET B)



PSE – PSE Setup 2 Test Results

TopVIEW - CASE3.OUT
File Edit Plot Traces Axis Format View Transform Cursors Tools Help

CASE 3 REVB, NOTE THE CHANGE TO THE TR, TF- Duty Cycle & Freq
OF VDET B So It Does Matter What Each Side is doing after all !?



**Voltage is
less than 5
Volt**

Plot 1: — V(RXPA) — V(RXNA) Plot 2: — V(TXPA) — V(TXNA)

PSE – PSE SUMMARY...

- **Same Issue exists for AC Disconnect Signal**
- **Can this impact the data?**
- **Ethernet Interoperability – what do I test to?**
- **What happens on a bundle of cables as the DC is switched up to 30V**
- **The pair-to-pair DCR mismatch may be a factor in the 1 quadrant detection (up to 5 mA discovery current)**
- **AGAIN, we used reasonable rise-times in simulations (mSec)**

Daddy did you break Ethernet in Vegas?

PSE – PSE SUMMARY

- Do we need to be **“aggressive”** ?
- Recommend a **Conservative Approach**
- Don't shift to 2nd probe voltage until a trigger at 1st voltage has taken place - This ensures Ethernet 'feels' the same. Interoperability friendly
- Turn off AC signal when no power is applied

PSE-PSE AC Disconnection signal

Concern:

- Same issues as the AC switching of the DC detection signal.
- When no PD is connected a PSE sending the AC signal **may** interfere with PSE-PSE data transfer

Recommendation:

- Do not send AC signal when a PD is removed (or not powered)

Yes to v3.1 with recommendation

Classification Using Forced Current

Concerns

- Lab work shows that this has the potential to oscillate.
- Thus this can be an inter-operability nightmare.
- Some vendors claim this will add cost (to integrate this on a PD chip) ...

Recommendation:

- We have enough things to worry about
- Disallow Current Based Classification

Change Summary

- **Amplitude to 4.4V max.**
- **AC Signal rise-time slowed to mSec**
- **AC signal off when not powering**
- **DC detection should be, well, DC**
- **Specify a Min AC load**
- **Classification using forced-Current Removed**
- **Specify test PSE and PD, with test profile**

The risk is Ethernet interoperability

CISCO SYSTEMS

