

Diode Discovery Process Power Level Detection

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Agenda

- **Assumptions**
- **Power Levels required**
- **Power Level Detection method**
- **Circuit Definition**
- **Test Results**
- **Spice Simulations**
- **Components costs**
- **Benefits**
- **Conclusions**

Assumptions

- **Based on data from straw poles, motions and liaison letters that have been put to this Task Force, I have arrived at the following conclusions;**
 - **The minimum amount of power that should be delivered across an MDI Link is 8 Watts.**
 - **The maximum amount of power that either wire pairs 1+2 and 3+6 OR wire pairs 4+5 and 7+8 can carry is 14.6 Watts delivered to the PD end.**
 - **That power can be delivered on either sets of wire pairs but not both simultaneously. I would like to change this objective such that maximum flexibility and power delivery is Achieved.**

Power Levels Required

- **The selection of the actual power levels should be decided by the Task Force, however here are a few suggestions;**
 - **Option 1 (optimised for a single set wire pairs only)**
 - **Level 1 – delivers 8W (minimum load requirement)**
 - **Level 2 – delivers up to 10W**
 - **Level 3 – deliver up to 12W**
 - **Level 4 – delivers up to 14.6W (Maximum load)**
 - **Option 2 (optimised for both sets of wire pairs)**
 - **Level 1 – delivers 4W**
 - **Level 2 – delivers 8W**
 - **Level 3 – delivers 12W**
 - **Level 4 – delivers 14.6W**

Power Level Detection Method

- **The power detection method is integrated into the Diode Discovery Process.**
 - The primary stage of the Diode Discovery Process remains unchanged.
- **The secondary stage of the Diode Discovery Process is altered but only slightly.**
 - Reminder, the secondary stage of the process is designed to charge the capacitor in the PD. Thus appearing to make the Diode discovered in the primary stage disappear.
 - The basic principal of the modification to the second stage discovery is to vary the value of the capacitor between 1 of 4 fixed values.
 - The capacitor is still charged to make the Diode disappear but now we measure the time it takes to charge.

SIMPLE

Power Level Detection Method

- **Now a few details**

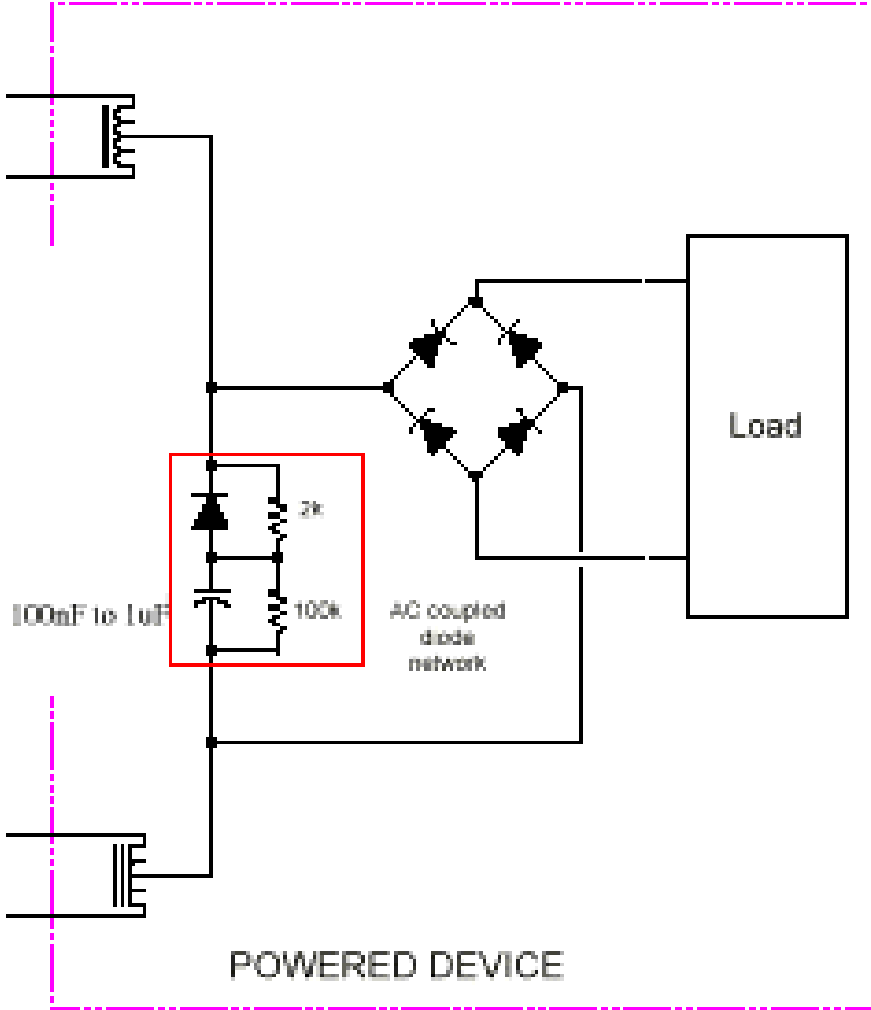
- **Capacitor values**

• Level 1	100n	+/- 20%	0-70°C
• Level 2	220n	+/- 20%	0-70°C
• Level 3	470n	+/- 20%	0-70°C
• Level 4	1u	+/- 20%	0-70°C

- **Duty Cycle for the second stage is fixed at 10u second pulse width and 40u second gap between pulses. There is still a train of 64 pulses in the second stage.**
- **Total time for the test remains as it is at present.**

Circuit Definition

DTE power over MDI



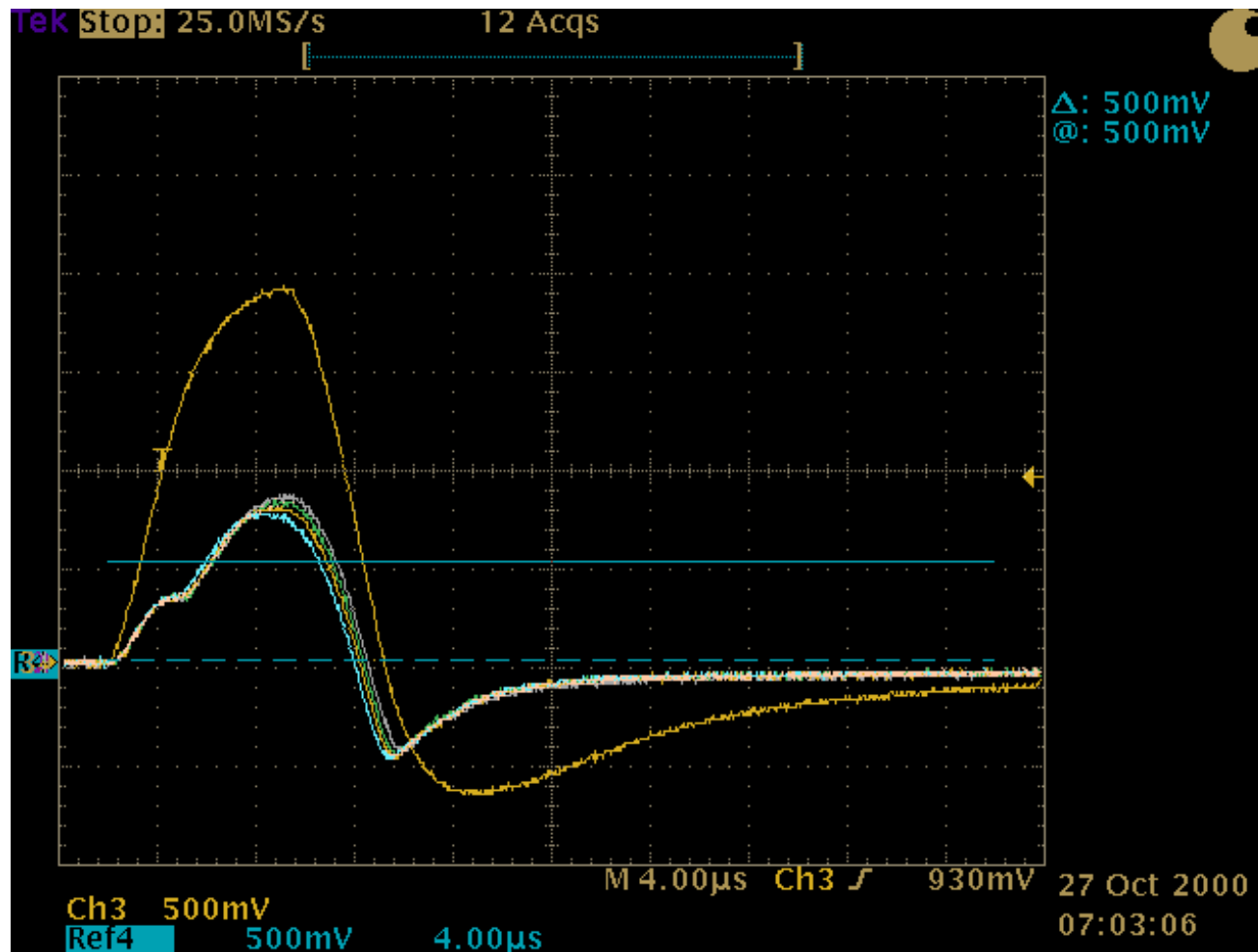
Test Results

- The following slides show the traces of the current Diode Discovery Process with the varying values of capacitance at the PD end.
- Also a BER test was performed on both a GOOD PHY and BAD PHY with all 4 values of capacitor in the load. **There was no change to the results previously presented.**
- In addition a test was carried out to verify that there was no degradation in the ability to detect correctly with each value of capacitance. **There was no degradation.** (200 consecutive correctly completed discovery cycles).

Test Results

Pulse Response @ 150m (Good PHY)

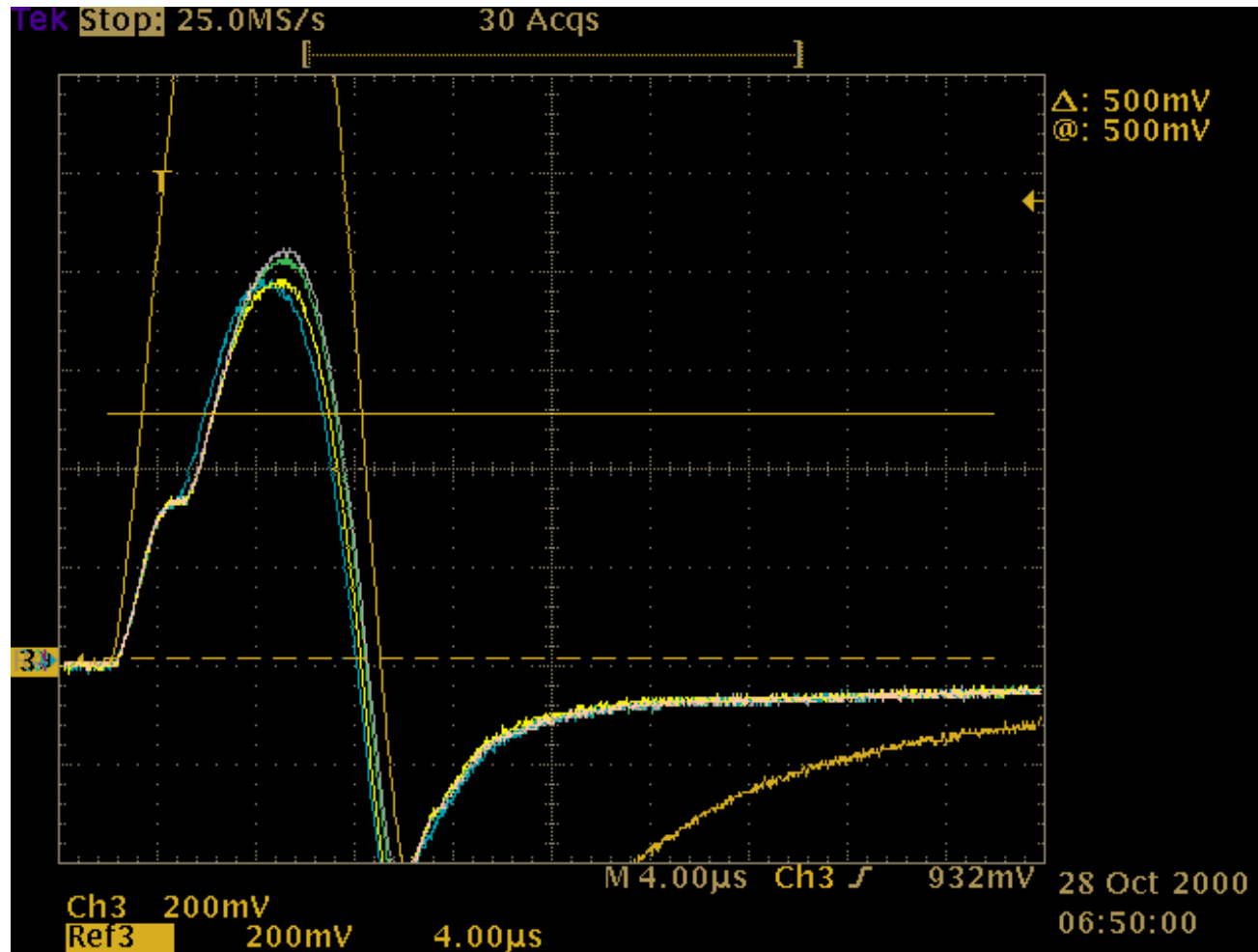
DTE power over MDI



Test Results

Pulse Response @ 150m (Zoom)

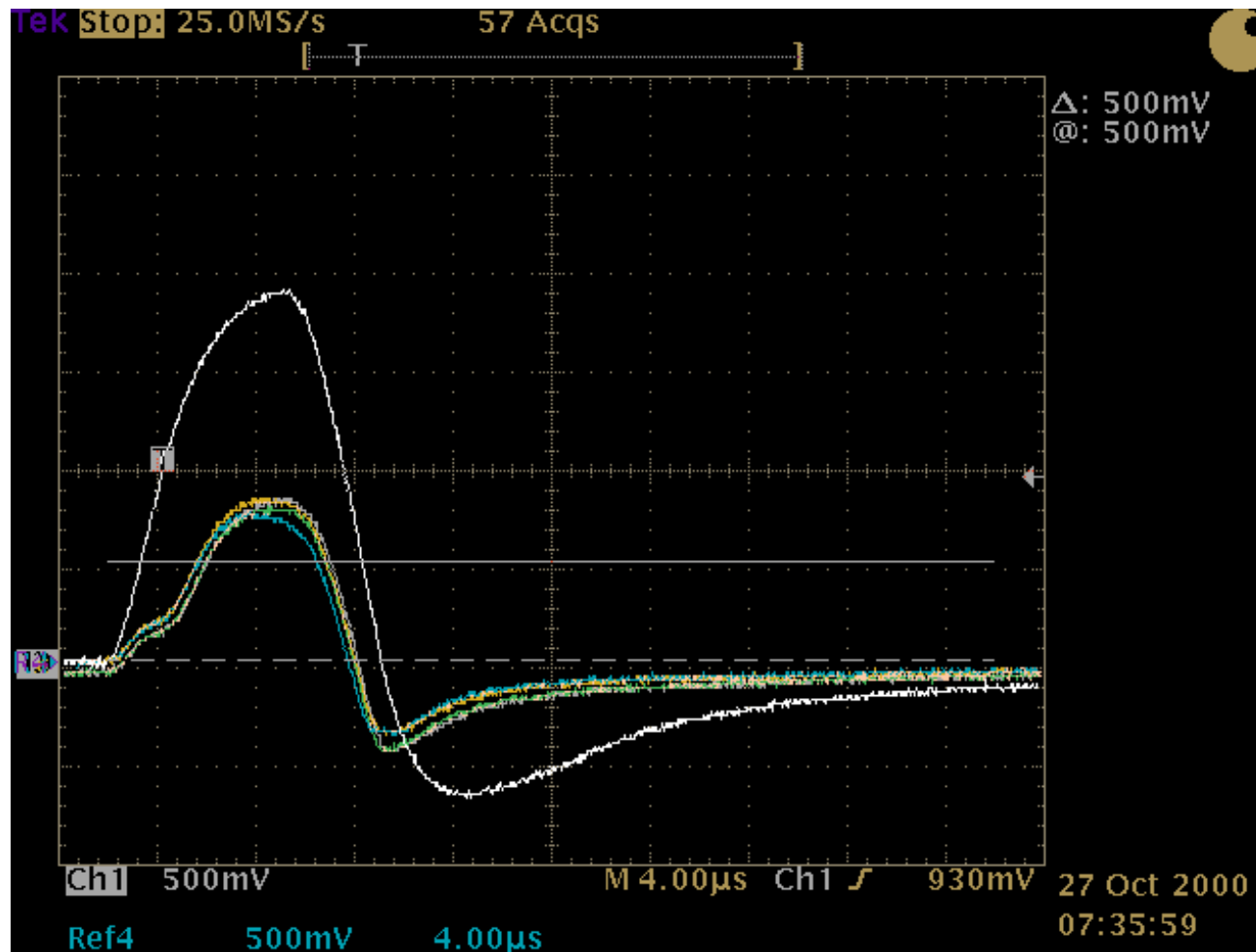
DTE power over MDI



Test Results

Pulse Response @ 93m (Bad PHY)

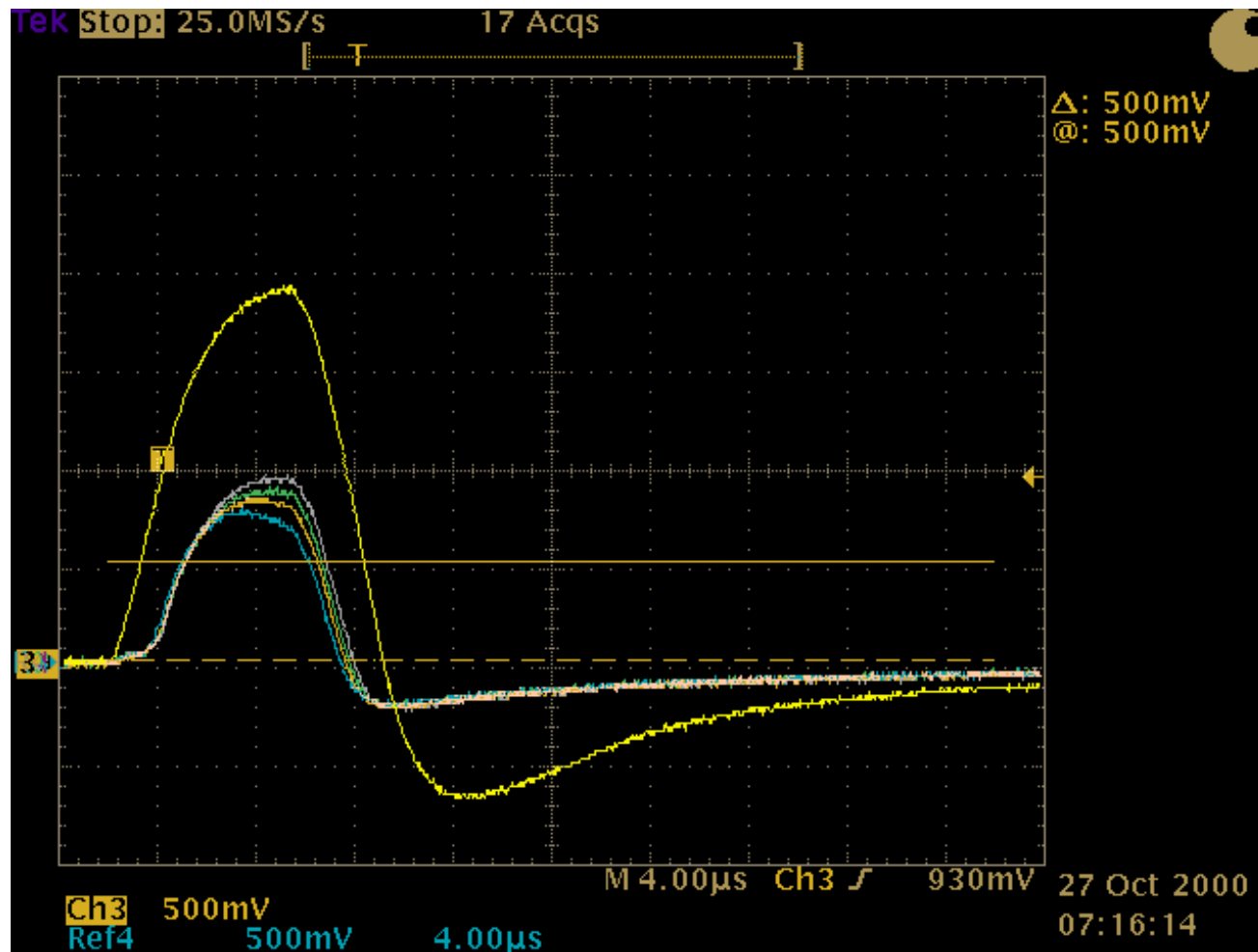
DTE power over MDI



Test Results

Pulse Response @ 5m (Bad PHY)

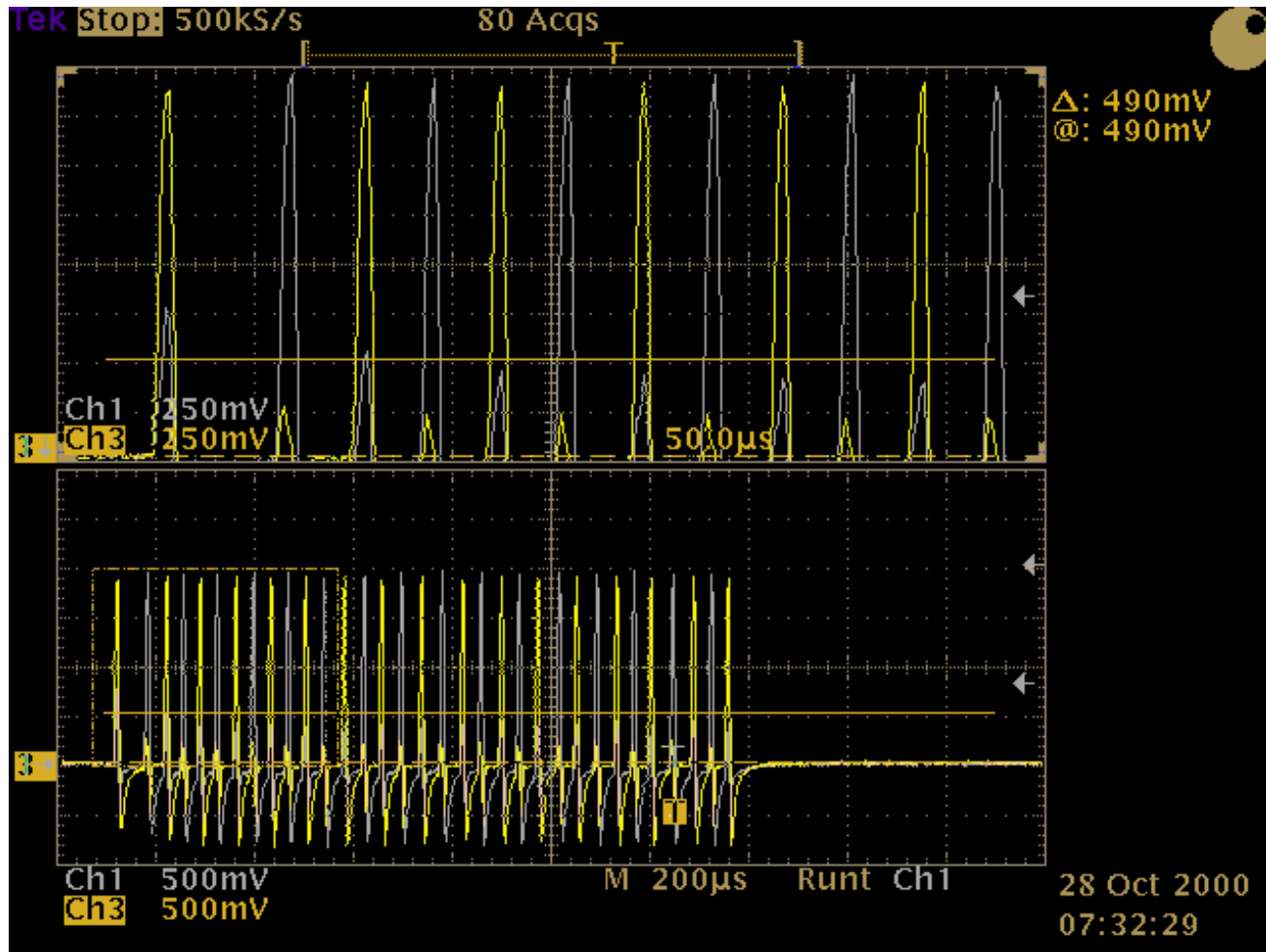
DTE power over MDI



Test Results

Second Stage Discovery 100nF Capacitor

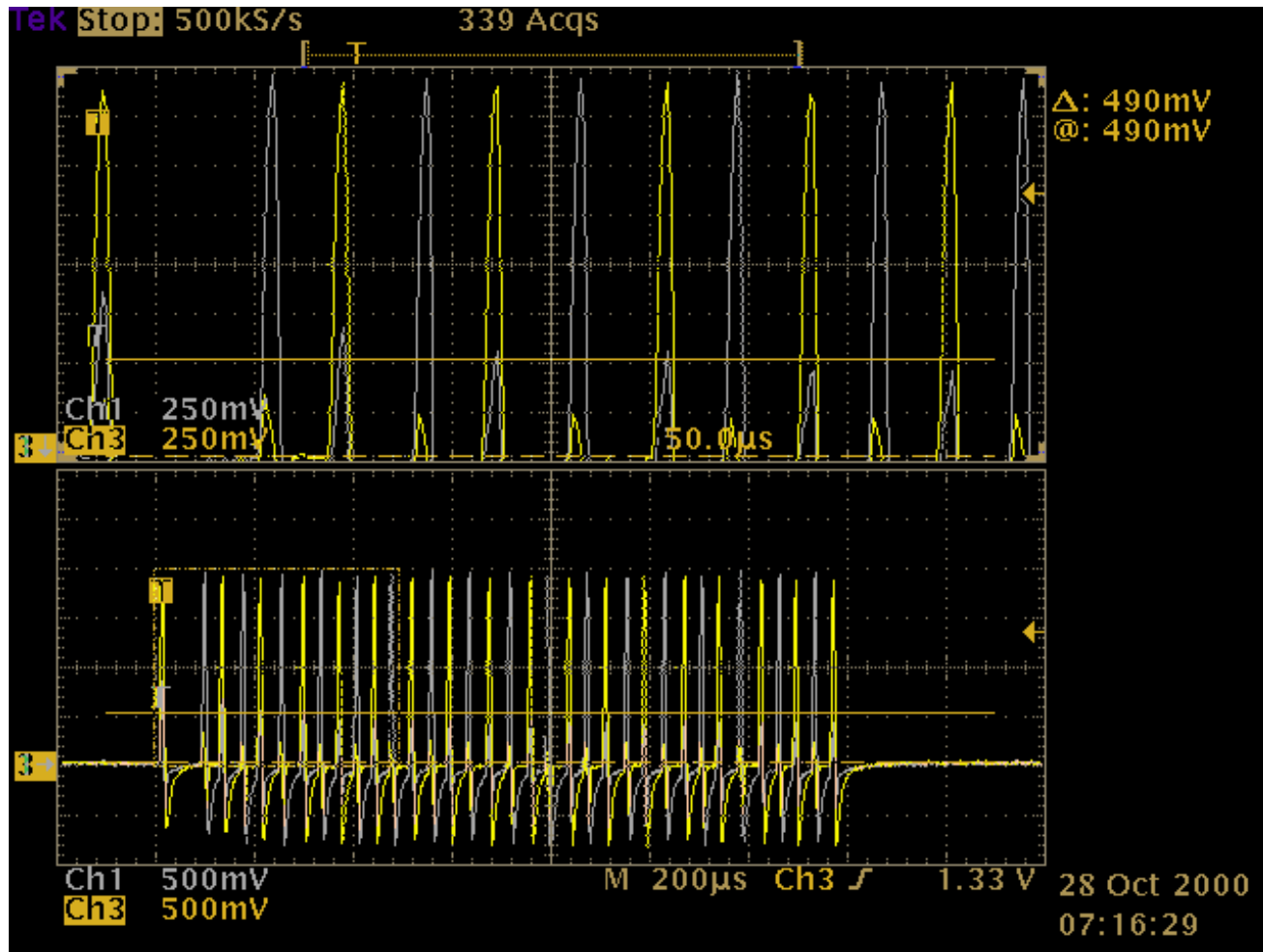
DTE power over MDI



Test Results

Second Stage Discovery 220nF Capacitor

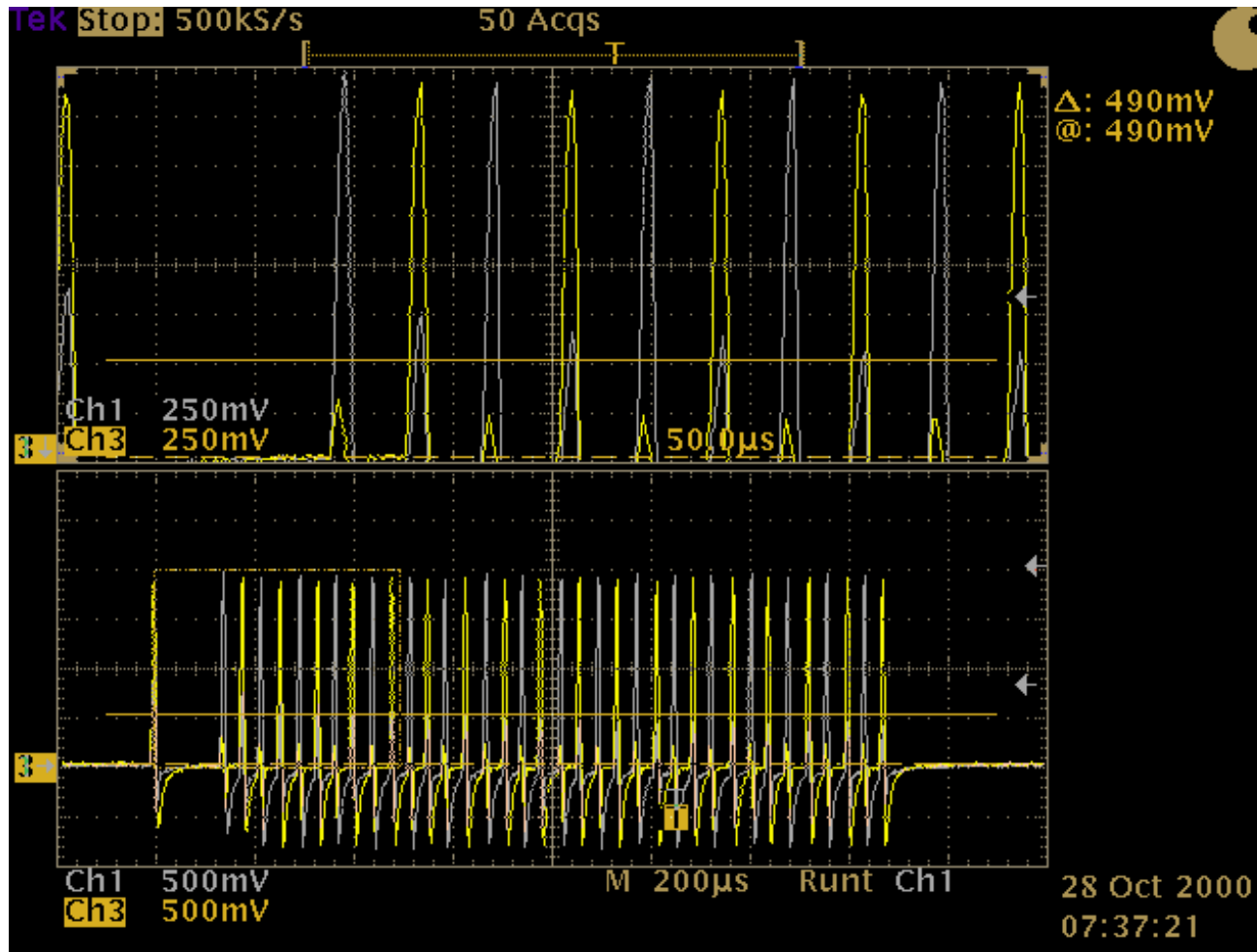
DTE power over MDI



Test Results

Second Stage Discovery 470nF Capacitor

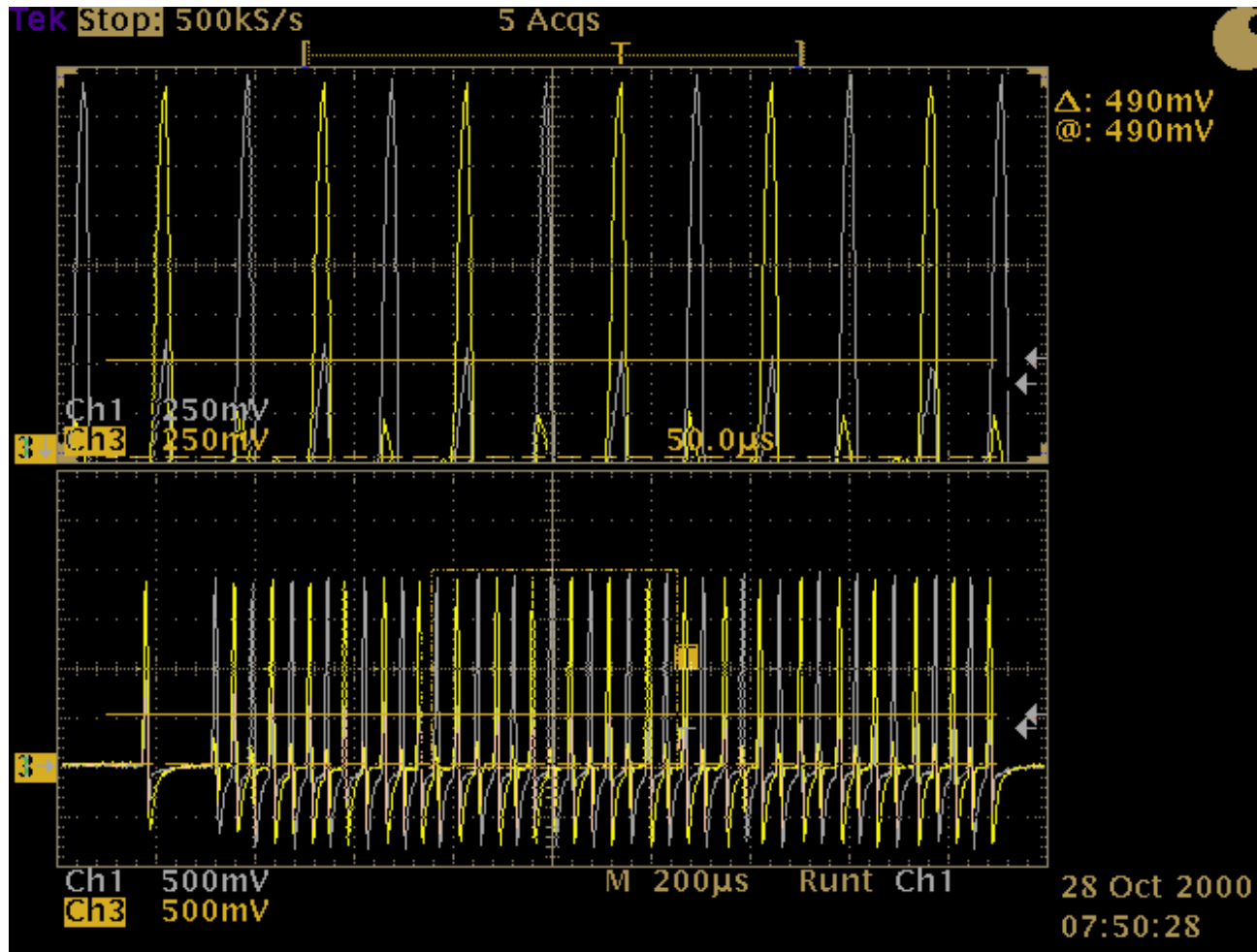
DTE power over MDI



Test Results

Second Stage Discovery 1uF Capacitor

DTE power over MDI



Test Results

Conclusions

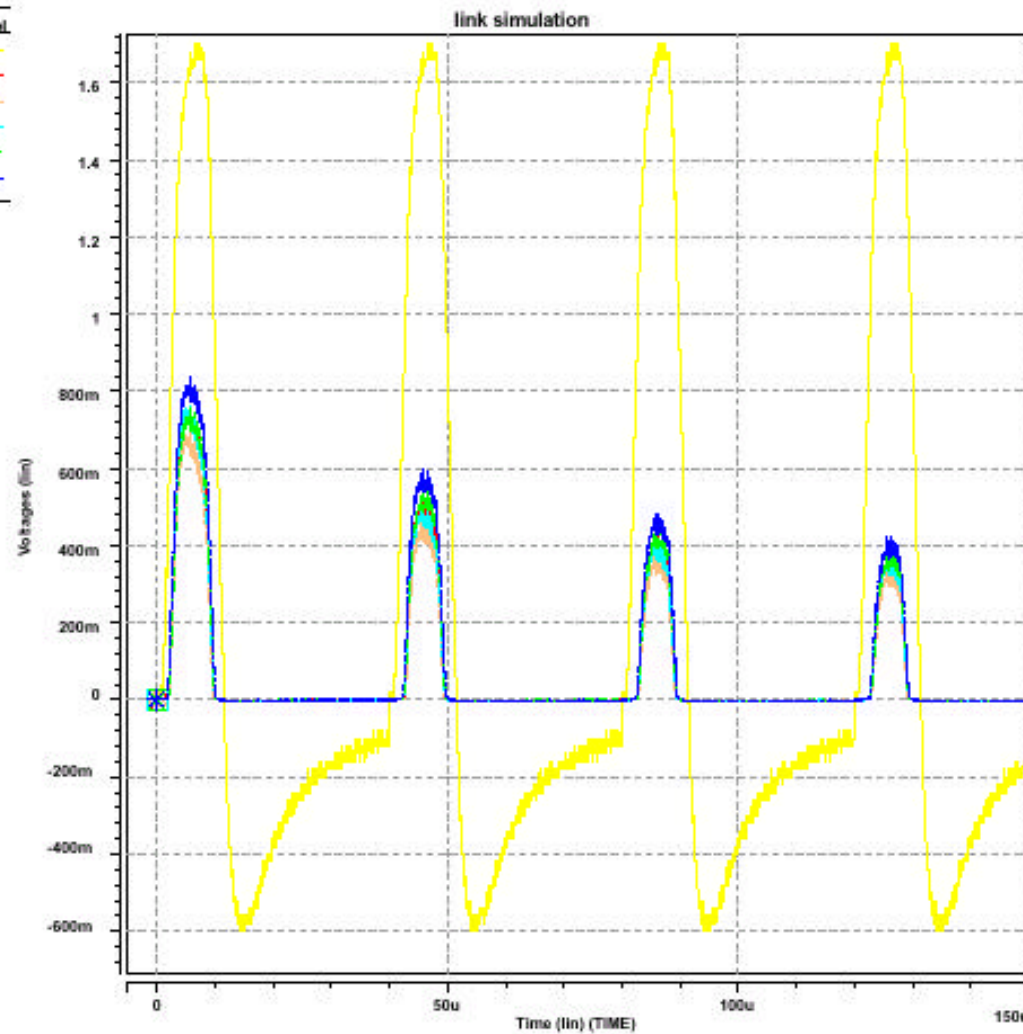
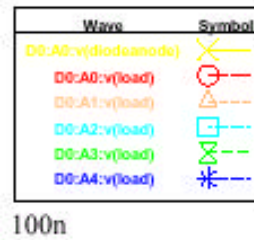
- **The traces show that there is still good margin in the standard mode of primary stage discovery to allow for changes in the values of the capacitor in the PD**
- **There is a clearly measurable time difference between the charging times of the various capacitor values in relation to the point that returned pulse crosses the 500mV detector level.**
- **This would allow us discover the power level required by a PD without any extra cost or complexity.**

Spice Simulations

- The Hspice simulations on the following four slides show for each value of capacitor the worst case tolerance and temperature behaviour of the pulse levels that can be expected.
- The combinations of tolerance and temperature are shown below;
 - Yellow Launch pulse
 - Red Return pulse, preferred value @ 25°C
 - Beige Return pulse, -20% value @ 0°C
 - L. Blue Return pulse, -20% value @ 70°C
 - Green Return pulse, +20% value @ 0°C
 - Blue Return pulse, +20% value @ 70°C

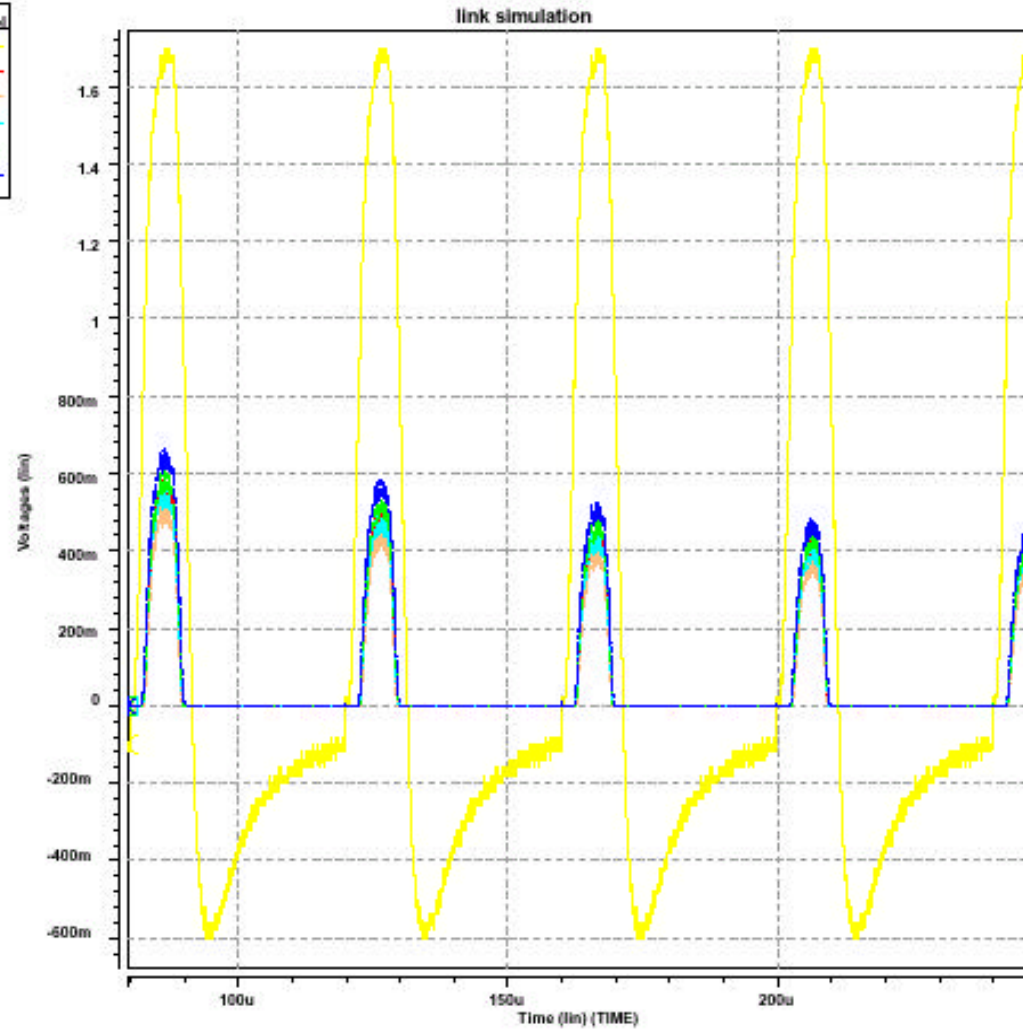
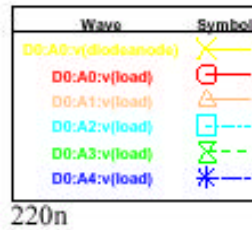
Spice Simulations

Tolerance and temperature of 100nF capacitor



Spice Simulations

Tolerance and temperature of 220nF capacitor

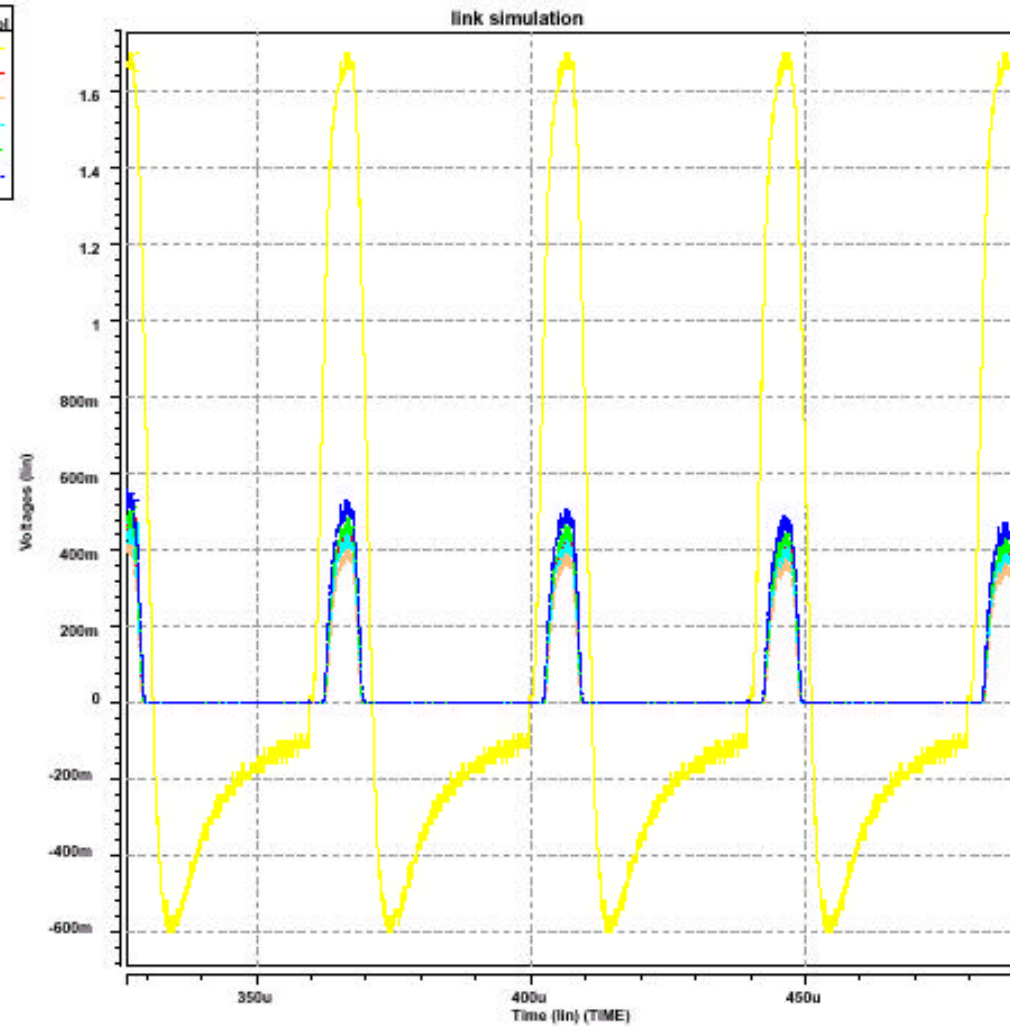


Spice Simulations

Tolerance and temperature of 470nF capacitor

Wave	Symbol
D0:A0:v(diodeanode)	X
D0:A0:v(load)	Q
D0:A1:v(load)	△
D0:A2:v(load)	□
D0:A3:v(load)	◇
D0:A4:v(load)	*

470n

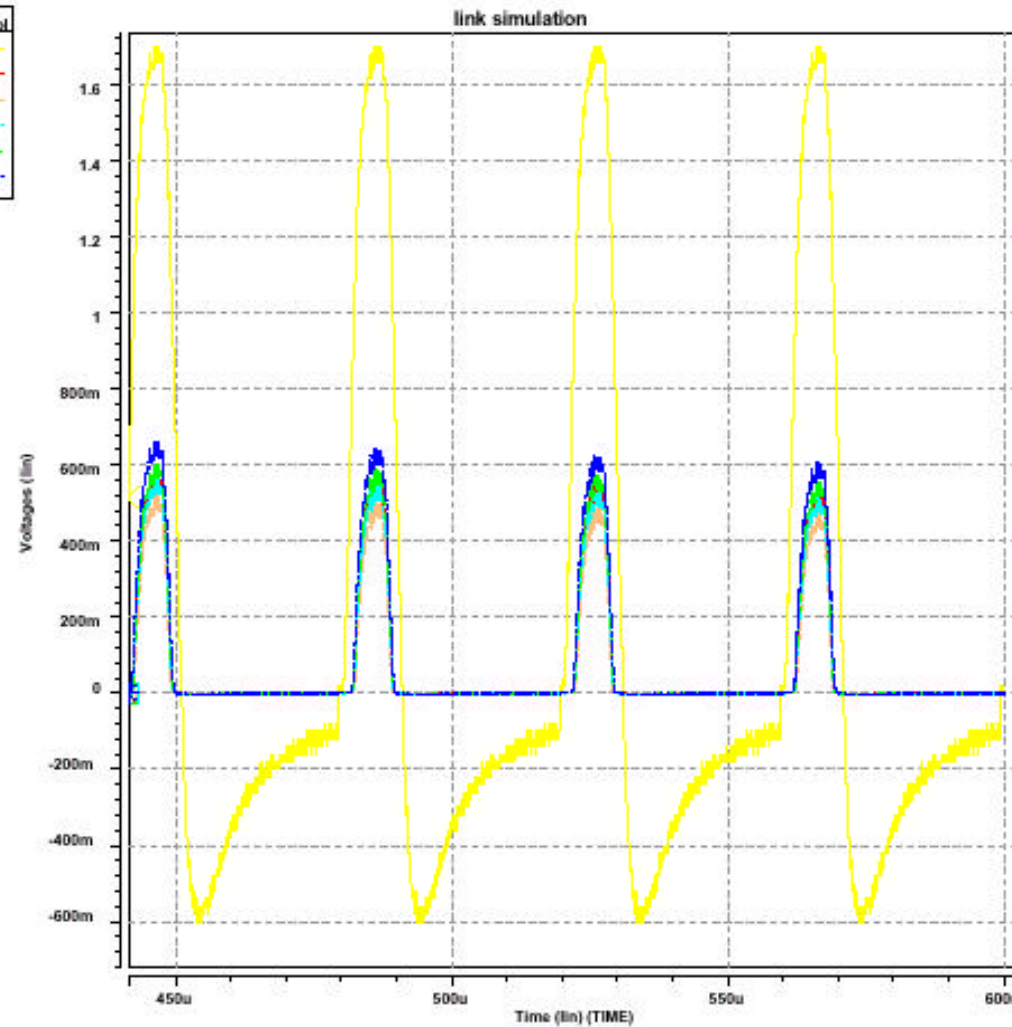


Spice Simulations

Tolerance and temperature of 1uF capacitor

Wave	Symbol
D0:A0:v(diodeanode)	X
D0:A0:v(load)	○
D0:A1:v(load)	△
D0:A2:v(load)	□
D0:A3:v(load)	◇
D0:A4:v(load)	*

1u



Spice Simulations

Conclusions

- **The previous slides show that even taking into account tolerance and temperature;**
- **There is ample headroom to maintain the primary discovery method robustly.**
- **There is a clearly measurable time difference between the charging times of the various capacitor values in relation to the point that returned pulse crosses the 500mV detector level.**

Component Costs

- Based on the data shown at the last meeting it is clear that there is little or no difference in cost for the PSE. This cost is dominated by the cost of the power supply.
- On the PD equipment it also appears that there is very little difference in cost. However at the last meeting the cost for the Diode Discovery scheme was shown in terms of a ratio. It is shown below in real component cost;

Component Description	Qty	Cost (\$)
Diode 1N4148	1	0.008
Resistor, 100k	1	0.00047
Resistor, 2k	1	0.00047
Capacitor, 100nF-1uF	1	0.03 – 0.08
Diode 1N4003	4	0.0078
Total for 100nF implementation		0.04774
Total for 1uF implementation		0.09774

- Component costs are based on 100,000 qty piece part price.

Benefits

- **PD cost is very low between 5 and 10 cents for a single channel. (Two channels for 10 to 20 cents)**
- **Primary detection method is unchanged, therefore all previous results presented on the performance and robustness of the discovery process remain valid.**
- **Allows the ability to detect different power levels on each wire pairs set and deliver the most flexible power requirement to a single PD (from 4 to 29.2W)**
- **Maintains the original SIMPLE detection component, a comparator. (Lucent scheme currently needs an ADC and would require it to do level detection based on varying resistor values).**
- **Robust across component tolerances and temperature**

Conclusions

- **Power Level Detection can be incorporated in to the existing Diode Discovery Process with -**
- **No added cost – PD cost reduces slightly**
- **No degradation to robustness of discovery**
- **Maximum flexibility of power delivery**
- **Operates on either wire pair set or both with no degradation to the MDI link data transfer capability**
- **No degradation to EMI or cross talk performance**