

Diode Discovery Process Signal Pair Test Results

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**Acknowledgments:
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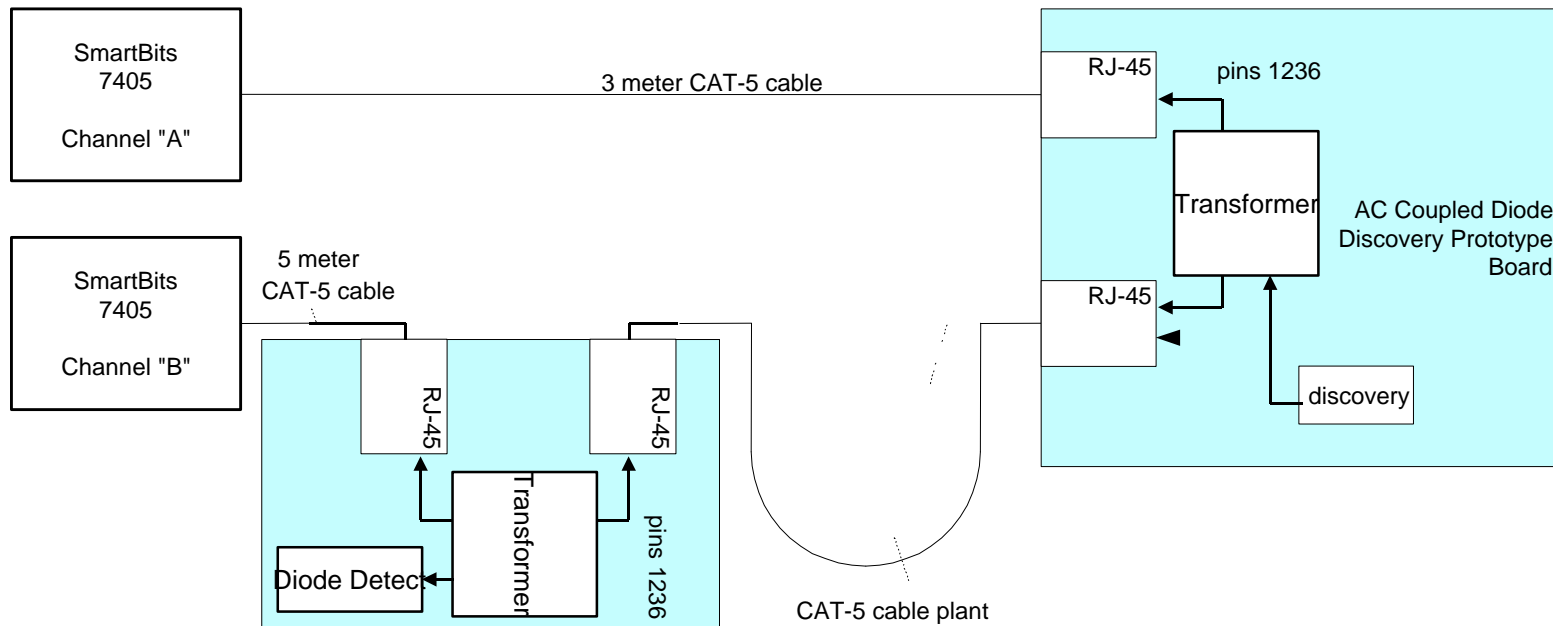
Agenda

- **Test Method and Device Selection**
- **Operational Effects - BER**
- **Signal Integrity - 100M**
- **Signal Integrity – 10M**
- **Conclusions**

Test Method and Device Selection

- **In order to set a base line for all of the tests to be comparative, BER testing against line length was used.**
 - **8 Different PHY devices were tested. Each was run to the longest line length possible for error free operation.**
 - **The best performing (Good PHY) and the worst performing (Bad PHY) devices were chosen. This is hoped to set the bounds of the majority of PHY products deployed in the field.**
 - **These two PHY devices were used in the testing that follows.**
 - **The schematic for the test bench is shown on the next slide.**

Test Method and Device Selection



- **The block diagram above shows the test set up used for this testing.**
 - The 3,5 meter patch cables are included to ensure a realistic cable structure and maximize the impedance mis-match usually associated with these patch cords.
 - The CAT-5 cable plant was varied in length during these tests. This cable is made up of various numbers of 25m, 10m and 1m cables connected together with RJ-45 MM couplers. This cable plant includes more sources of impairment than the specified worst case.

Operational Effects

- **BER Effects**
 - PHY Devices were tested against line length to indicate degradation in performance.
 - The line length was noted at each point when the PHY became error free again. Each PHY was tested under the following conditions;
 - No Power, No Discovery
 - No Power, Discovery running continuously
 - Power On, Discovery On, No Load
 - Power On, Discovery On, 100mA Load
 - Power On, Discovery On, 300mA Load
- The results are shown in the following slides.

Operational Effects

Good PHY

- **No Power, No Discovery**
 - Error free operation was achieved at a line length of 155m
- **No Power, Discovery running continuously**
 - Error free operation was achieved at a line length of 155m
- **Power On, Discovery On, No Load**
 - Error free operation was achieved at a line length of 136m
- **Power On, Discovery On, 100mA Load**
 - Error free operation was achieved at a line length of 151m
- **Power On, Discovery On, 300mA Load**
 - Error free operation was achieved at a line length of 150m

Operational Effects

Bad PHY

- **No Power, No Discovery**
 - Error free operation was achieved at a line length of 94m
- **No Power, Discovery running continuously**
 - Error free operation was achieved at a line length of 94m
- **Power On, Discovery On, No Load**
 - Error free operation was achieved at a line length of 90m
- **Power On, Discovery On, 100mA Load**
 - Error free operation was achieved at a line length of 93m
- **Power On, Discovery On, 300mA Load**
 - Error free operation was achieved at a line length of 93m

Operational Effects

Conclusions

- **These results demonstrate that the Discovery detection process has no effect on the performance of the PHY device and as such does not degrade the existing MDI link.**
- **It can also be clearly seen that the power supply will degrade the MDI link.**
- **This is especially true in a failure mode as shown in “Power On, Discovery On, No Load” test case where the power supply is allowed to cycle on and off continuously.**

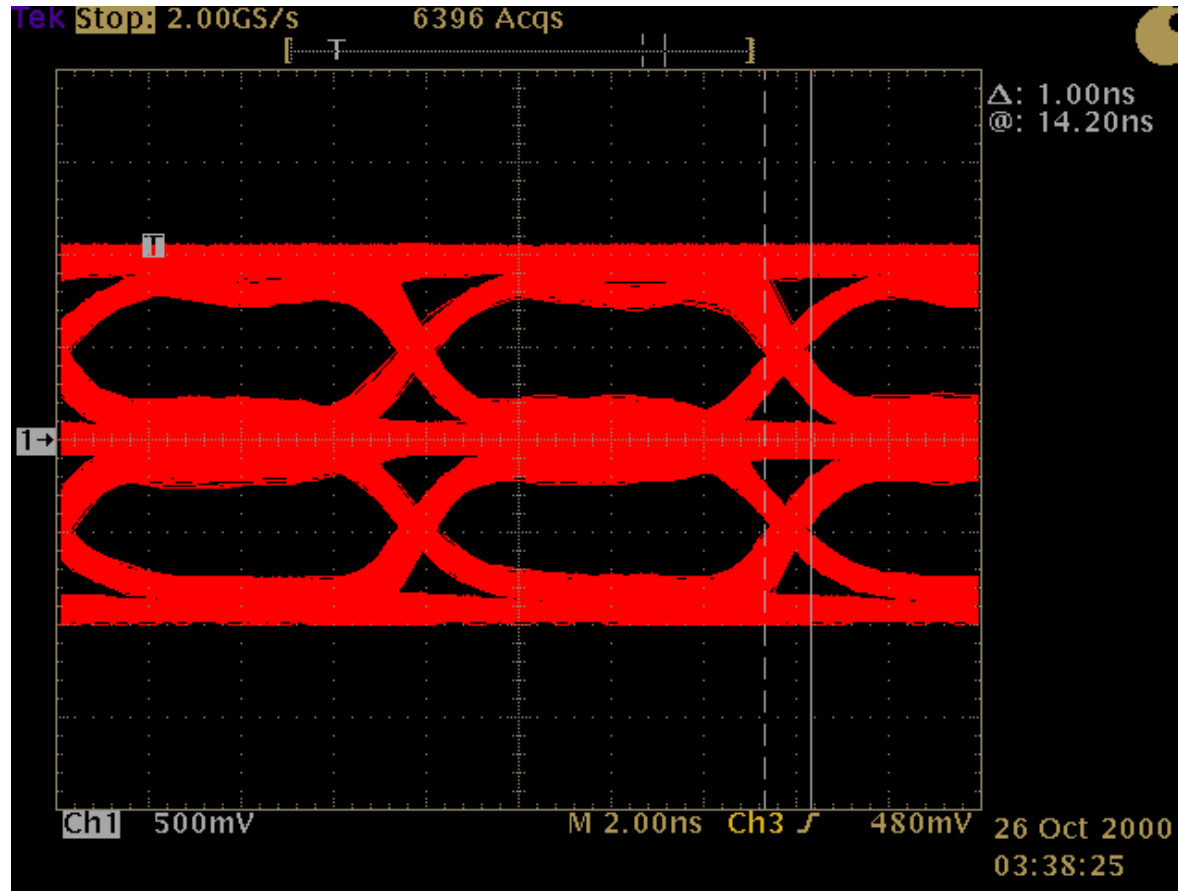
Signal Integrity - 100M

- **Each PHY device had the following signal integrity tests carried out;**
 - Differential Signal 0-Pk
 - Rise/Fall Time
 - Transmit Jitter
 - Amplitude Symmetry
 - Duty Cycle Distortion
 - Overshoot
- **These tests were carried out under the following conditions**
 - No Power, No Discovery
 - No Power, Discovery running continuously
 - Power On, Discovery On, 300mA Load

Signal Integrity - 100M

Good PHY

DTE power over MDI

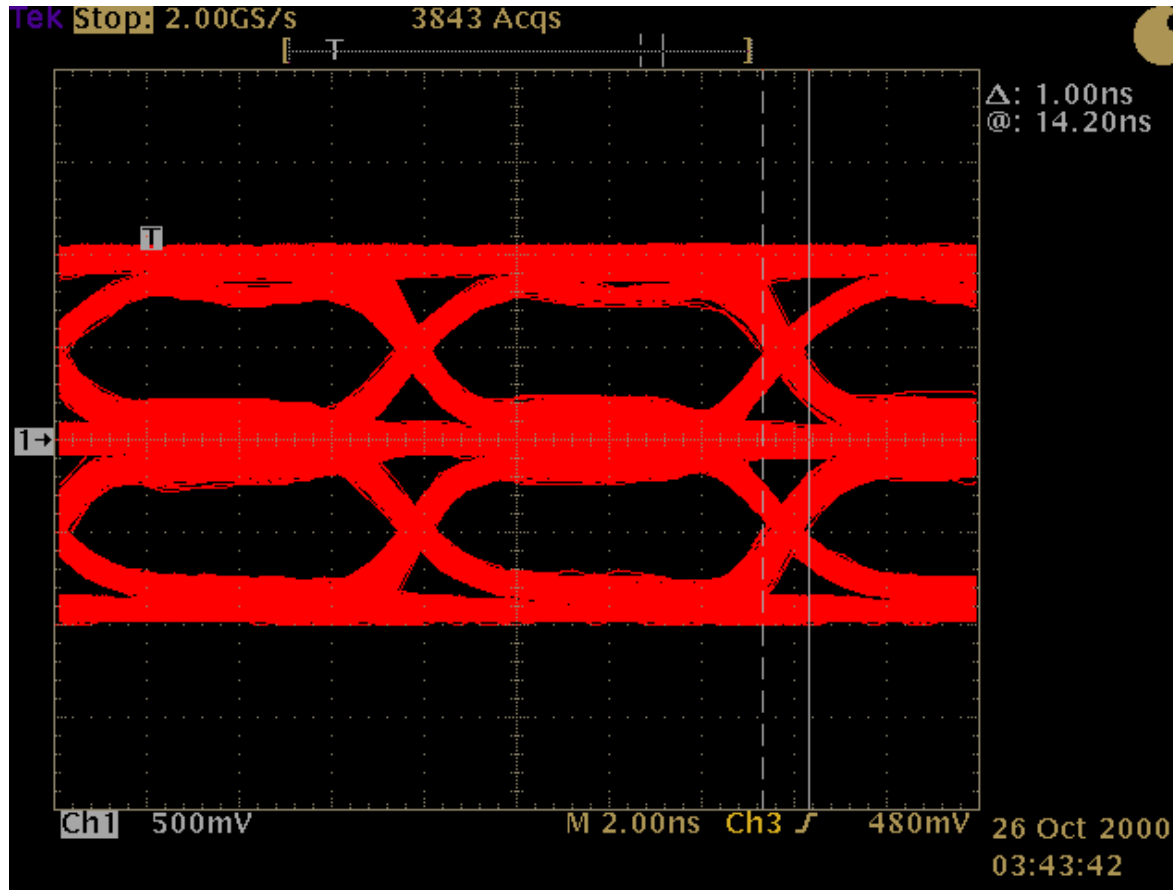


Tx Eye and Jitter, No Discovery, No Power

Signal Integrity - 100M

Good PHY

DTE power over MDI

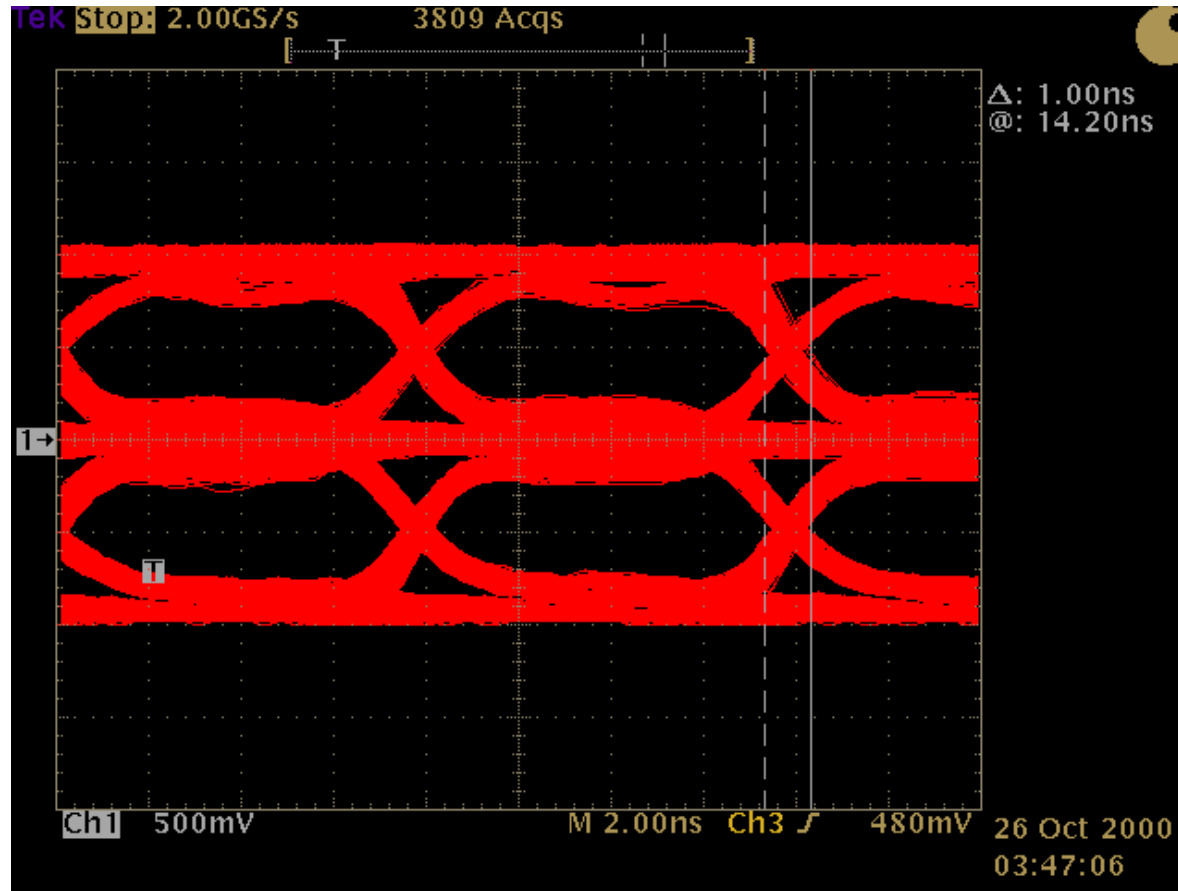


Tx Eye and Jitter, No Power, Discovery On

Signal Integrity - 100M

Good PHY

DTE power over MDI

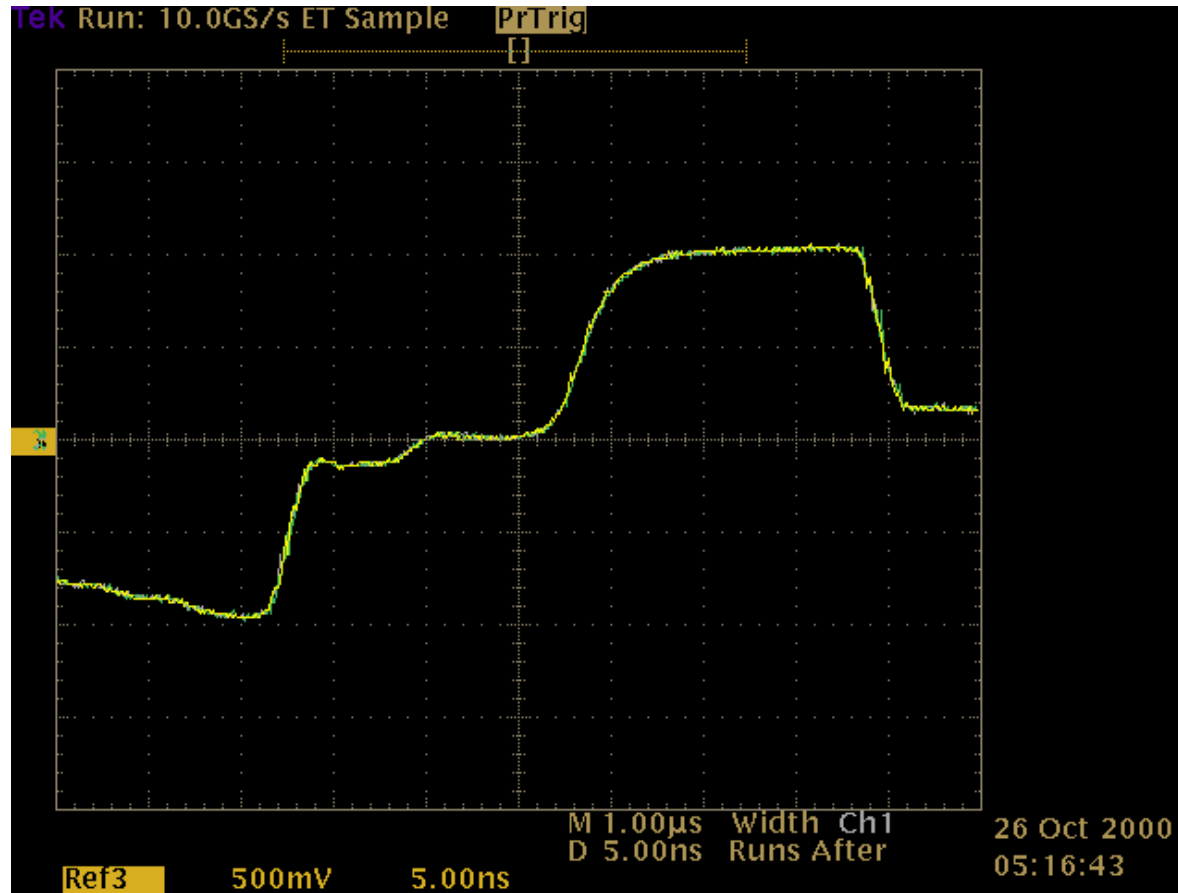


Tx Eye and Jitter, Power On, Discovery On, I = 300mA

Signal Integrity - 100M

Good PHY

DTE power over MDI

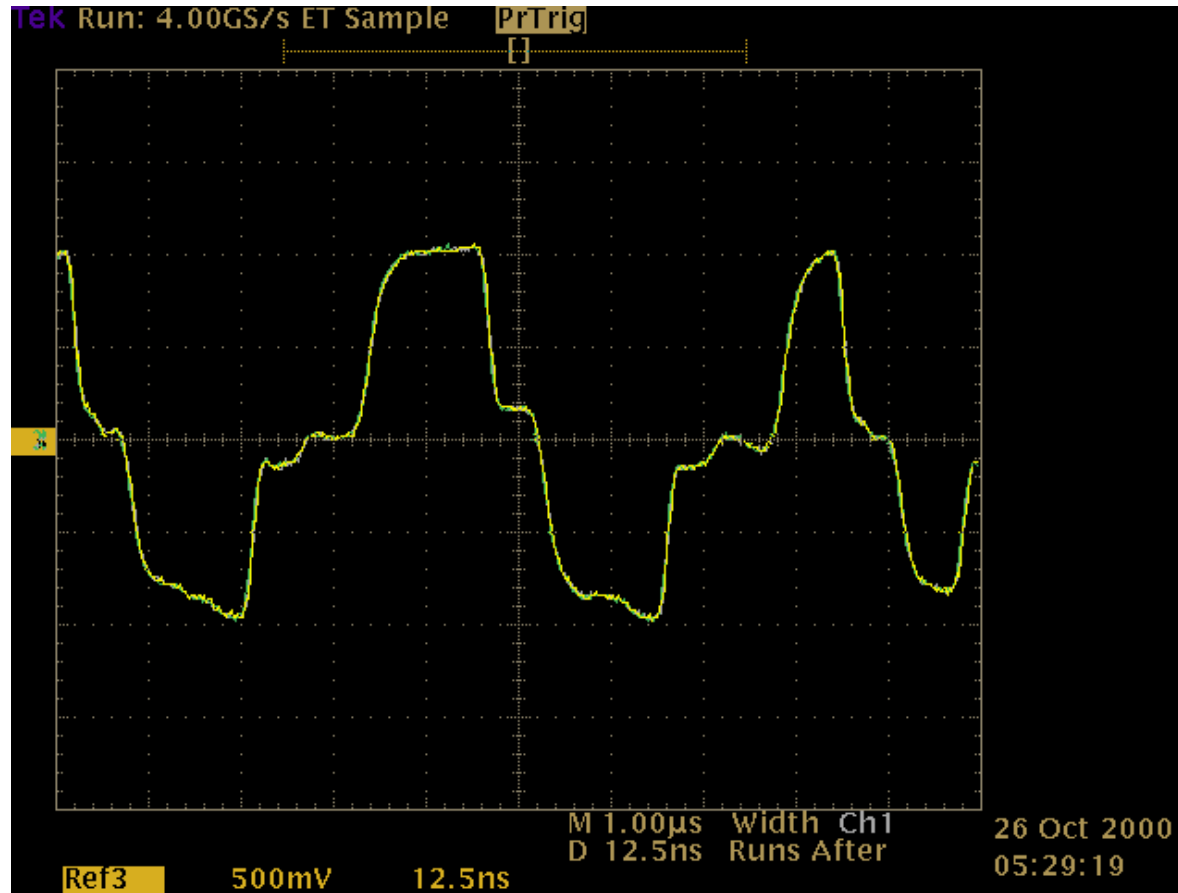


Tx Overshoot, All three conditions

Signal Integrity - 100M

Good PHY

DTE power over MDI

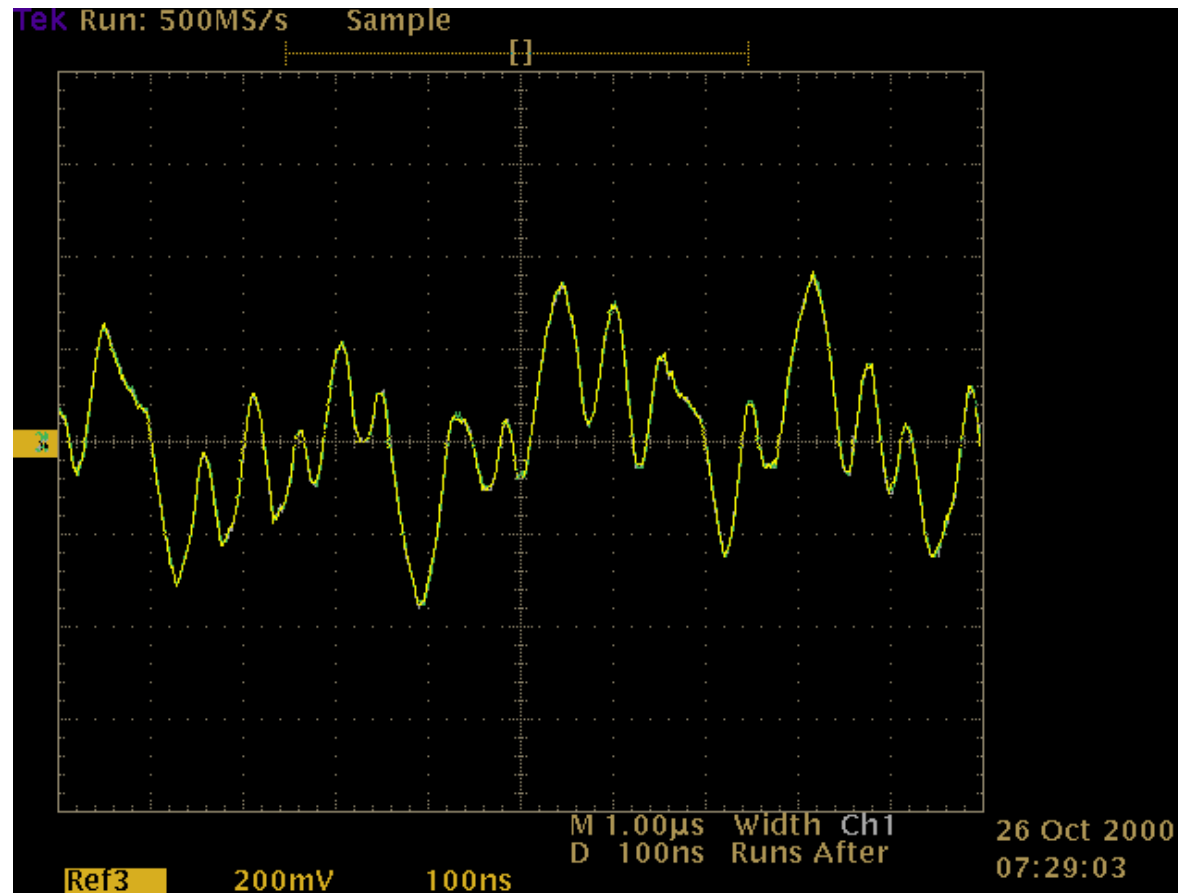


Tx Duty Cycle Distortion, All three conditions

Signal Integrity - 100M

Good PHY

DTE power over MDI



Rx Waveform at 150m

Signal Integrity - 100M

Good PHY – Results Summary

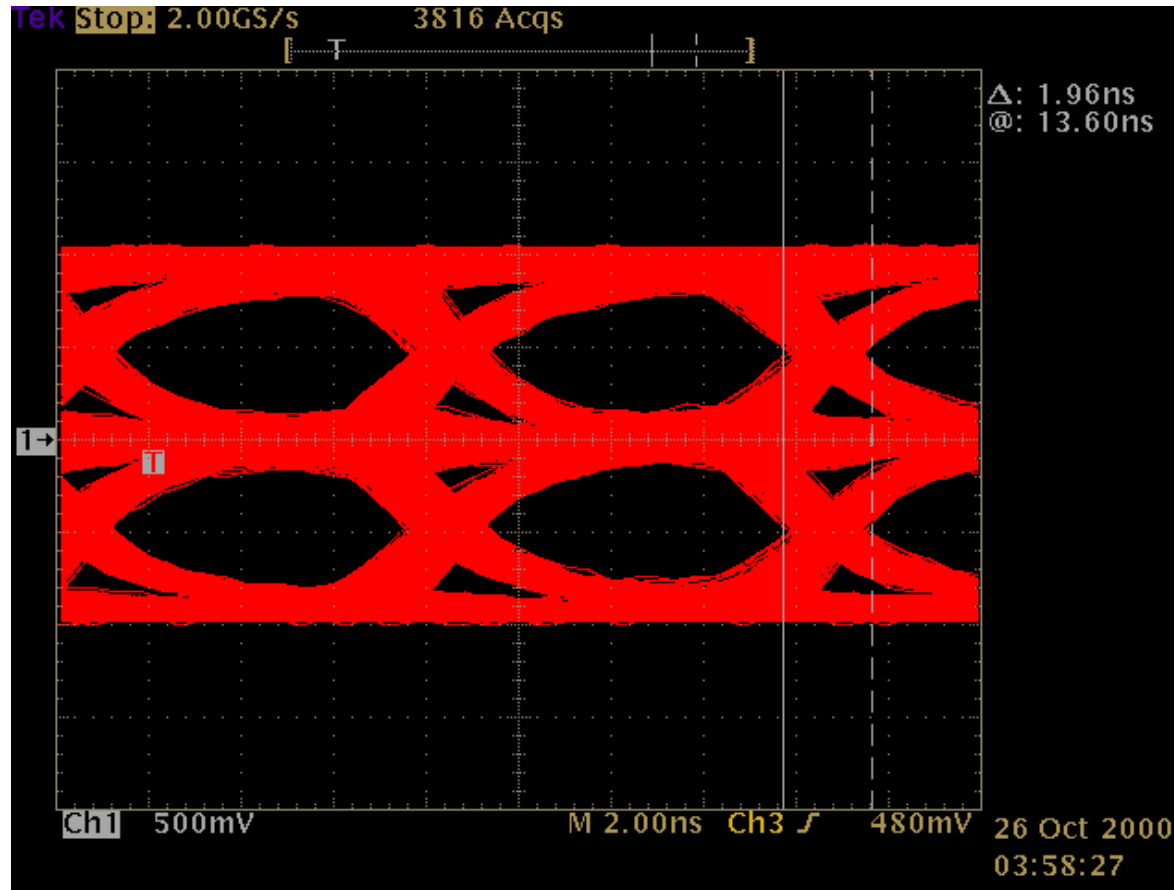
DTE power over MDI

Characteristic	Normal	Discovery	Power
Differential Signal			
Positive Peak	1.04V	1.04V	1.04V
Negative Peak	0.99V	0.99V	0.99V
Rise/Fall Time	3.6/3.2ns	3.6/3.2ns	3.6/3.2ns
Duty Cycle Distortion			
Positive Width	24.0ns	24.0ns	24.0ns
Negative Width	24.2ns	24.2ns	24.2ns
Transmit Jitter	1000ps	1000ps	1000ps

Signal Integrity - 100M

Bad PHY

DTE power over MDI

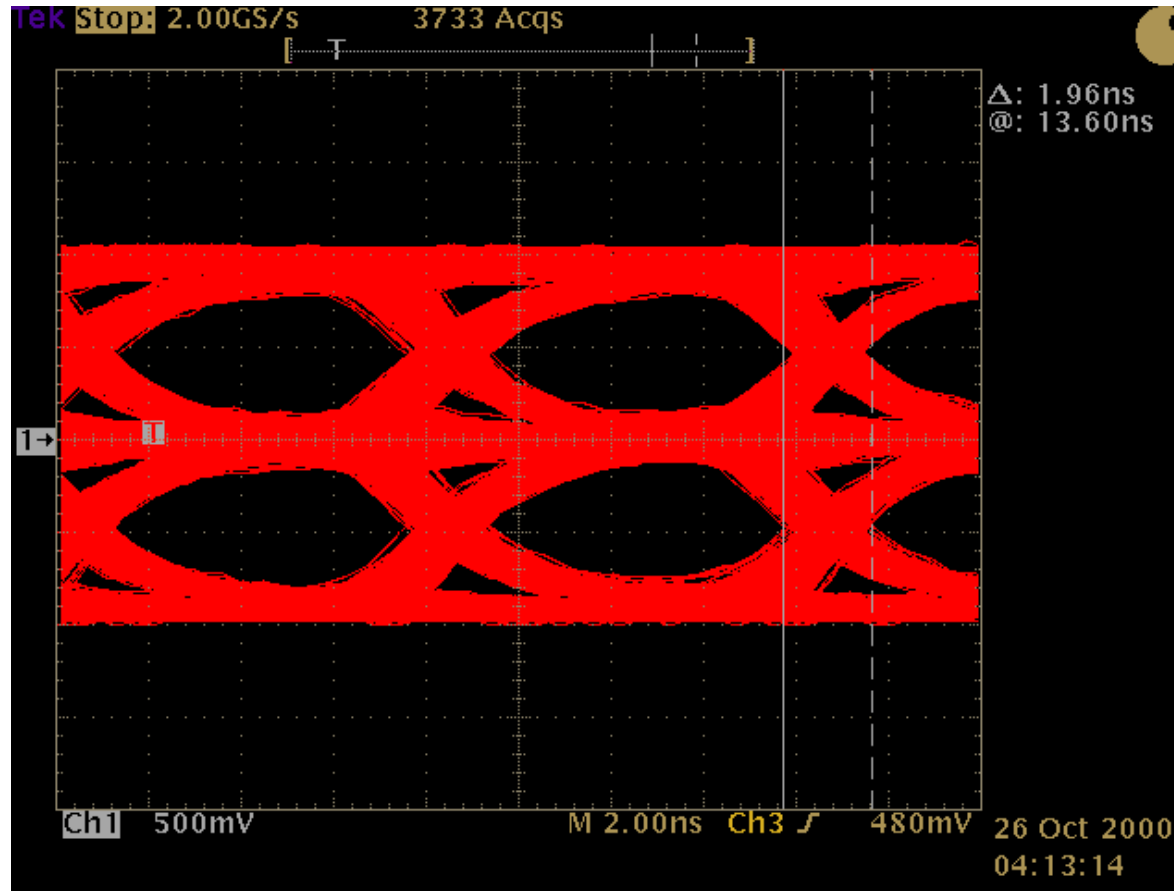


Tx Eye and Jitter, No Discovery, No Power

Signal Integrity - 100M

Bad PHY

DTE power over MDI

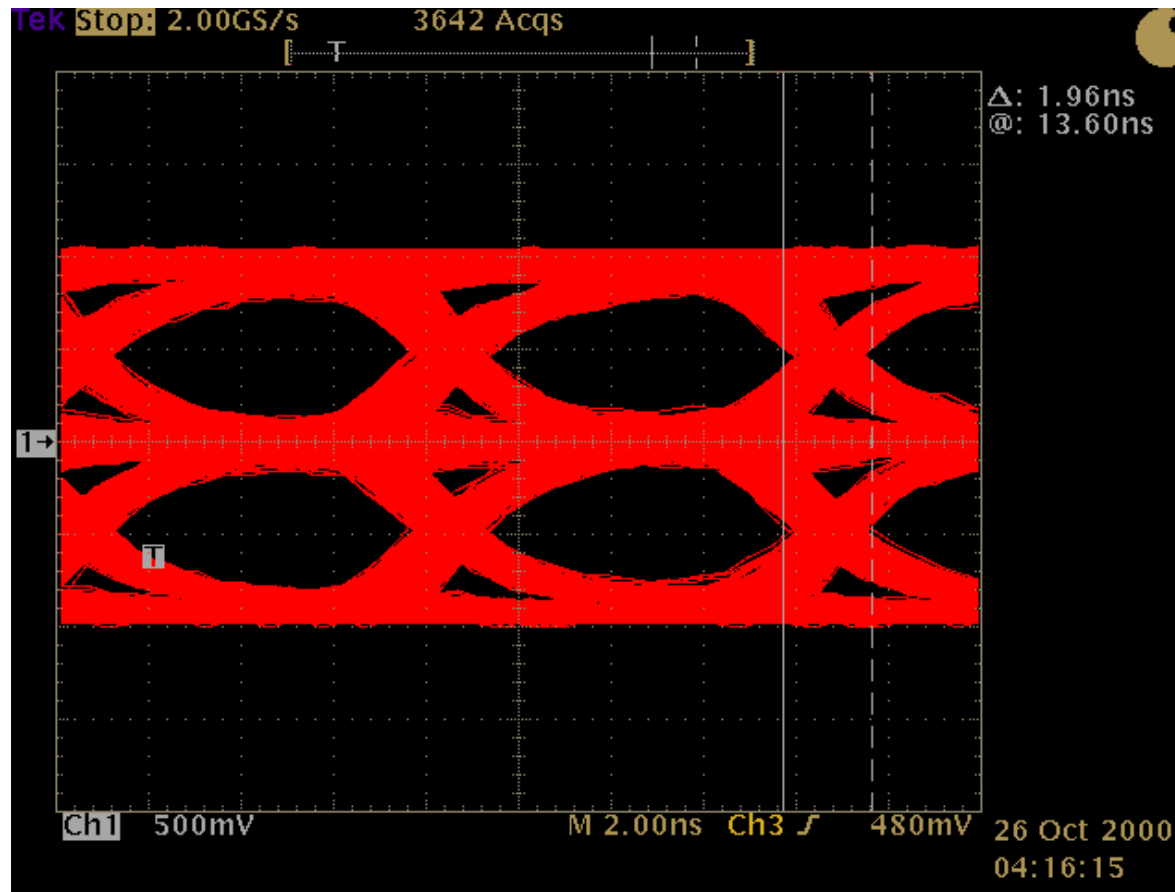


Tx Eye and Jitter, No Power, Discovery On

Signal Integrity - 100M

Bad PHY

DTE power over MDI

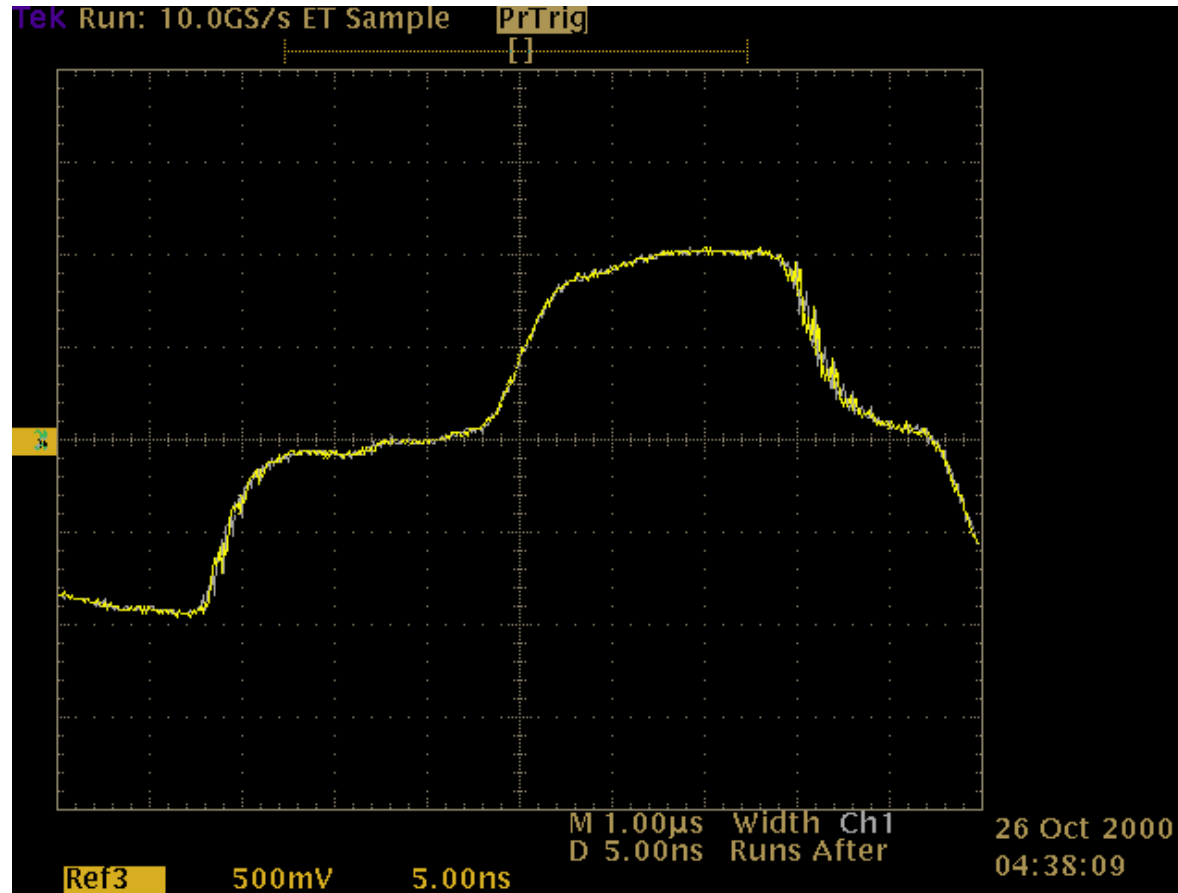


Tx Eye and Jitter, Power On, Discovery On, I = 300mA

Signal Integrity - 100M

Bad PHY

DTE power over MDI

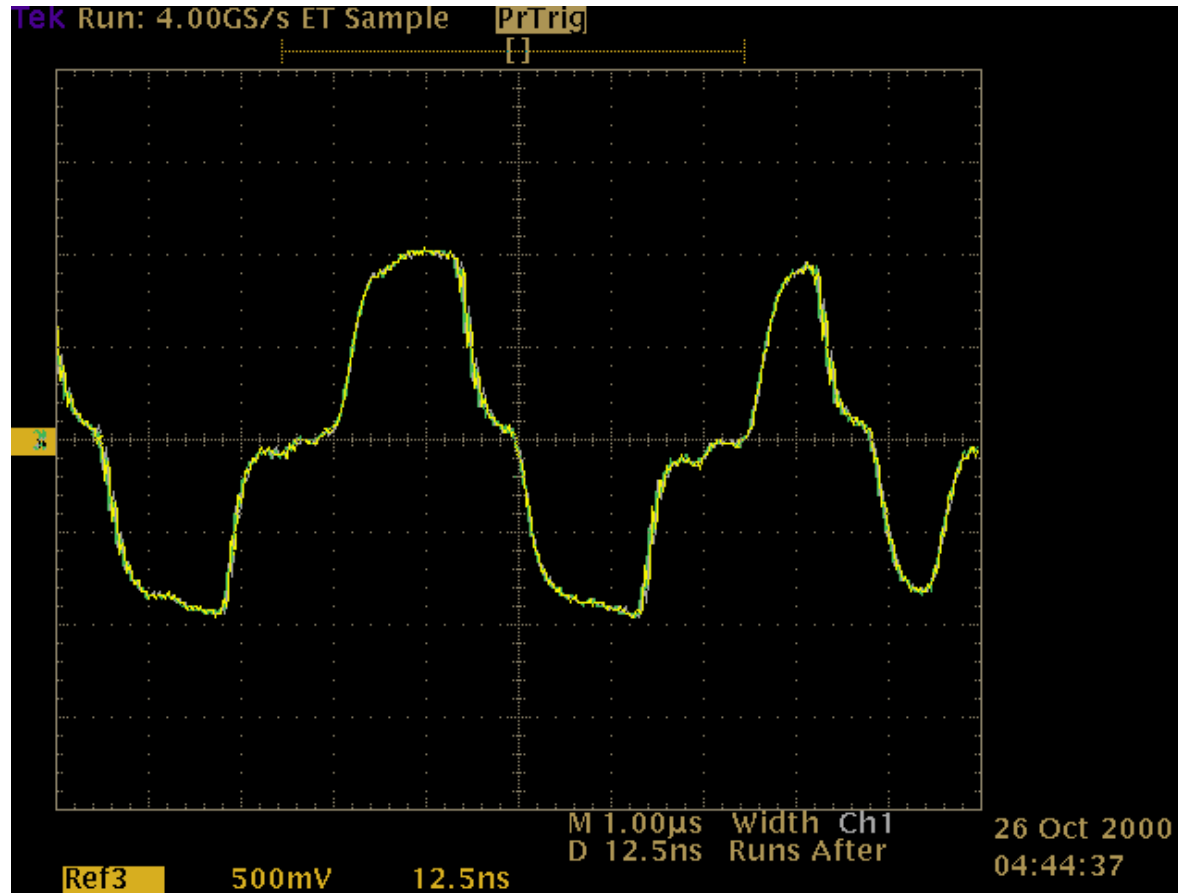


Tx Overshoot, All three conditions

Signal Integrity - 100M

Bad PHY

DTE power over MDI

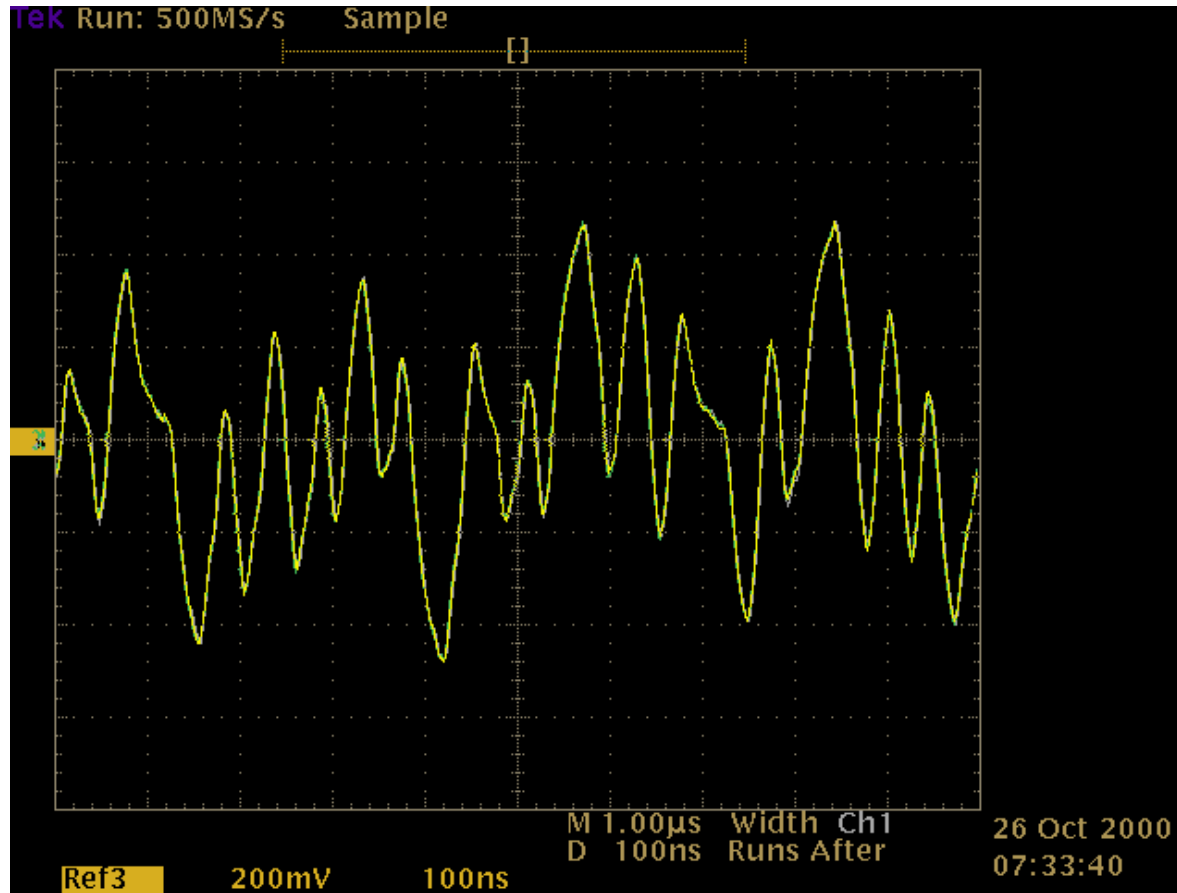


Tx Duty Cycle Distortion, All three conditions

Signal Integrity - 100M

Bad PHY

DTE power over MDI



Rx Waveform at 93m

Signal Integrity - 100M

Bad PHY – Results Summary

DTE power over MDI

Characteristic	Normal	Discovery	Power
Differential Signal			
Positive Peak	1.03V	1.03V	1.03V
Negative Peak	0.98V	0.98V	0.98V
Rise/Fall Time	3.9/3.2ns	3.9/3.2ns	3.9/3.2ns
Duty Cycle Distortion			
Positive Width	24.5ns	24.5ns	24.5ns
Negative Width	24.7ns	24.7ns	24.7ns
Transmit Jitter	1.96ns	1.96ns	1.96ns

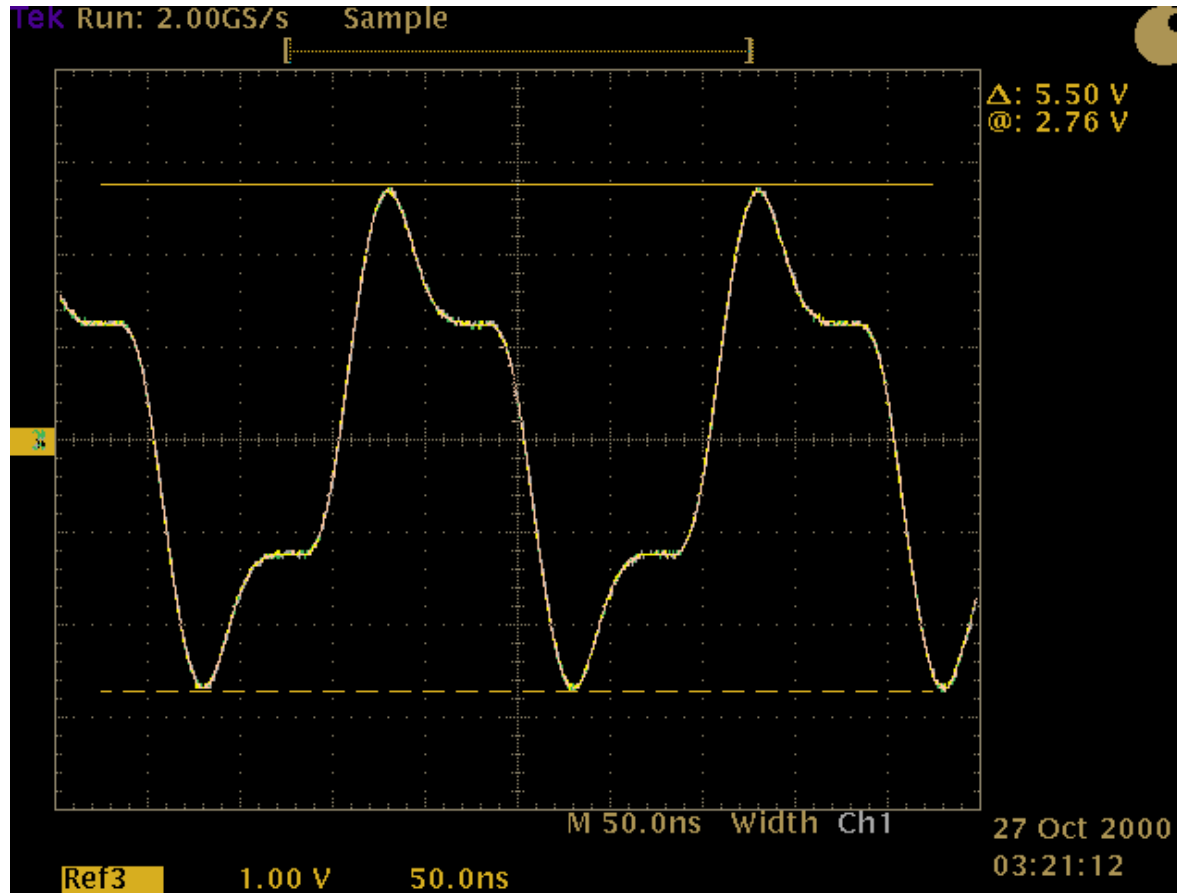
Signal Integrity - 10M

- Each PHY device had the following signal integrity tests carried out;
 - Peak Differential Output Voltage
 - Output Waveform vs Template
 - Start Of TP_IDL(End of 10Base-T Packet) waveform vs Template
 - Link Test Pulse vs Template
- These tests were carried out under the following conditions
 - No Power, No Discovery
 - No Power, Discovery running continuously
 - Power On, Discovery On, 300mA Load

Signal Integrity - 10M

Good PHY

DTE power over MDI

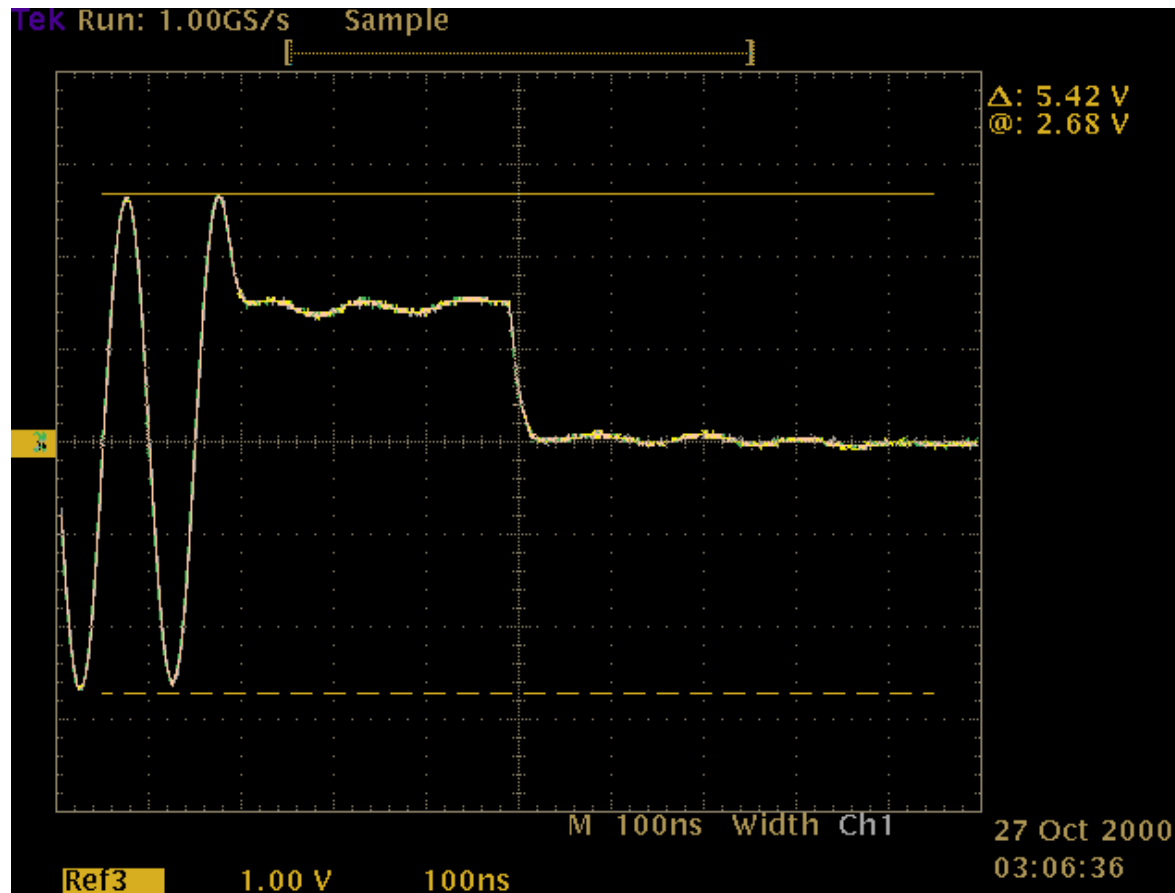


10Mbit/s Signal, All three conditions

Signal Integrity - 10M

Good PHY

DTE power over MDI

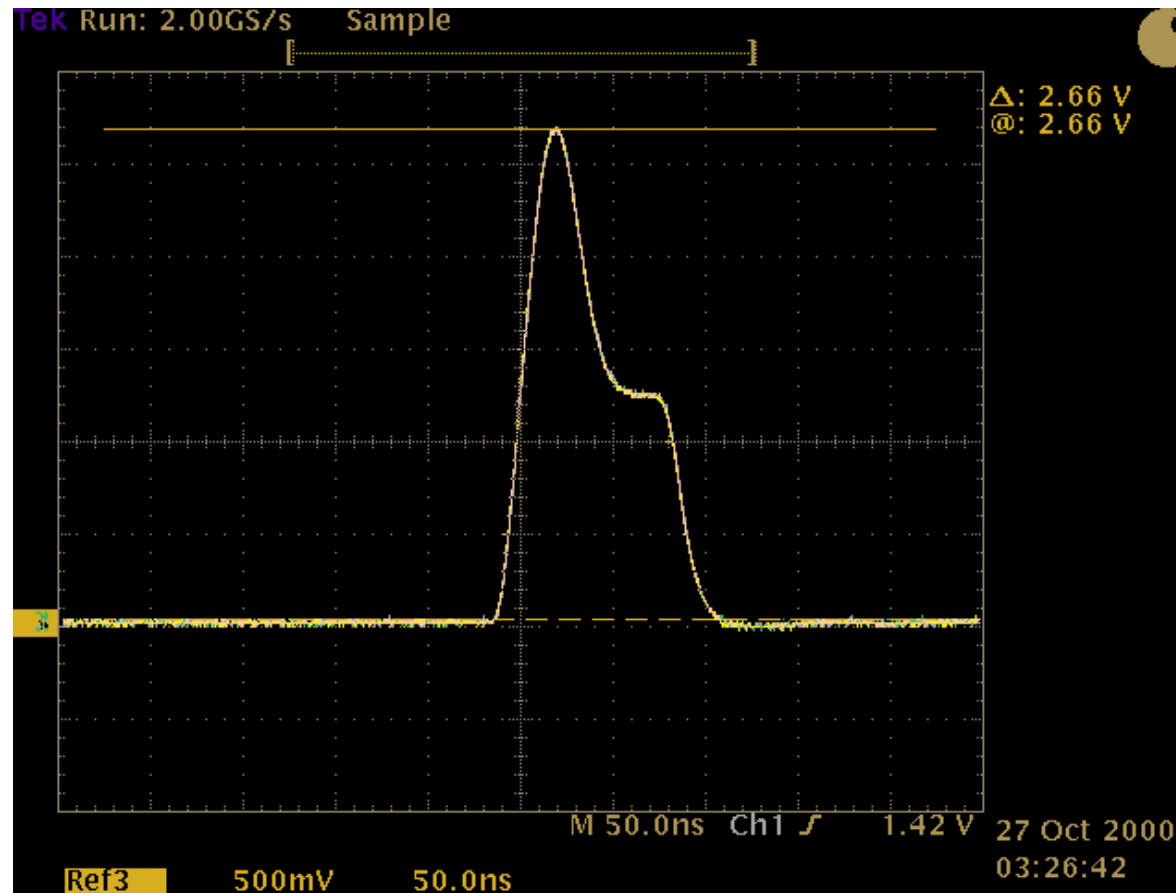


10 Mbit/s Start of TP_IDL, All three conditions

Signal Integrity - 10M

Good PHY

DTE power over MDI

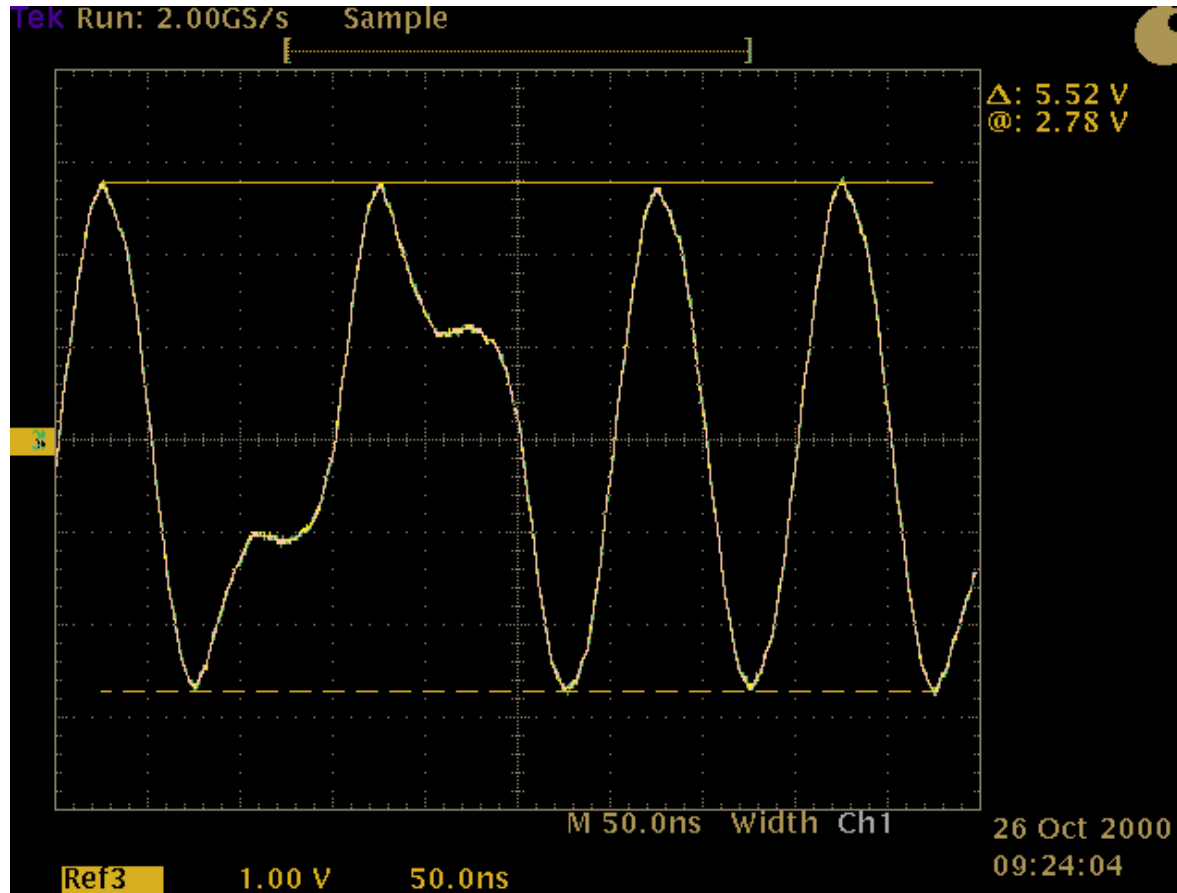


10 Mbit/s Link Pulse, All three conditions

Signal Integrity - 10M

Bad PHY

DTE power over MDI

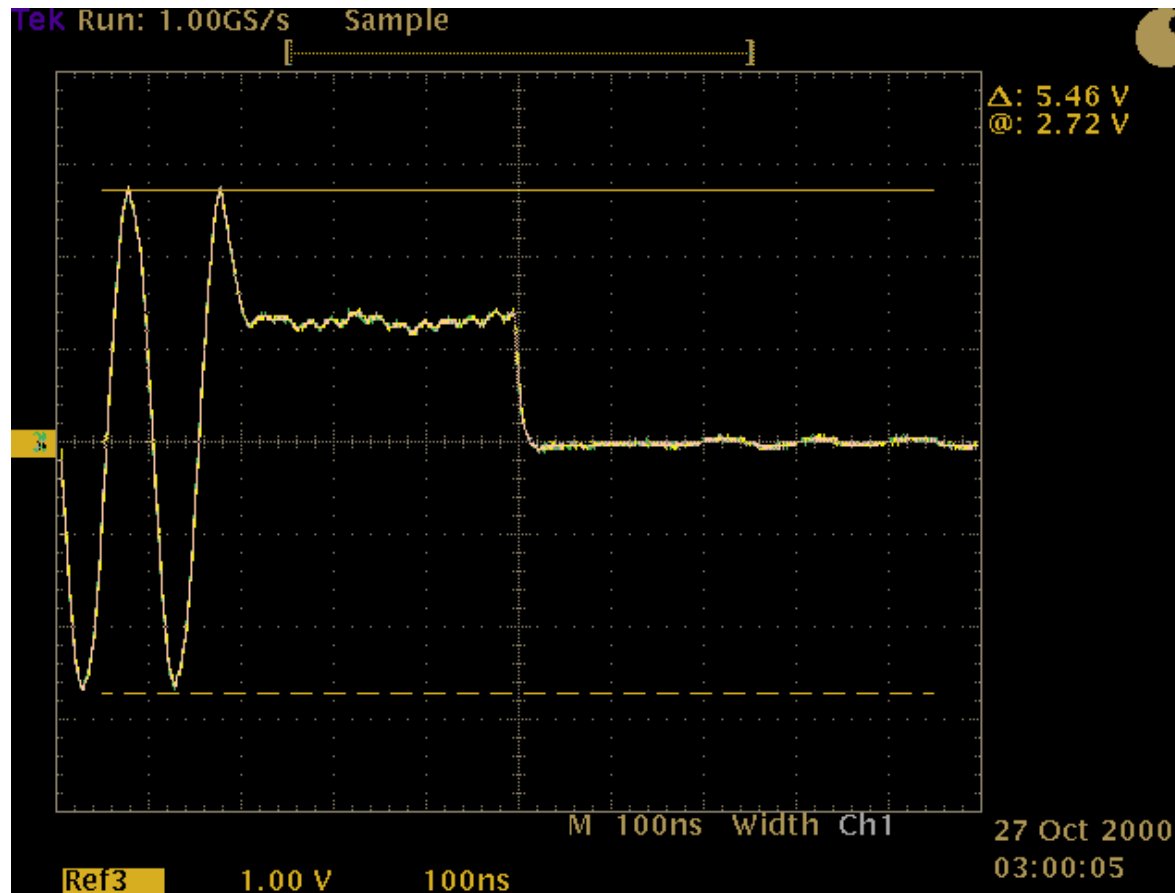


10Mbit/s Signal, All three conditions

Signal Integrity - 10M

Bad PHY

DTE power over MDI

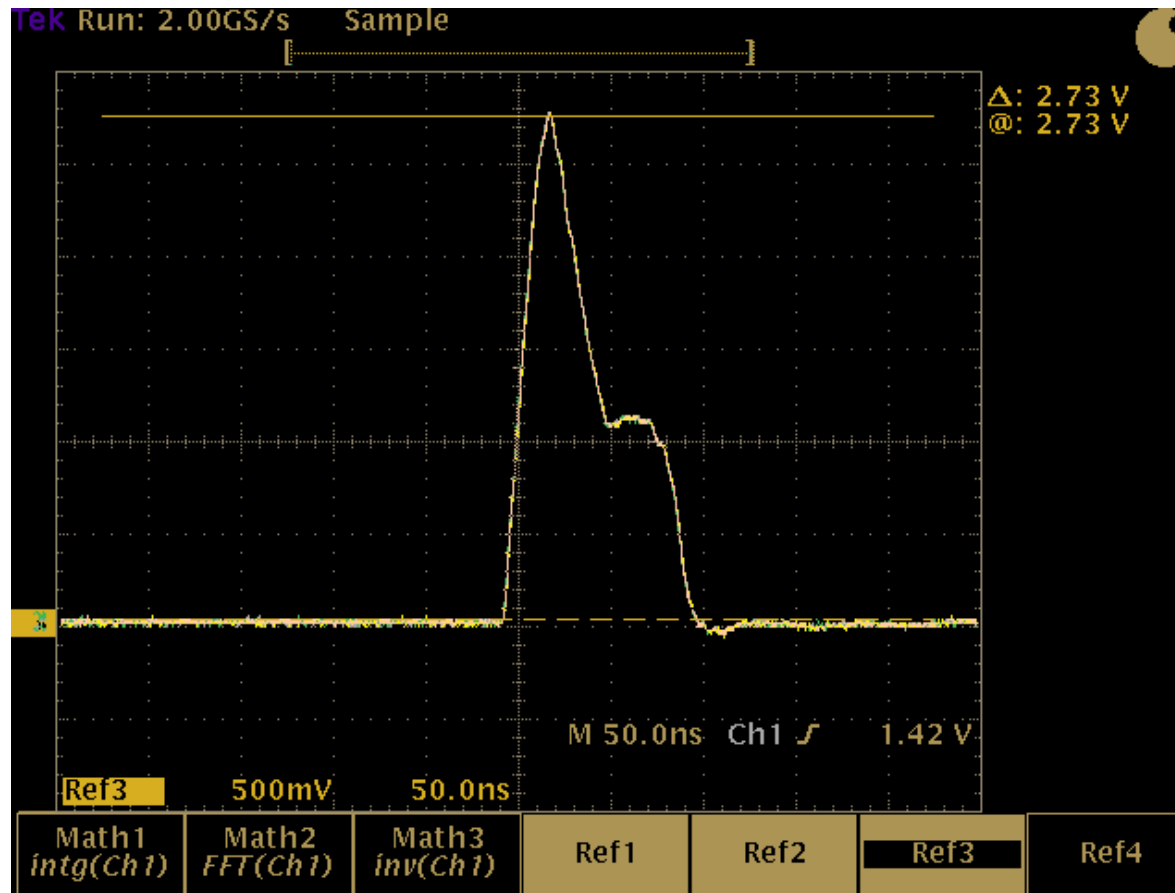


10 Mbit/s Start of TP_IDL, All three conditions

Signal Integrity - 10M

Bad PHY

DTE power over MDI



10 Mbit/s Link Pulse, All three conditions

Conclusions

- **The Diode Discovery Process does not degrade the performance of the MDI link.**
- **No degradation on the Signal pairs even when the Discovery Process is running at the same time as data transfer or idle signalling.**
 - It can be seen that the signals shown on this set of slides are degraded in comparison to the signals shown in the previous data for the idle pairs testing presented at the September meeting. This is due to the addition of the extra transformer included in the signal path to allow connection to the prototype board.
- **DC power transfer is still the major contributor to degradation on the MDI link.**