Resistor Signature Analysis

IEEE 802.3af DTE Power via MDI Meeting

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Resistor Signature Analysis

• **Basics**
• Technical Concerns
  – High Impedance
  – ESD
• Signature Impedance
  – Voltage versus Current Plot
  – Leakage
  – Diode Voltage
• Tolerance
Signature Detection

• PD with
  – 25K Resistor
  – Isolation Circuit

• PSE with
  – Probe Circuit
    • 75K Resistor
    • 12 or 24 volt detection voltage
  – Power Switch
PSE Probe Circuit

• No Damage to Loop Circuits
  – Limit Probe Voltage
  – Limit Probe Current
  – High Impedance
Detection Probe

• DC Source
  – Thevenin Source
    • Series Resistance = 75K
    • Voltage = 12 volts and 24 volts
  – Norton Equivalent
    • Parallel Resistance = 75K
    • Current steps 0.16 ma and 0.32 ma
Why a Source Impedance is needed

• Needed to detect an un-powered PSE
  – Current Probe PSE looks like open circuit
  – Voltage Source Probe looks like short
  – Source Impedance must differ from Signature Impedance

• High Impedance makes Probe more Robust
Why Multiple Measurements

- Single measurement can pass with a big cap load.
  - As the capacitor charges or discharges it can create the loop voltage (or current) for signature detection.
- More robust.
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Why High Impedance

• Signature impedance = 25K
  – Power dissipation = 0.125 watts
  – Below minimum current threshold
• Detect impedance = 75K
  – Isc = 24/75K = 0.32 ma
  – Minimal Interference
• Noise Immunity
  – High Z does not attenuate capacitive coupling
High Impedance Noise Tests

• **Interference Test**
  – Switch between test voltages
  – Measure Voltage on open circuit loop

• **Noise Immunity Test**
  – Apply AC source on loop
  – Monitor A to D sense voltage
Interference Simulation Model

Source

Waveform
Open Circuit Loop Voltage
Spectrum
Open Circuit Loop Voltage
High Impedance Noise Tests

• Interference Test
  – Switch between test voltages
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  – Apply AC source on loop
  – Monitor A to D sense voltage
Noise Immunity Simulation Model
Noise Immunity Response
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K9 ESD Strategy

• Energy = Voltage * Current * Time
• Want at least one term to be equal to zero
  – Can’t block high voltage.
    • Current is not equal to zero.
    • Use high Impedance to limit circuit current.
  – Make Voltage low – provide easy path
    • MOSFET = Surge Rated Power Zener.
    • Surge current is passed to Power supply or PD
PSE Wire Interface
Resistor Signature Analysis

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PD Signature Impedance

- Simulation Circuit
- V – I plot of Signature Impedance
- Technical Concerns
  - Leakage
  - Diode Voltage
Signature Detection
Alternatives

- **Measure Loop Voltage**
  - \( V(\text{loop}) = \text{Voltage at PSE output} \)
- **Measure Detect Current**
  - \( I(\text{Rdetect}) = \text{Current flowing out of PSE} \)
Simulation Model

PARAMETERS:
Rsigt 25K
Resistor + Signature Plot
Signature V-I Plot
Temperature + Resistor Tolerance
Signature only

T = 0, 27, 50, 70 °C
Rdetect = +/- 1%
Rsig = +/- 2%
PD Impedance

• Signature similar to 30K Resistor
• Can be detected via V(loop)
• Can be detected via I(Rdetect)
DC Detection Problems

• Leakage Current
  – MOSFET switches
  – Diodes
  – Flux

• Diode Voltage
  – Function of Temperature
  – Function of Diode Type
Leakage

- MOSFET Switches
  - PD isolation
    - Low Probe Voltage
  - PSE Power Switch
    - (Battery – Probe Voltage) ~ 40 to 56 volts

- PD Diodes
  - Low Probe Voltage
Leakage

• Data Sheet
• Simulation Circuit
• Simulation Results
MOSFET Leakage

From MTD3055VL Data Sheet

Figure 6. Drain–To–Source Leakage Current versus Voltage
Leakage Simulation Model
MOSFET Leakage Current

![Graph showing MOSFET Leakage Current](image)

Probe Cursor:
- E1 = 0.000, 4.0002μA
- E2 = 10.000, 5.0003μA
- dif = -10.000, -1.0000μA
MOSFET Leakage

- **PSE MOSFET**
  - 4μA Constant Current
  - 10 Meg Resistance

- **PD MOSFET**
  - Negligible
Diode Leakage

Temperature = 0 27 50 70 degree C

1N4002 Diode
Diode Leakage

- Constant Current
  - Modeled via a Current Source
  - Varies with temperature

- Linear Resistance at origin
Leakage Model

• Norton Model
  – Constant Current source
  – Parallel Resistor to model slope
Constant Current Leakage

- Simulation Circuit
- Effect on Loop Voltage
Constant Current Leakage Simulation Model
Constant Current Leakage Effect on Vloop

- 24 volt detect voltage
- 12 volt detect voltage

**Probe Cursor**
- B1 = 0.000, 6.7457
- B2 = 10.000u, 6.5557
- dif = -10.000u, 190.039m

**Probe Cursor**
- B1 = 0.000, 3.6895
- B2 = 10.000u, 3.4966
- dif = -10.000u, 192.838m
Diode Voltage

• Temperature Variation

• Offset Voltage
  – Silicon Rectifier
  – Schotky Rectifier
  – MOSFET

• Series Resistance
  – Small signal AC resistance
Diode Offset Voltage Simulation Model

[Diode offset voltage simulation model diagram]
Diode Offset Voltage Effect on $V_{\text{loop}}$
Daisy’s Suggestion

• Don’t use individual measurements
• Only use the difference
Constant Current Leakage Effect on Delta Vloop

![Graph showing the relationship between Delta Loop Voltage and Current]
Diode Offset Voltage Effect on Delta $V_{vloop}$
Daisy Effect

• Constant Current Leakage does not contribute to delta measurement
• Diode Offset Voltage does not contribute to delta measurement
• The above create a DC Offset which is cancelled by the delta measurement
Detection Circuit

![Circuit Diagram](image)
Detection Circuit
Delta Measurement
Resistor Signature
Alternatives

• 25K Resistor
  – Resistor behind polarity guard
  – Resistor in front of polarity guard
Detection Voltage Summary

- Leakage effects Loop measurements
- Diode offset effects Loop measurements
- Delta measurement minimizes errors
  - Minimize Constant Current Leakage
  - Minimize Diode Offset Voltage
- Delta measurements do not detect diodes
Leakage – Resistive Component

• Norton Model
  – Constant Current Source
  – Parallel Resistance
• Norton Detection Circuit Model
• Lumped Model
DC Detection Model
Norton PSE

Diagram:
PSE MOSFET  Diode Leakage  PD MOSFET

- Iprobe
- IleakPSE
- Rdetect 75K
- RleakPSE
- IleakD
- RleakD
- Rsignature 25K
- D1N4002
- D1N4002
- D2
- 12/75K≈160uA
- 24/75K≈320uA
DC Detection Model
Delta Measurement
DC Detection Model
Lumped Leakage
Loop Resistance

- Loop equivalent Resistance =
  - $R_{detect} // R_{signature} // R_{leak}$
- Probe detect resistance = 75K
- Signature resistance = 25K
- Ideal Loop resistance
  - $75K // 25K = 18.75K$
# Loop Resistance with Leakage Resistance

<table>
<thead>
<tr>
<th>Leakage</th>
<th>Loop Resistance</th>
<th>% Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000 Meg*</td>
<td>18,749.65</td>
<td>-0.002%</td>
</tr>
<tr>
<td>100 Meg</td>
<td>18,746</td>
<td>-0.02%</td>
</tr>
<tr>
<td>10 Meg</td>
<td>18,715</td>
<td>-0.2%</td>
</tr>
<tr>
<td>1 Meg</td>
<td>18,405</td>
<td>-1.875%</td>
</tr>
<tr>
<td>500K</td>
<td>18,072</td>
<td>-3.75%</td>
</tr>
<tr>
<td>100K</td>
<td>15,789</td>
<td>-18.75%</td>
</tr>
</tbody>
</table>
Resistor Signature Analysis

• Basics

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  – High Impedance
  – ESD

• Signature Impedance
  – Voltage versus Current Plot
  – Leakage
  – Diode Voltage

• Tolerance
Detection Tolerance

- What’s possible
- PD Tolerance
- PSE Tolerance
- Leakage
- Budget
- What’s needed
PD Tolerance

- Signature Resistor = 25K  +/- 1%
- Choice of:
  - Resistor in front of Diodes
  - Resistor behind Polarity Guard
- Diodes – cancelled by delta  0%
- Isolation Switch – low leakage  0%
- Misc.                    +/- 1%

- Total                    +/- 2%
PSE Tolerance

• Micro-controller with A to D converter
  – Very precise measurements
    • 10bits = 0.1%

• Reference Signature Circuit
  – Cancel Detect voltages

• Delta Measurements
  – Cancel Leakage and Diode drops

• Accuracy dependent on Resistor Matching
PSE Alternatives

• 1% Discrete Resistors
• Precise PSE
  – Matched Resistor Network
    • Laser Trimmed Thick Film Resistor Network
  – Micro Correction
    • Gain and Resistor Variation stored in Memory
    • Requires accurate Test Circuit
Tolerance Budget
PSE - 1% Resistors

- PD: +/- 2%
- PSE: +/- 6%
- Leakage - 1 Meg: +0/- 2%
- Margin: +/- 1%
- Total: +/- 10%
Tolerance Budget
Precise PSE

- PD: +/- 2%
- PSE: +/- 1%
- Leakage - 1 Meg: +0/- 2%
- Margin: +/- 1%
- Total: +/- 5%
Tolerance Budget

- Signature Resistor  +/- 2%
- Diodes           +/- 1%
- Leakage - 500K    +0% / -5%
- PSE              +/- 6%
- Margin          +/- 4%
- Total            +/- 15%
Tolerance Budget
More Conservative

- Signature Resistor: +/- 2%
- Diodes: +/- 2%
- Leakage - 200K: +0%/-10%
- PSE: +/- 10%
- Margin: +/- 6%

- Total: +/- 25%
What’s Needed

• Do not false detect
  – 2 Parallel PDs $25K // 25K = 12.5K$
    -50% tolerance
  – Unpowered PSE $75K$
    +200% tolerance
Tolerance Budget
What’s Needed

• Signature Resistor  +/- 2%
• Diodes  +/- 2%
• Leakage – 100K  +0% /- 20%
• PSE – Simple Analog Circuit  +/- 20%
• Margin  +/- 6%

• Total  +/- 40%
Resistor Signature Summary

• Signature Impedance – 25K
• Probe Impedance – 75K
• DC detection
  – Daisy Method = Delta Measurements
    • Eliminates constant current leakage
    • Eliminates diode offset voltage
  – Effected by linear leakage resistance
  – Can tolerate wide tolerance
Robust

• DC detection
• High Impedance
  – Immune to high frequency
  – Can’t Interfere
• PSE
  – Survived ESD
Signature

Resistor

Almost DC
High Impedance

Coupled Diode

us Pulses
Low Impedance