IEEE 802.3 DTE Power via MDI
Analysis and Implementation of Coupled Diode Detection

Presented by PowerDsine:

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Coupled Diode Method
Defining parameters for cost-effective implementation

- **PD Section**
  - Isolating Circuit

- **PSE (Switch, Mid-Span)**
  - Probing signal feeding methods with coupling transformer
  - Two transformers implementation
  - Single transformer implementation
  - Silicon implementation

Acknowledgment to Rick Brooks & Larry Miller / Nortel
Their previous work is used as the baseline for this presentation

PD Section - Isolating Diode Bridge Rectifier

- Advantages
  - Simple
  - Polarity insensitive.
  - Low Cost

- Issues to address
  - Power & voltage drop (1Wmax, 3Vmax), reduces PD available power
  - Transmitted pulse amplitude is limited to 4Vd, practical value about 2Vmax.
  - Actual detected pulse amplitude is approximately 1V

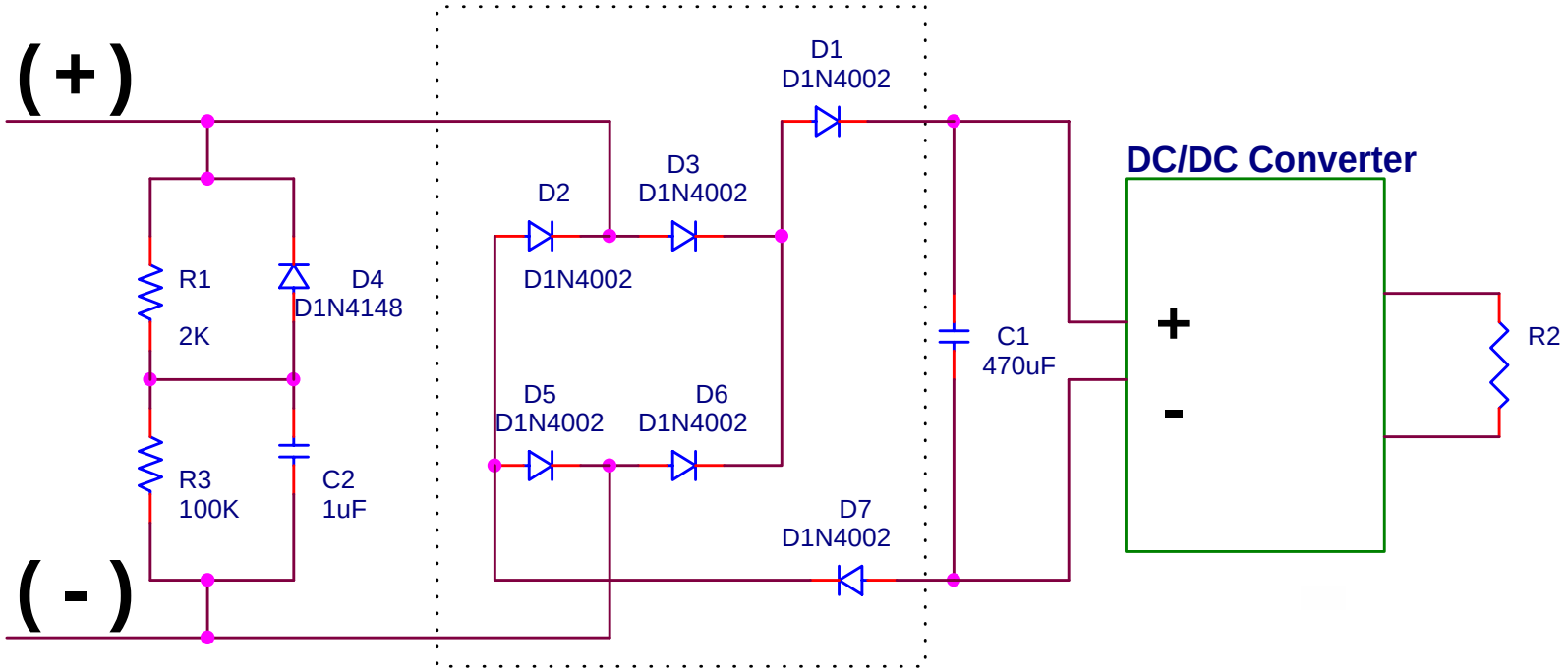
PD section- Enhanced Isolating Circuit

- Reliable implementation must include an Under Voltage protection circuit as part of the PD power supply input*

- The UV circuitry may be utilized as the isolation block between the Coupled Diode signature element and the PD power supply

* Refer to the PowerDsine IEEE 802.3af May 2000 presentation

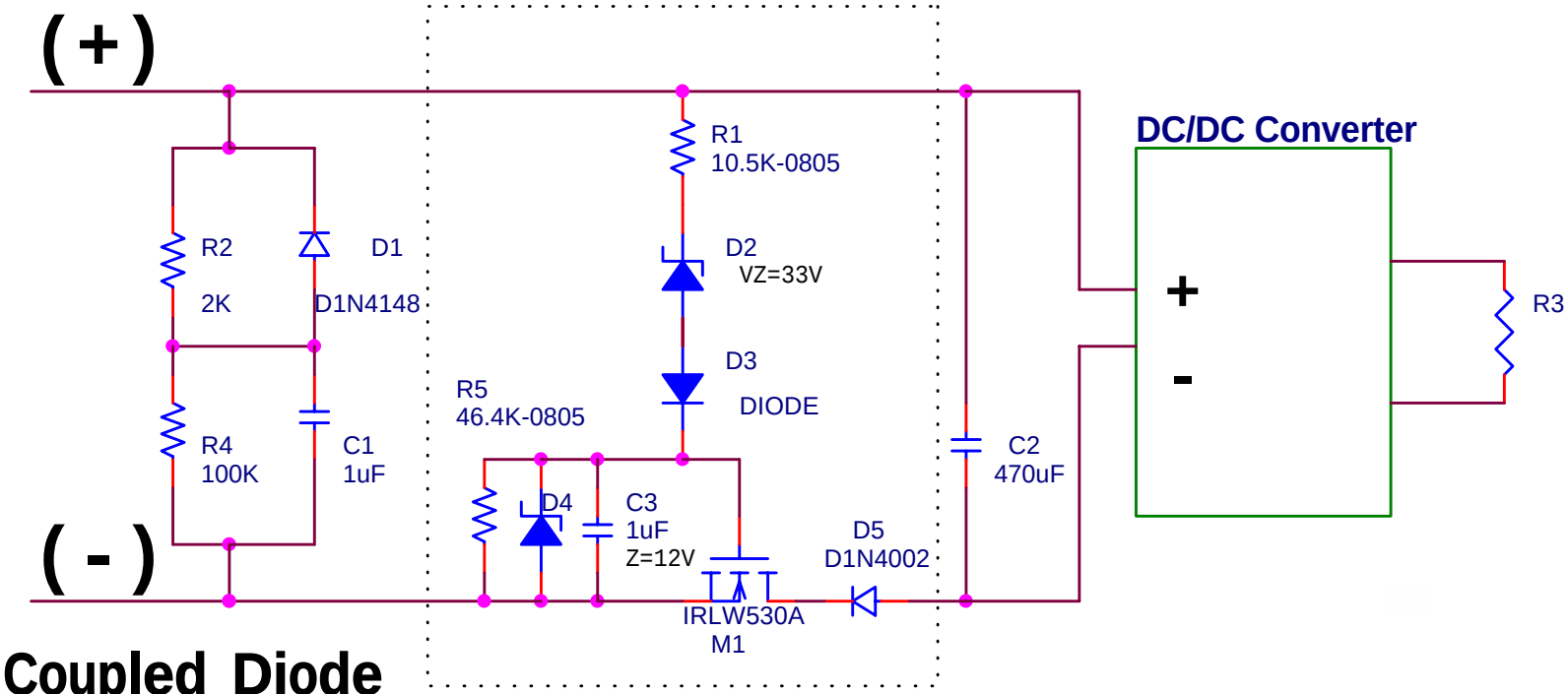
PD Section - Isolation Circuitry



Coupled Diode

Isolating Circuit

PD Section - Enhanced Isolation Circuitry



* Hysteresis circuitry may be added for setting different On/Off thresholds

PD section - Enhanced Isolating Circuitry

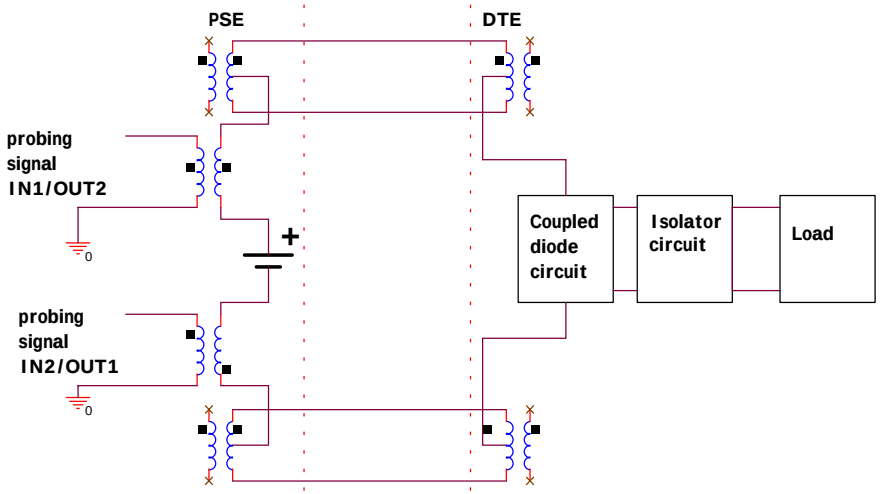
- Utilizing the existing UVLO
- Increases PD available power by reducing diodes power/voltage drop
- Probing pulses amplitude value range can be widen to improve signal to noise ratio and lower detected pulse sensitivity to circuit elements tolerance
- Lab testing confirms that the detected pulse shape is highly similar to one measured using the Diode Bridge

PSE - Pulse Amplitude Limitations

Setup A

Nortel proposed setup

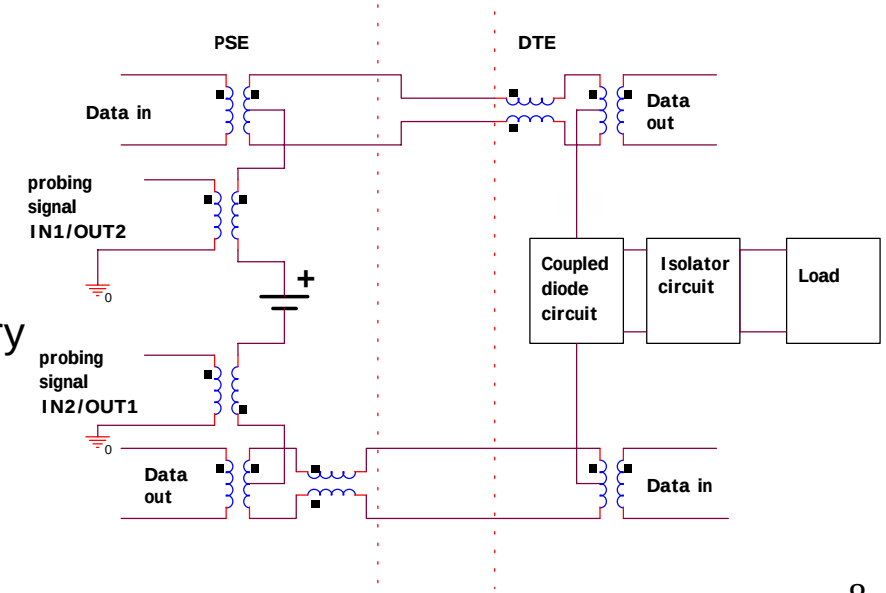
- Mid-Span solution architecture



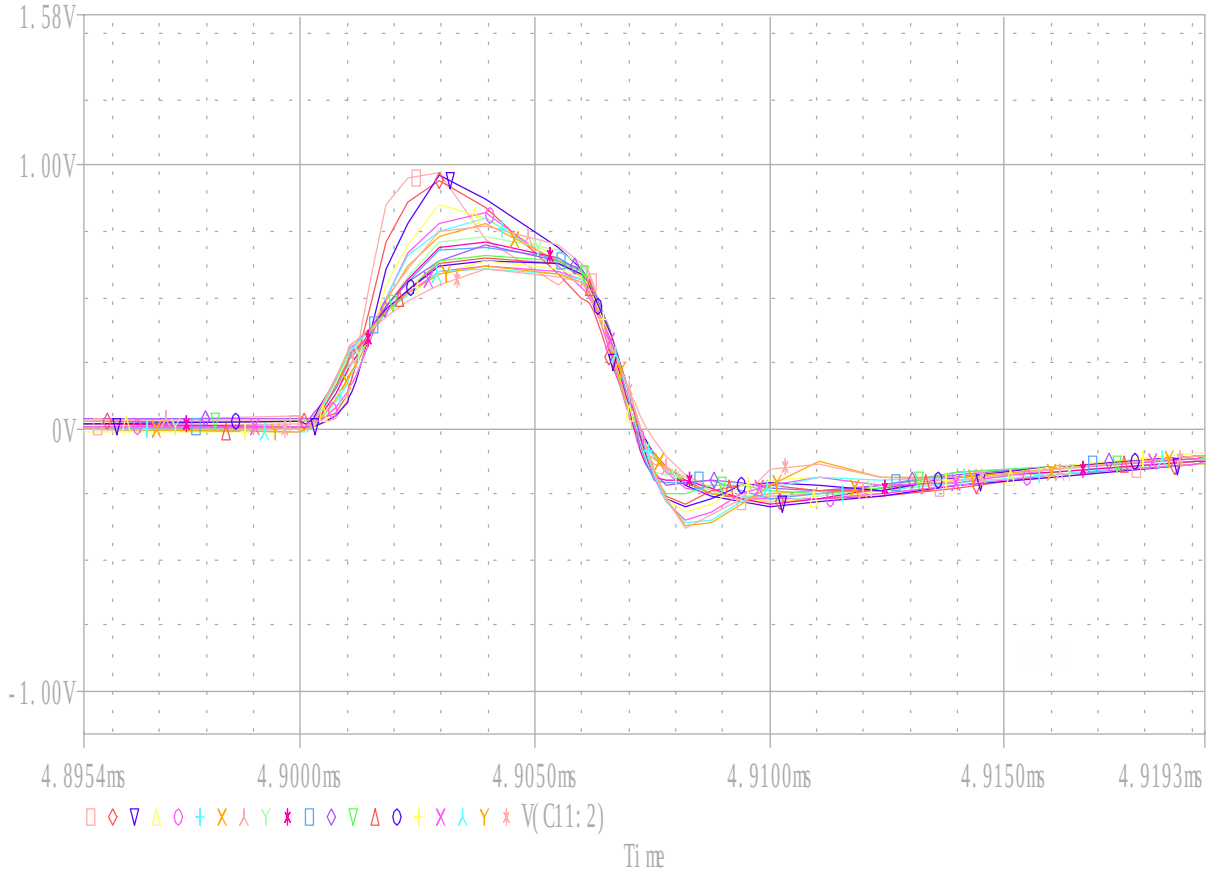
Setup B

Power is Phantom fed through standard data transformer module including integrated data path common mode filter

- Switch solution architecture
- Common mode filter inductance may vary in range of 2-120uH (depends on application, vendors etc.)

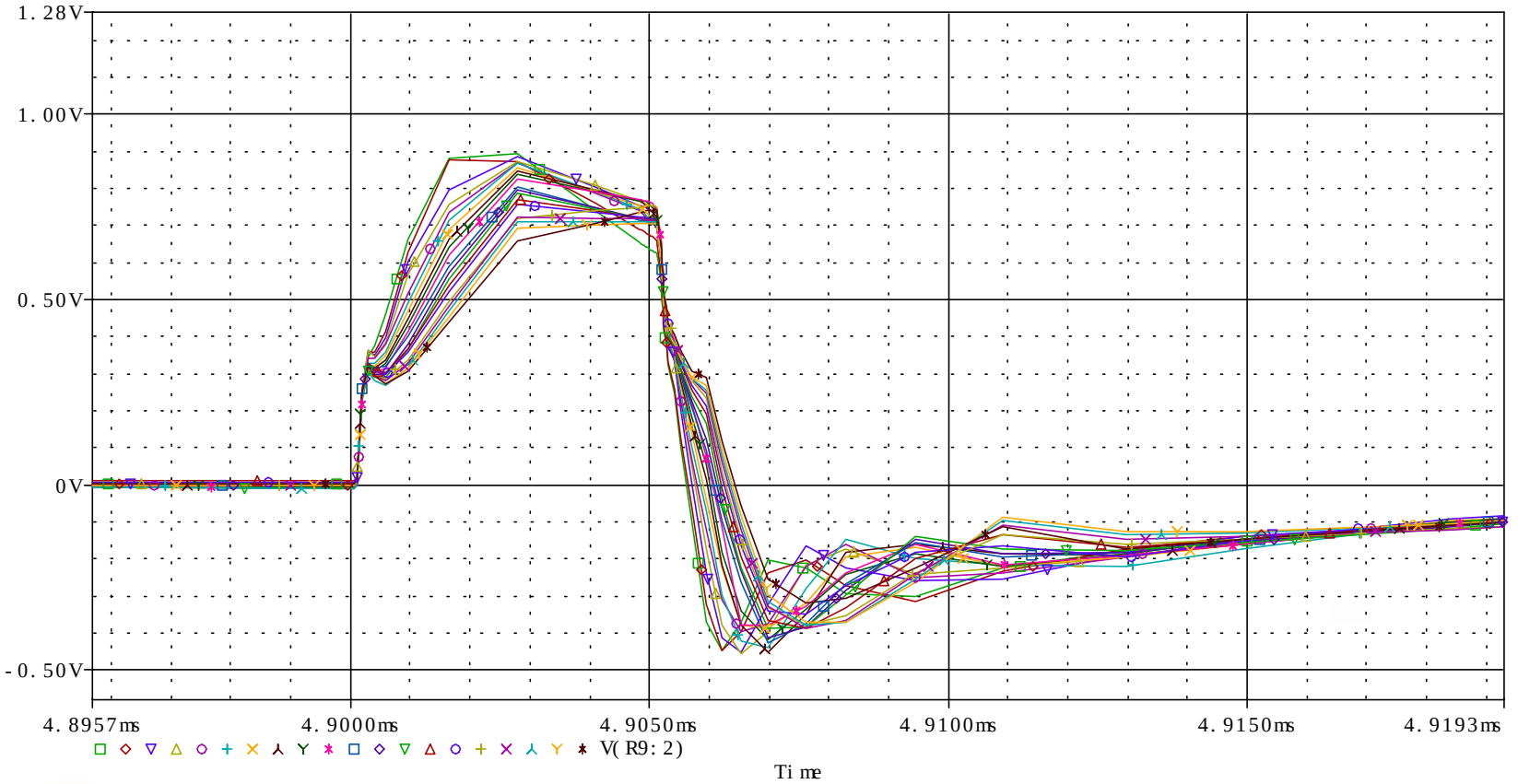


Detected Pulse Shape Vs. Link Length



Setup A: Link length=0-100m, 5m steps

Detected Pulse Shape vs. Link Length



Setup B: Link length = 100m, 0-100uH Common Mode inductance, 5uH steps

Refer to Annex C for details

Recommendations

Setup A:

- Detected signal shape changes within acceptable detected and processed range

Setup B:

- Pulse leading edge changes significantly with series inductance
- Pulse sampling time should be positioned close to tailing edge for robust detection

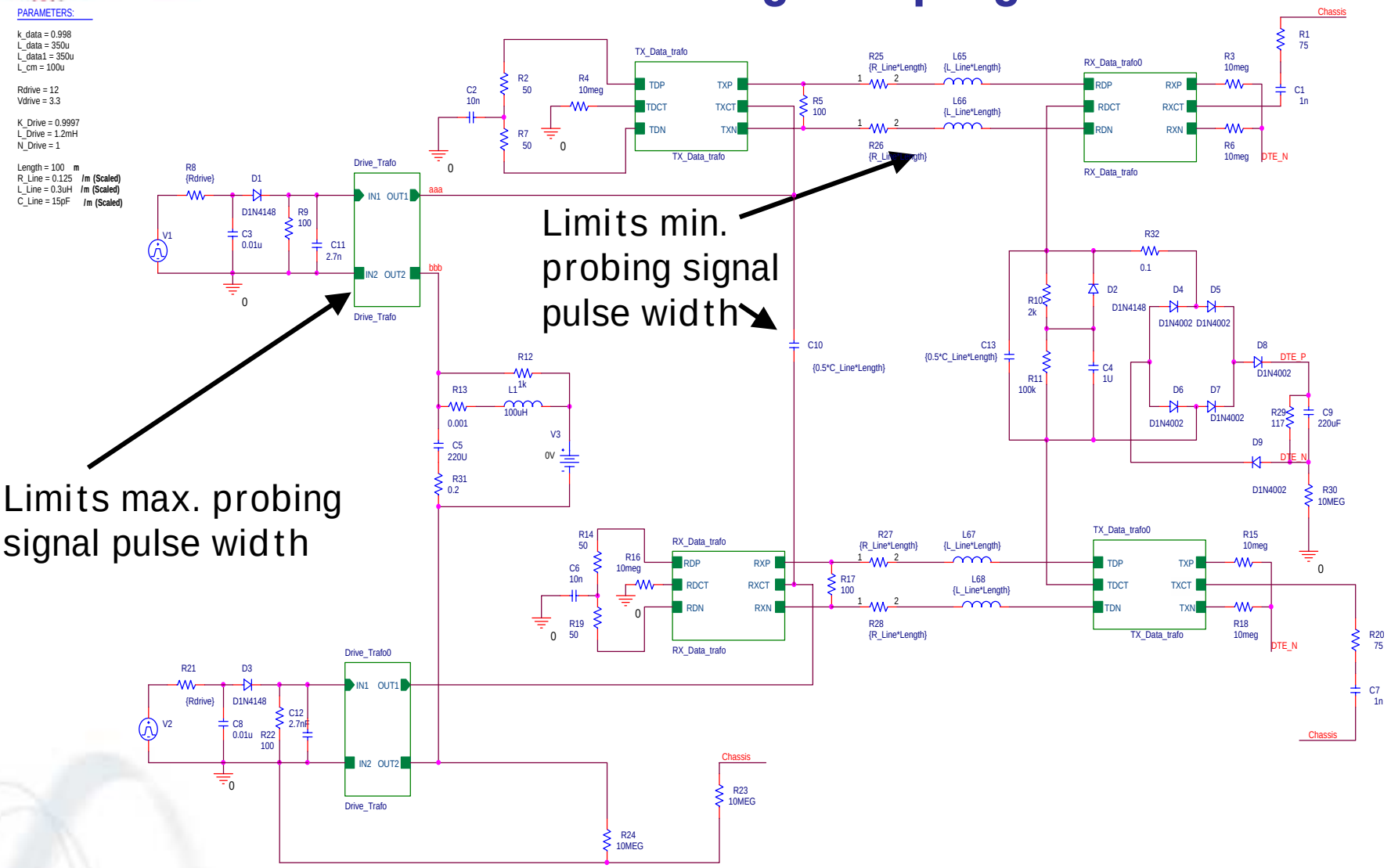
Note

- While power over MDI is supplied the Common Mode filter inductance that is located inside the link will be significantly reduced due to core saturation. This may affect common mode noise rejection. Consider locating Common Mode filter external to the link side

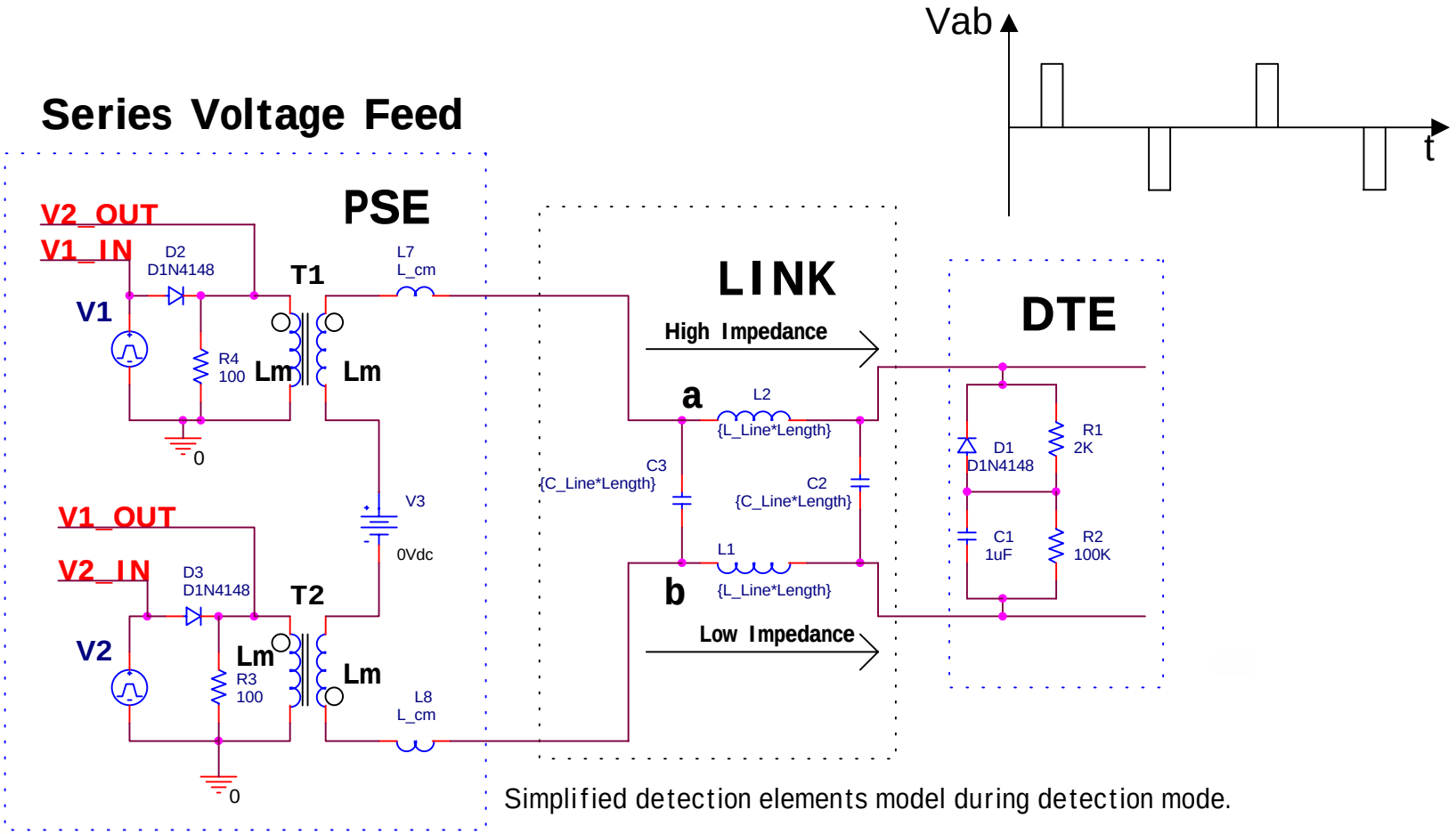
PSE Detection Circuitry Implementations

- Proposed coupled diode concept requires two coupling transformers
- Questions
  - Can we reduce it to single transformer?
  - Can we find solutions that can fit on Silicon?
- Goal:
- Specifying pulse shape parameters which do not limit the implementation methods

Two Transformers Circuitry
Can We Reduce it to a single Coupling Transformer?



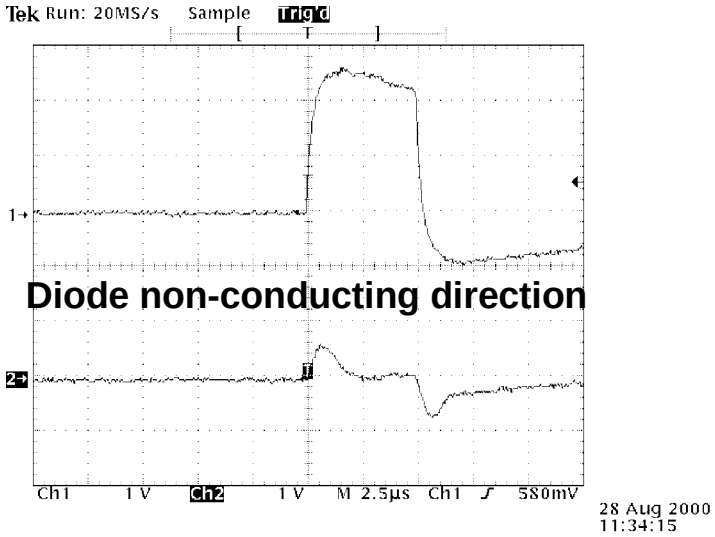
Simplified Two Transformer Circuitry Representation

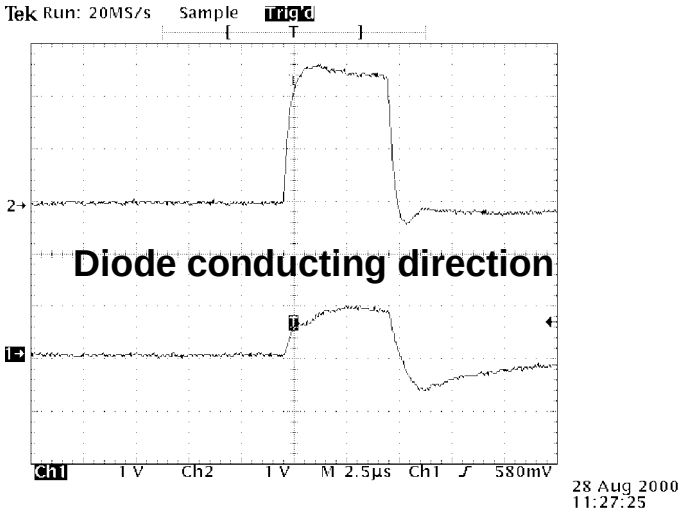


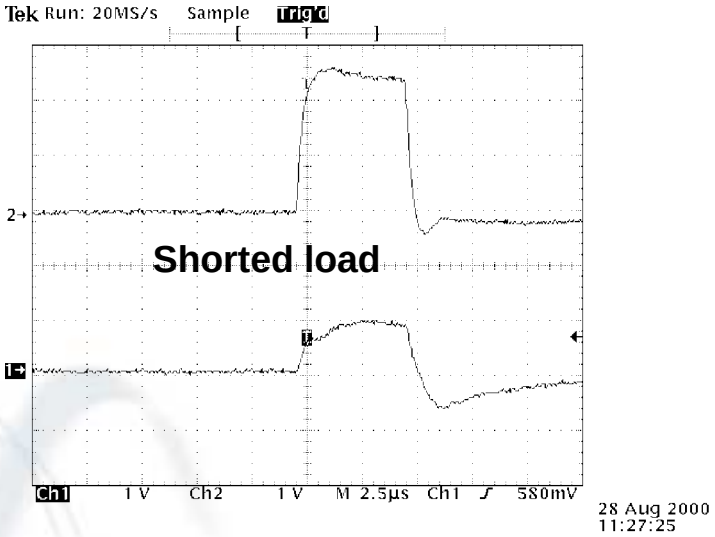
Simplified detection elements model during detection mode.

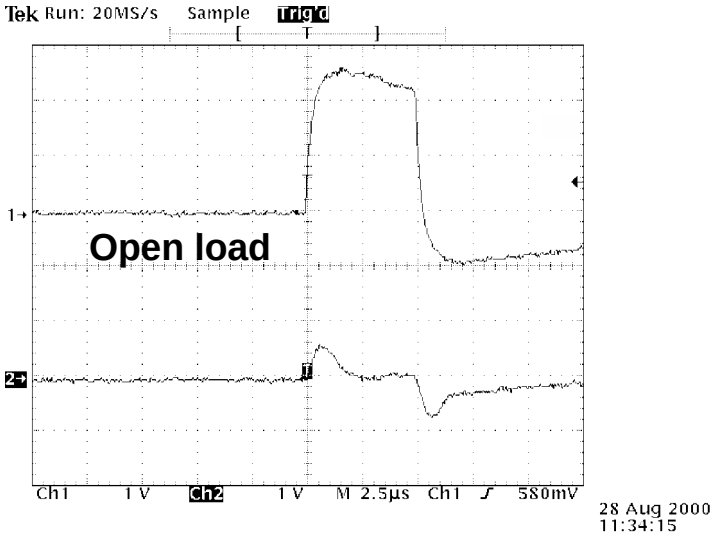
Sensed voltage wave shape is within acceptable distortion level while Lm>> Total Series impedance (Refer to Annex A for details)

Two Transformer Circuit - Test Results
Setup A & B measurements,100m Cat 5 UTP cable

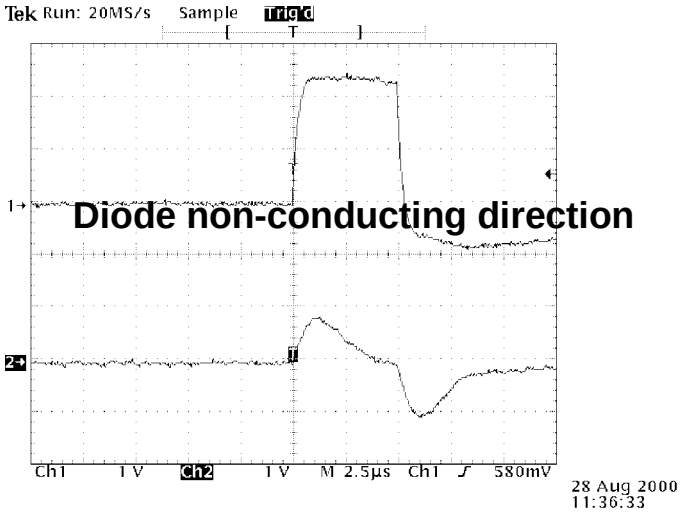


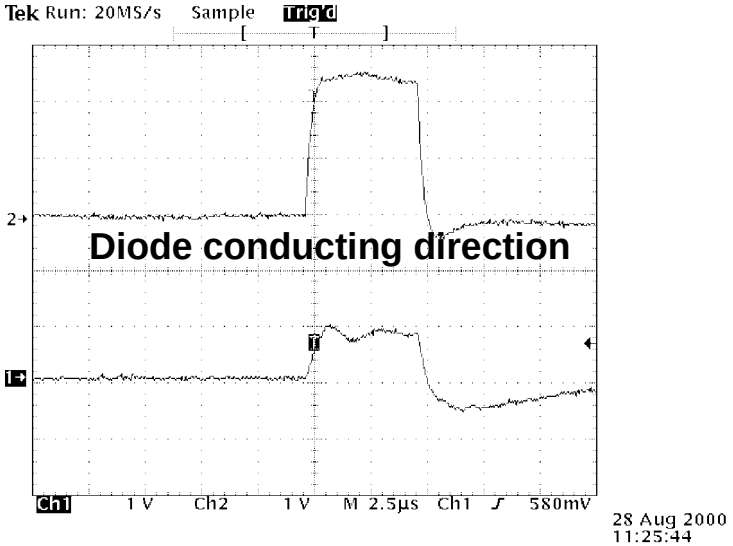


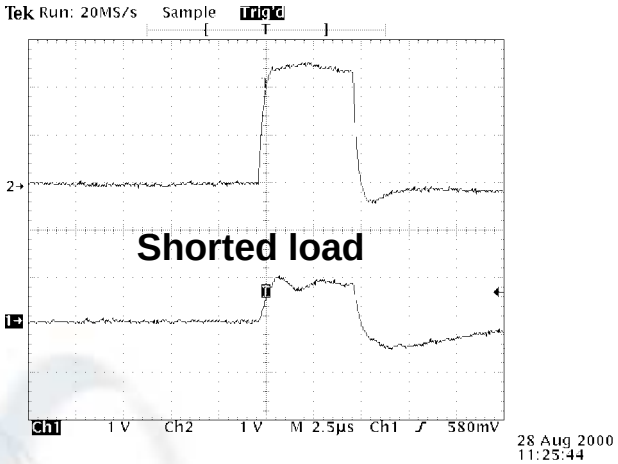


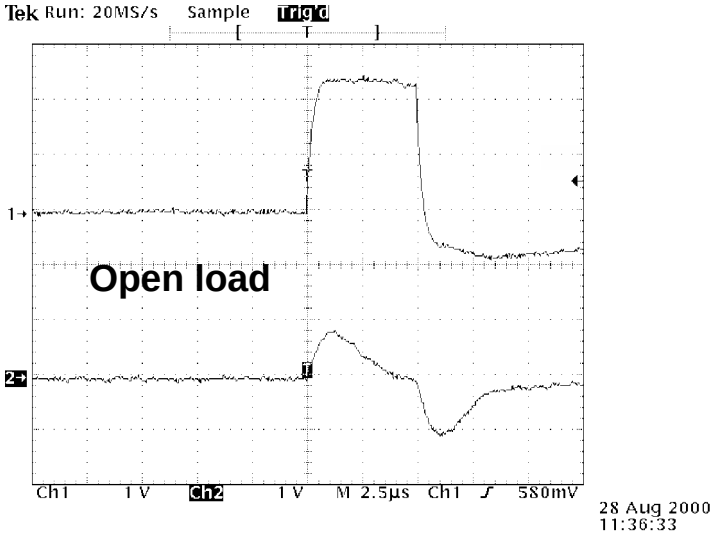


Two Transformer Circuit - Test Results
Setup A & B measurements,100m Cat 5 FTP cable

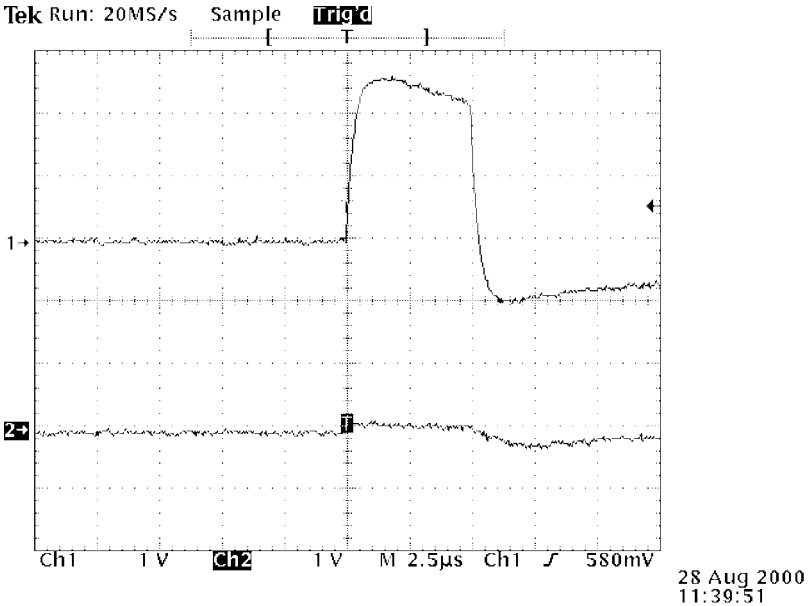




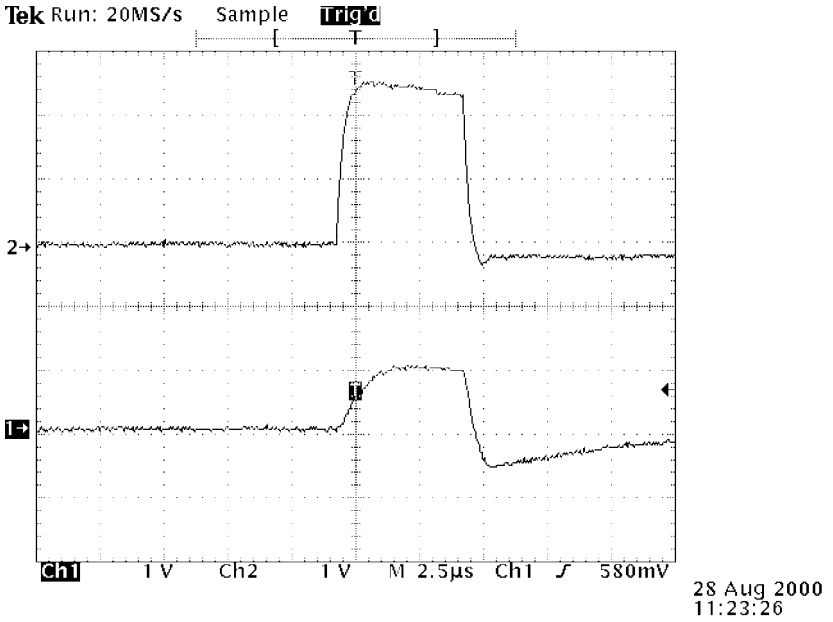




Two Transformer Circuit - Test Results
Setup A & B measurements,0.2m Cat 5 FTP/UTP cable



Diode non-conducting direction

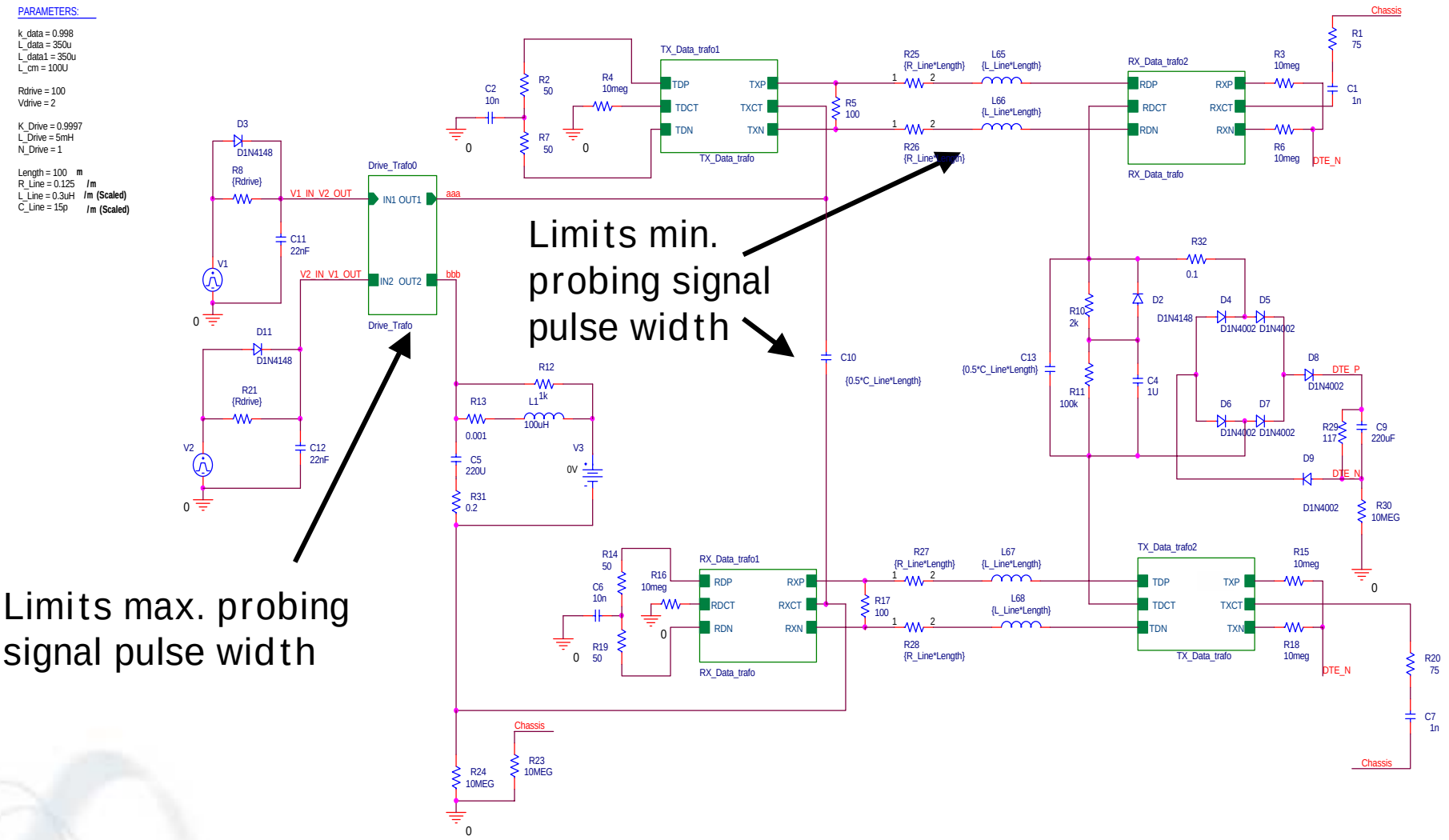


Diode conducting direction

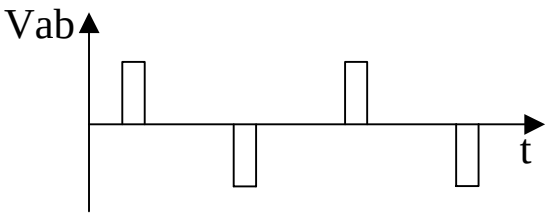
Two Transformer Circuit - Test Results

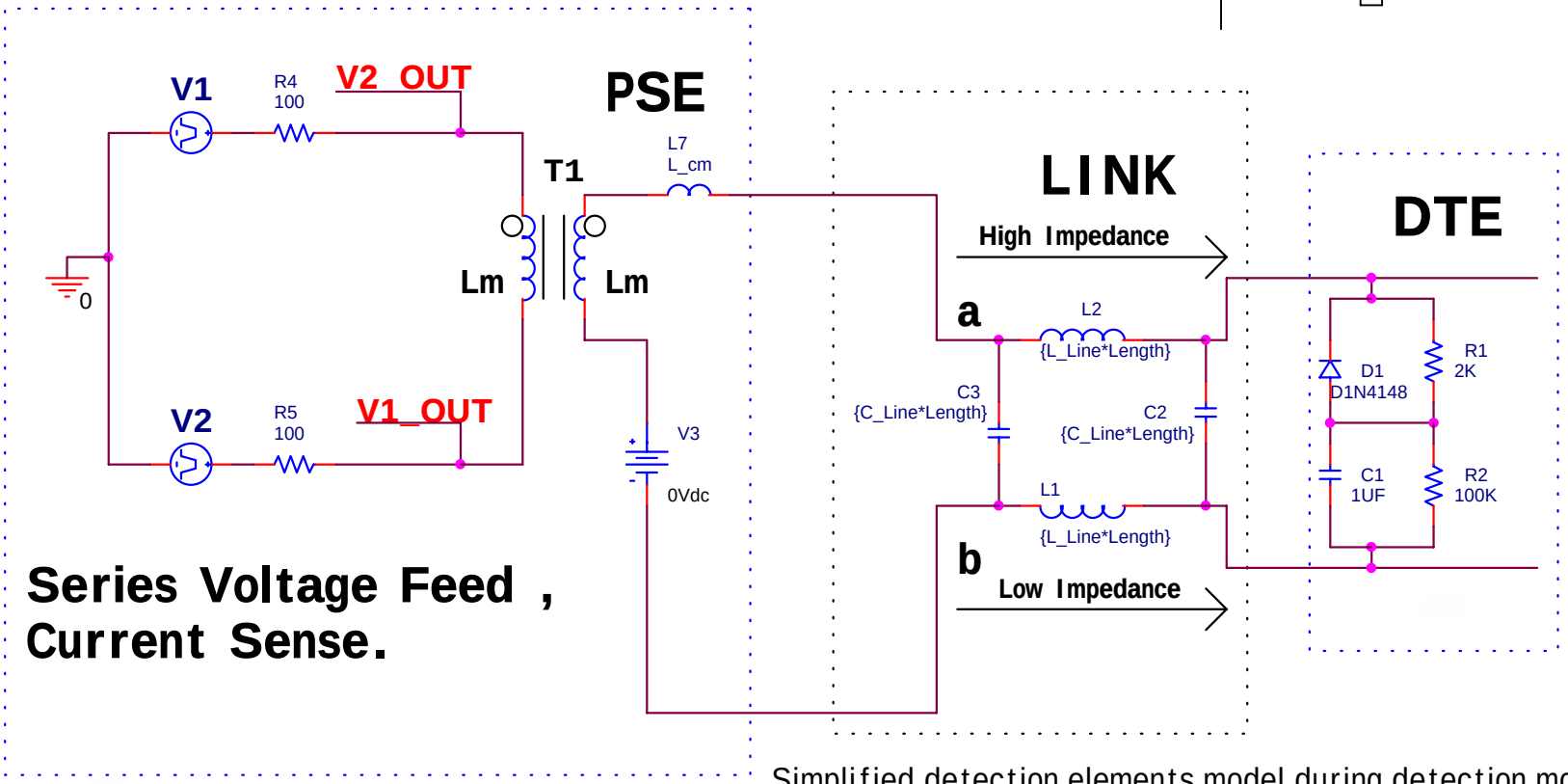
- Measured results confirm those presented by Rick Brooks & Larry Miller / Nortel at the July 2000 meeting
- The detected signal is affected by the Cat 5 cable equivalent input capacitance between pairs (by-passing Coupled Diode Signature element)
  - Simple High Pass filter at receive side can improve performance

Reduction to Single Transformer Circuit



Simplified Single Transformer Circuit Model





Simplified detection elements model during detection mode.

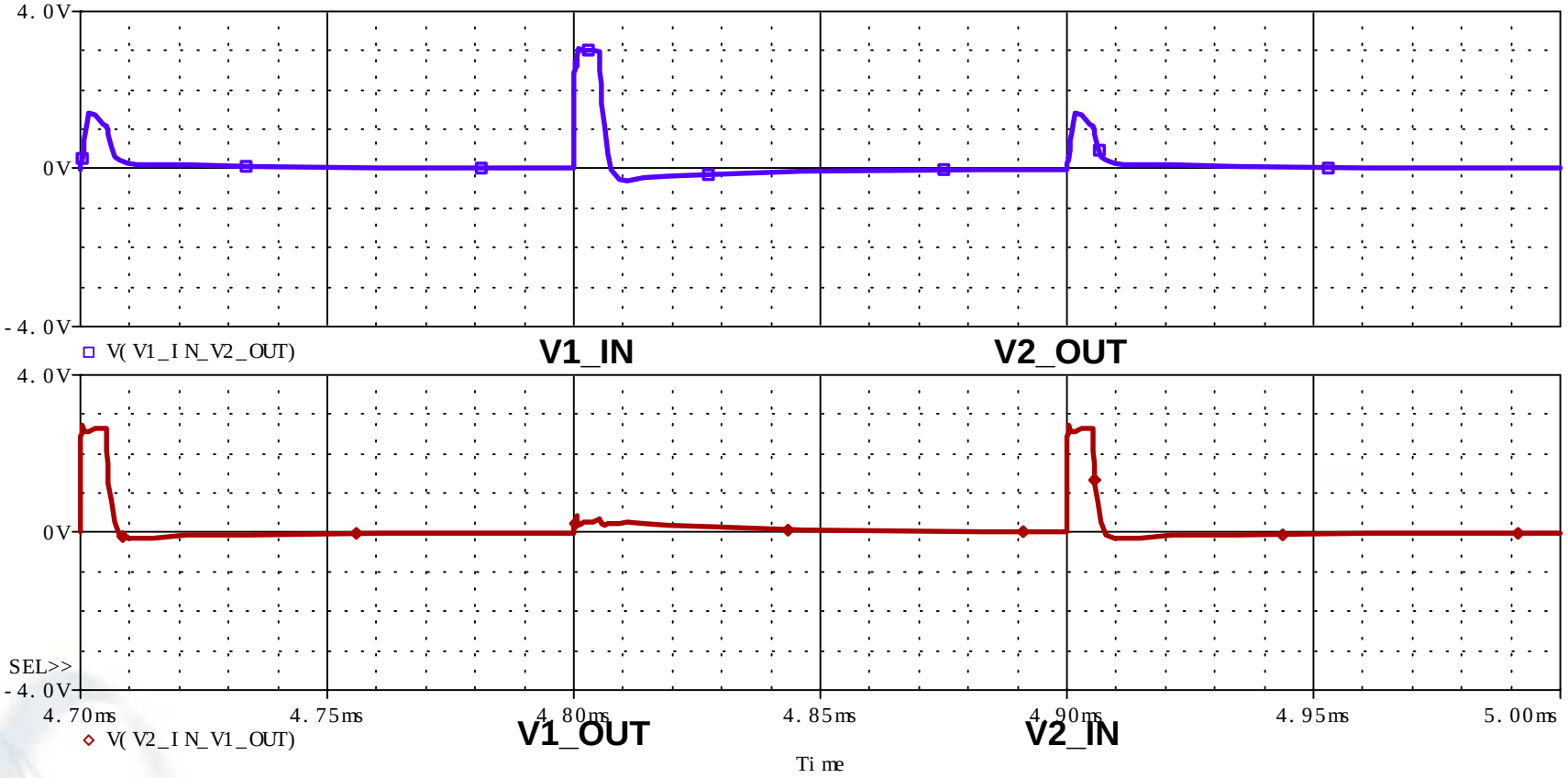
Sensed voltage wave shape is within acceptable distortion level while Im << Ishort (Refer to Annex B for details)

Single Transformer Circuit – Concept Principles

- Coupling transformer primary inputs are driven with two low impedance pulse source introducing 180 degree phase shift.
- Sensing Primary current for short / open condition (Coupled diode is conducting or reversed biased)
- Primary winding is always closed circuit to ground.
  - Clean and noise-free pulse shape at secondary.
- Pulse parameters requirements are compatible with 2 transformer solution

Single Transformer Circuit - Simulation

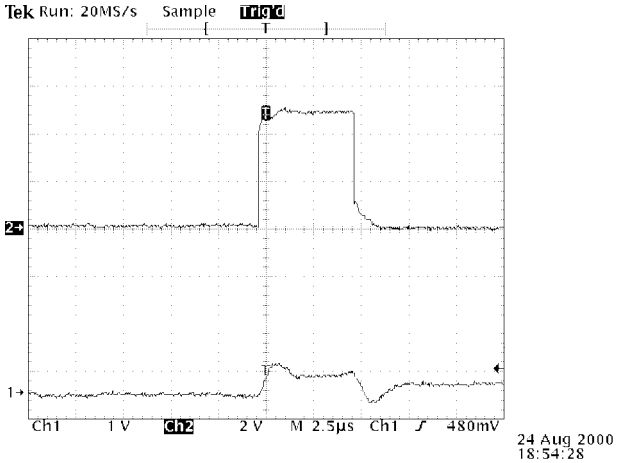
- Setup: 100m Cat 5 UTP cable
- Cable parameters measured between pairs 4/5 to 7/8 and 1/2 to 3/6



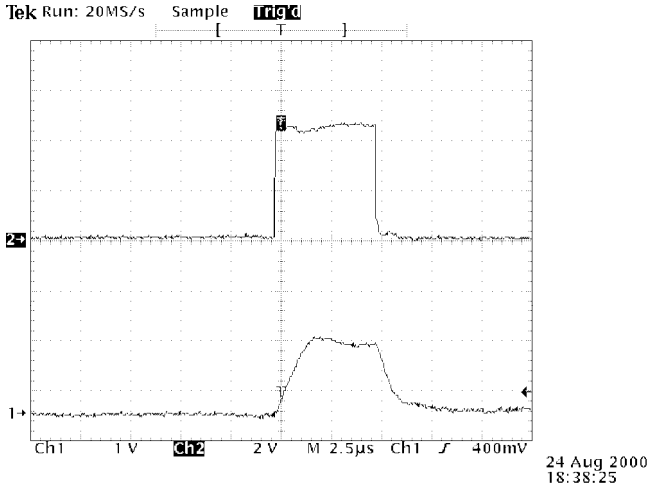
Single Transformer Circuit - Measurements

IEEE 802.3af, Sep. 2000.

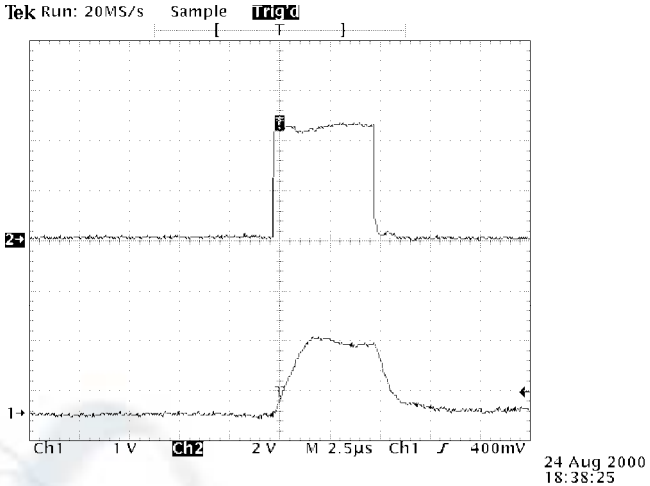
Setup A & B, 100m Cat 5, UTP cable



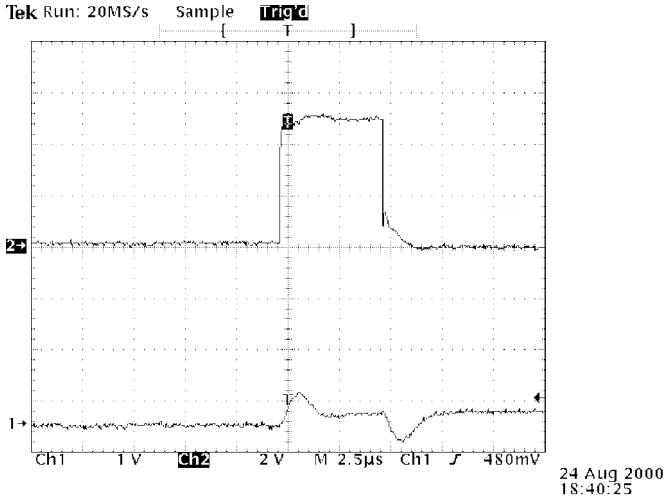
Diode non-conducting direction



Diode conducting direction



Shorted load



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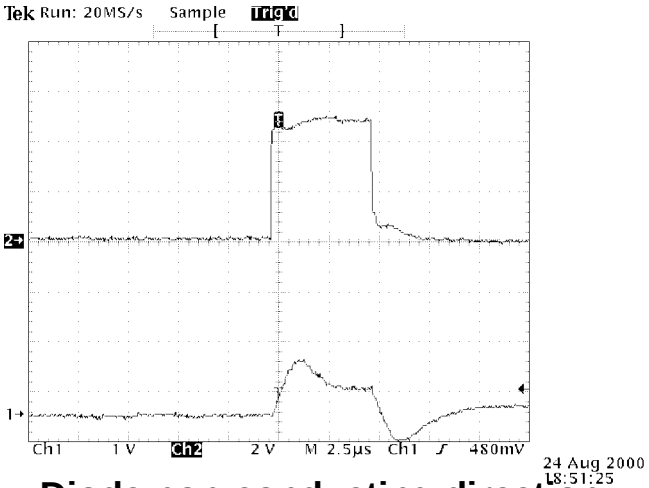
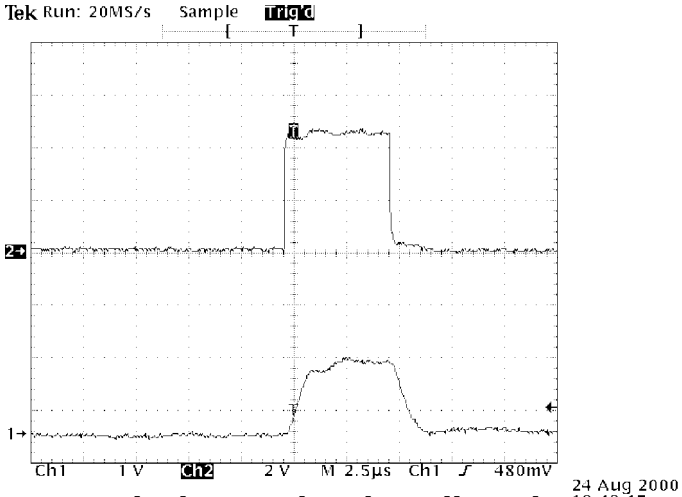
Single Transformer Circuit - Measurements

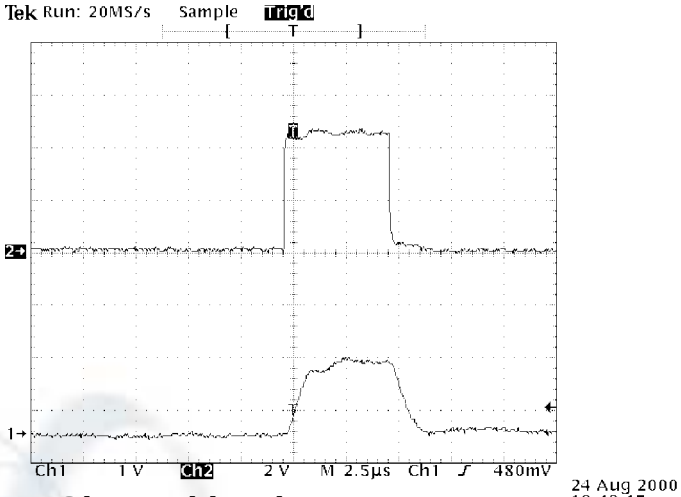
Setup: Mid-Span,100m Cat 5 FTP cable



Diode non-conducting direction



Diode conducting direction



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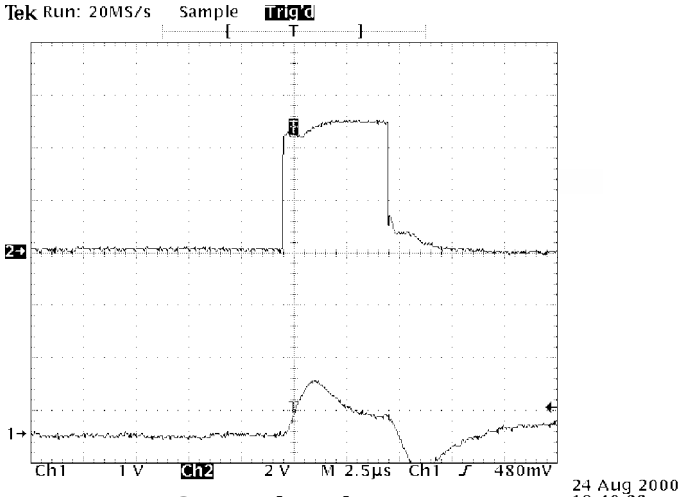

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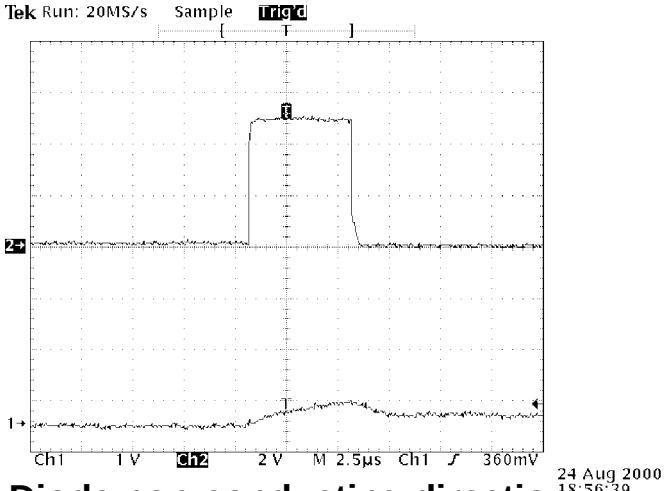
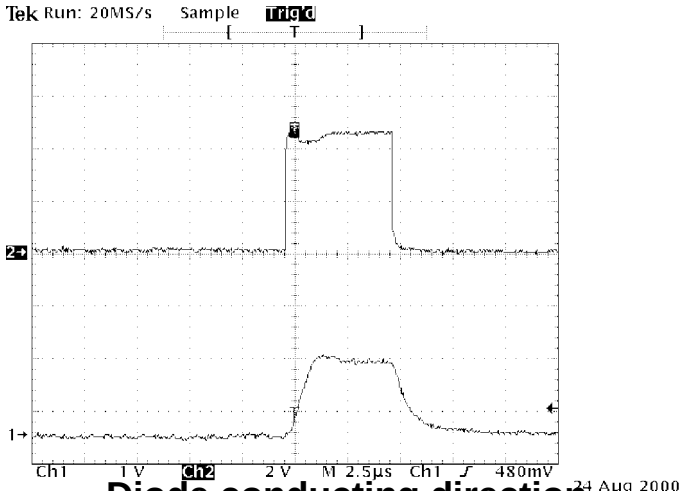
Single Transformer Circuit - Measurements

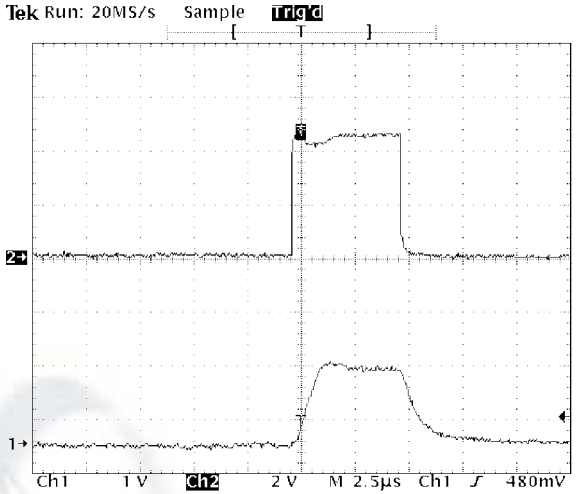
Setup: Mid-Span, 20cm Cat 5 UTP cable



Diode non-conducting direction



Diode conducting direction



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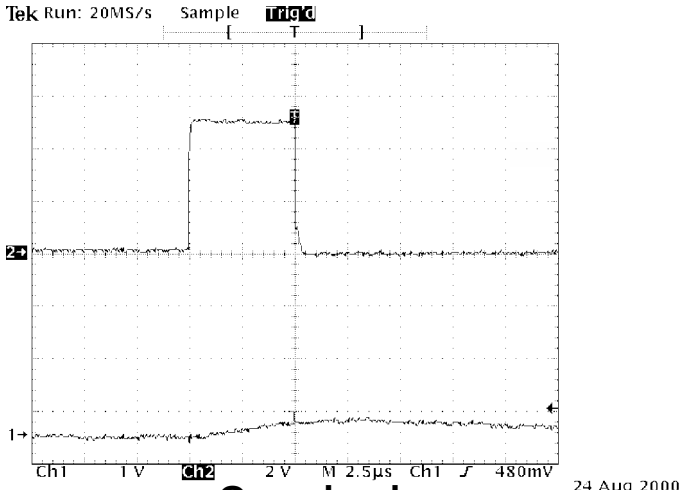

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Single Transformer Circuit - Conclusions

- Utilizing a single coupling transformer is feasible
- Similar results were observed for both A and B setup

Comparison Between Single / Double Transformers

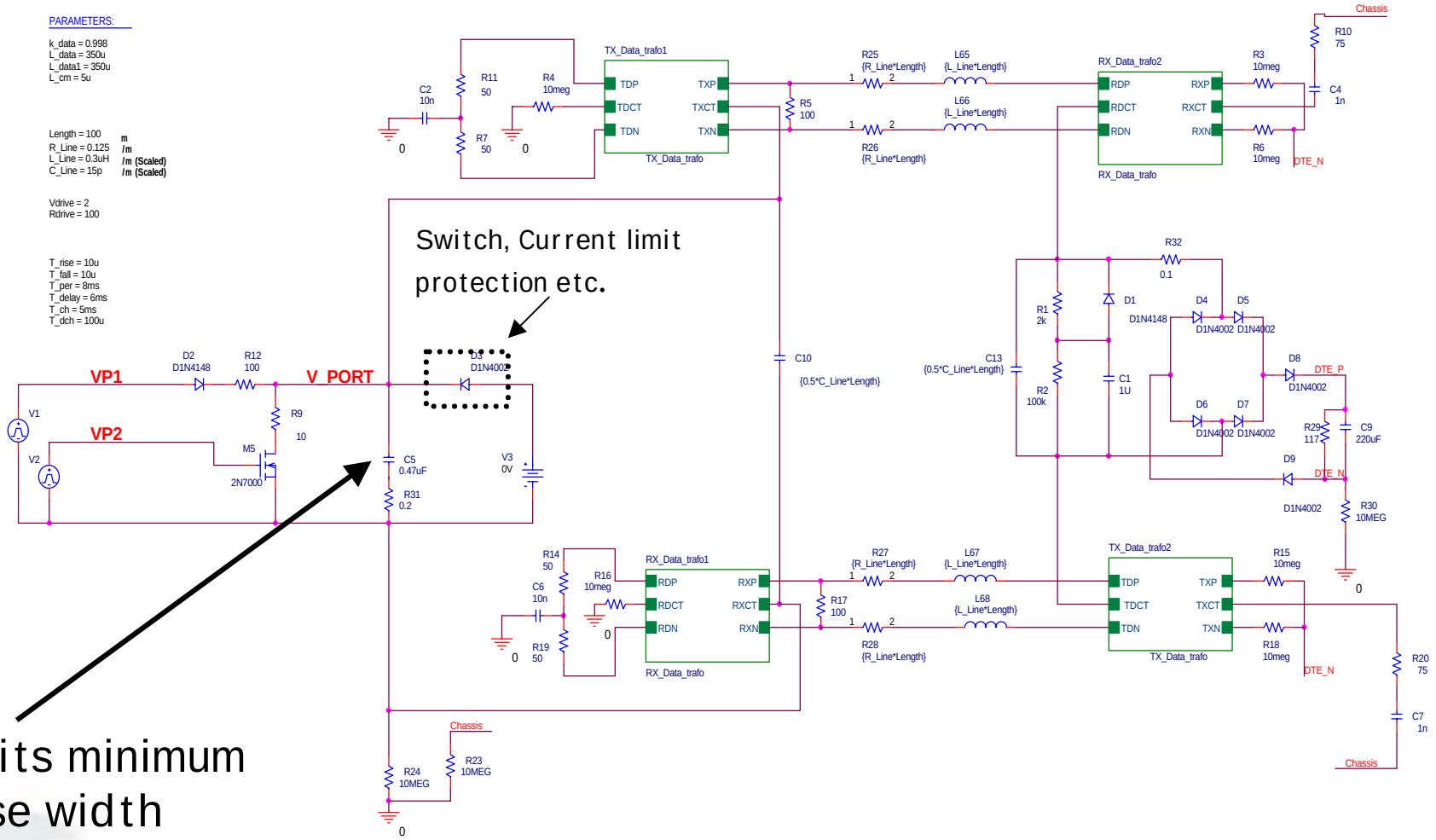
Parameter	Probing signal sensing method	
	Single Transformer	Double Transformer
Min. Primary inductance	4mH	1.350mH
Operating mode	Voltage pulse transformer	Voltage pulse transformer
Footprint	about 0.6X	1" x 0.5" = X
Cost	TBD	TBD

*Further investigation and testing should be performed to evaluate impact on cost and footprint

Coupled Diode Implementation Limitations

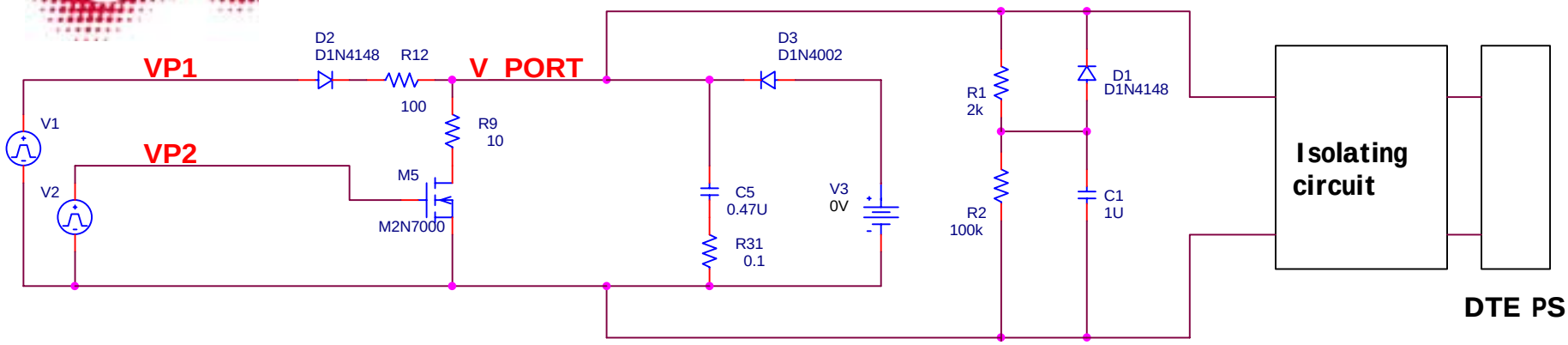
- Series voltage pulses feeding requires coupling transformers
- Implementing this scheme without using coupling transformers must utilize a different type of probing pulse feeding method
- Parallel voltage pulse feeding is required to allow future Silicon implementation

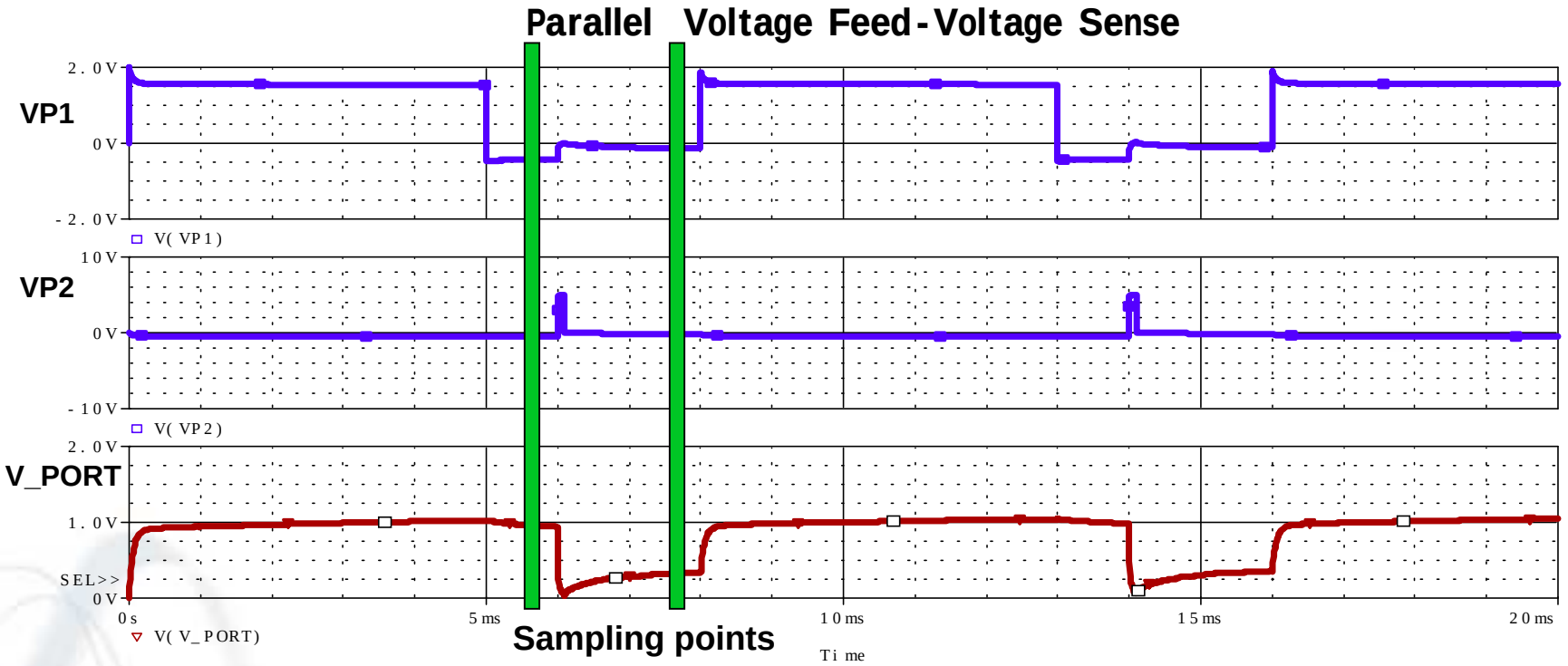
Transformer-less Implementation



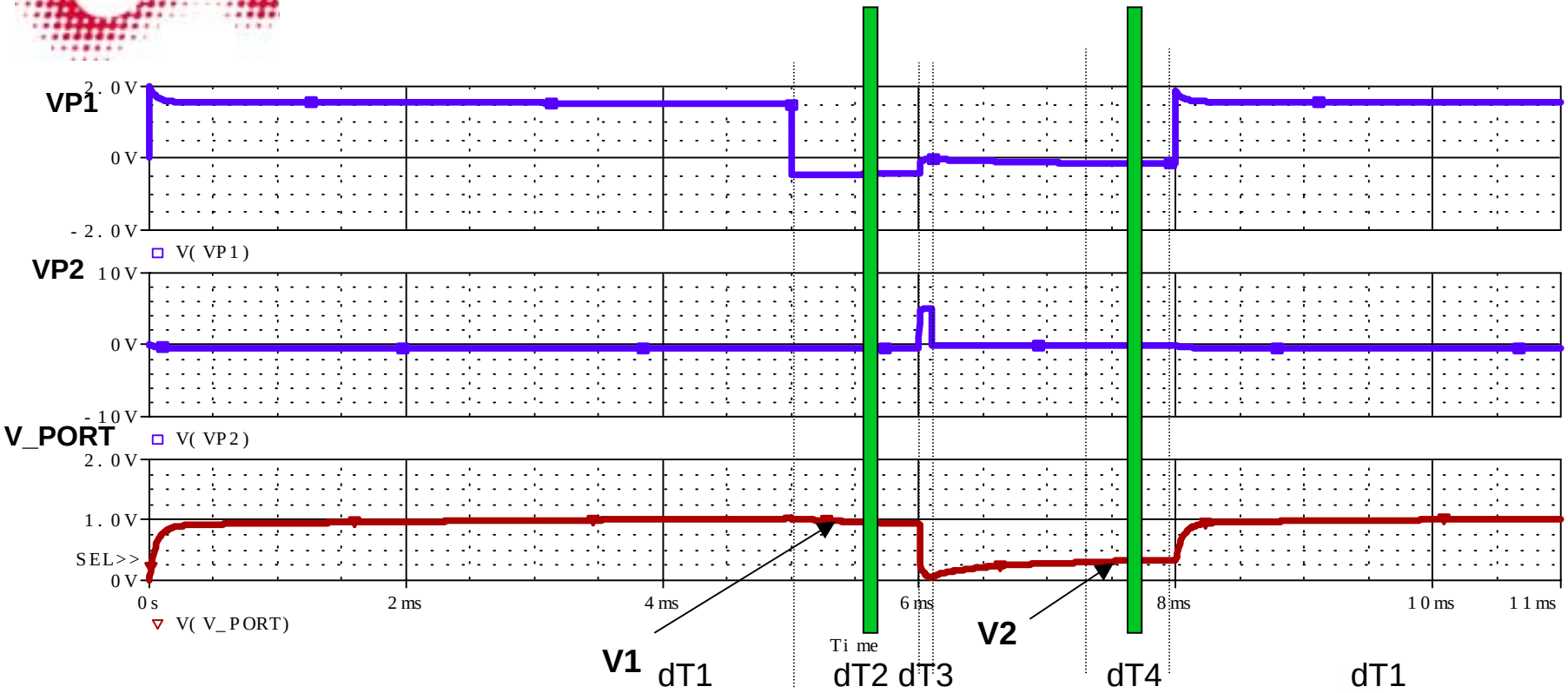
Limits minimum pulse width

Simplified Transformer-less Implementation Model





Transformer-less Implementation - Waveforms



dT1: Diode is at non-conduction direction, Cap is charged to V1.

dT2: Port output pulse voltage peak is sensed for V1±TBD% within dT2 gape.

dT3: Diode is in conducting direction, by shorting the port for limited time dT3.

dT4: Port output pulse voltage valley is sensed for V2=0.7V ±TBD% within dT4 gape.

- All other digital pulse manipulation and processing apply to this concept as well and are conceptually similar to Series Feed solutions (with the transformers…)

Transformer-less solution - Concept Principles

- Parallel probing signal feeding method
- AC coupled diode elements are detected by two pulse sources with different characteristics.
- Detected signal is unique function of coupled diode elements values.
- Immunity to ambiguous detection is ensured by pseudo randomly changing pulse width on both pulse sources.
  - In addition to behavioral signature detection, higher level of detection reliability can be achieved by utilizing the forward and reversed AC coupled diode time constant network.

Comparison between probing signal Implementation methods

Parameters-DTE side	Single Transformer	Double Transformer	With Out Transformer
Coupled diode elements	No Change	No Change	No Change
Coupled diode elements values	No Change	No Change	No Change
Parameters-PSE side			
Pulse amplitude	No Change	No Change	No Change
Pulse width	5uS	5uS	5uS to 5mS
Pulse Frequency	5Khz - 25Khz	5Khz - 25Khz	100Hz - 2KHz
Imunity to false detection	Digital Processing	Digital Processing	Digital Processing
Impact on EMI	No Change	No Change	Better
Pulse manipulation and processing concept	No Change	No Change	No Change
Imunity to ESD(See separate presentation)	No Change	No Change	No Change
Other Interface hardware(Data path)	No Change	No Change	No Change
Parameters-System			
PSE to DTE competability	No Change	No Change	No Change
Integration into Silicon	NA	NA	Possible
Cost Reduction	limited	limited	Possible
Footprint Reduction	limited	limited	Possible
Port to GND isolation achieved by	Coupling transformer	Coupling transformer	48V DC/DC conv.
Port to Port Isolation achieved by	Coupling transformer	Coupling transformer	48V DC/DC conv.
	& 48V DC/DC conv.	& 48V DC/DC conv.	

Implication on Detection Parameters Specifications

- Same coupled diode signature circuit is used in all probing signal feeding methods
- Proposed coupled diode and pulse parameters specifications should not limit implementation methods
- Transformers and silicon implementations will be feasible if a wider range of parameters be specified:
  - Frequency (5Khz to 25Khz and 100Hz to 2Khz)
  - Pulse width (5uS, 5uS to 5ms)
  - Pulse Amplitude TBD
  - Pulse average power (TBD mW max.)
  - Successful detection if TBDmin to 256max consecutive positive detection cycles where received.

What next?

- Additional investigation and testing are needed
  - Optimizing total detection time
  - Setting pulse width and duty cycle range as function of Coupled Diode element values.
  - Lab tests and further theoretical analysis to find if discovery process can be fooled.
  - With acknowledgments to Vladimir Portonov & Alon Ferenz for their help.

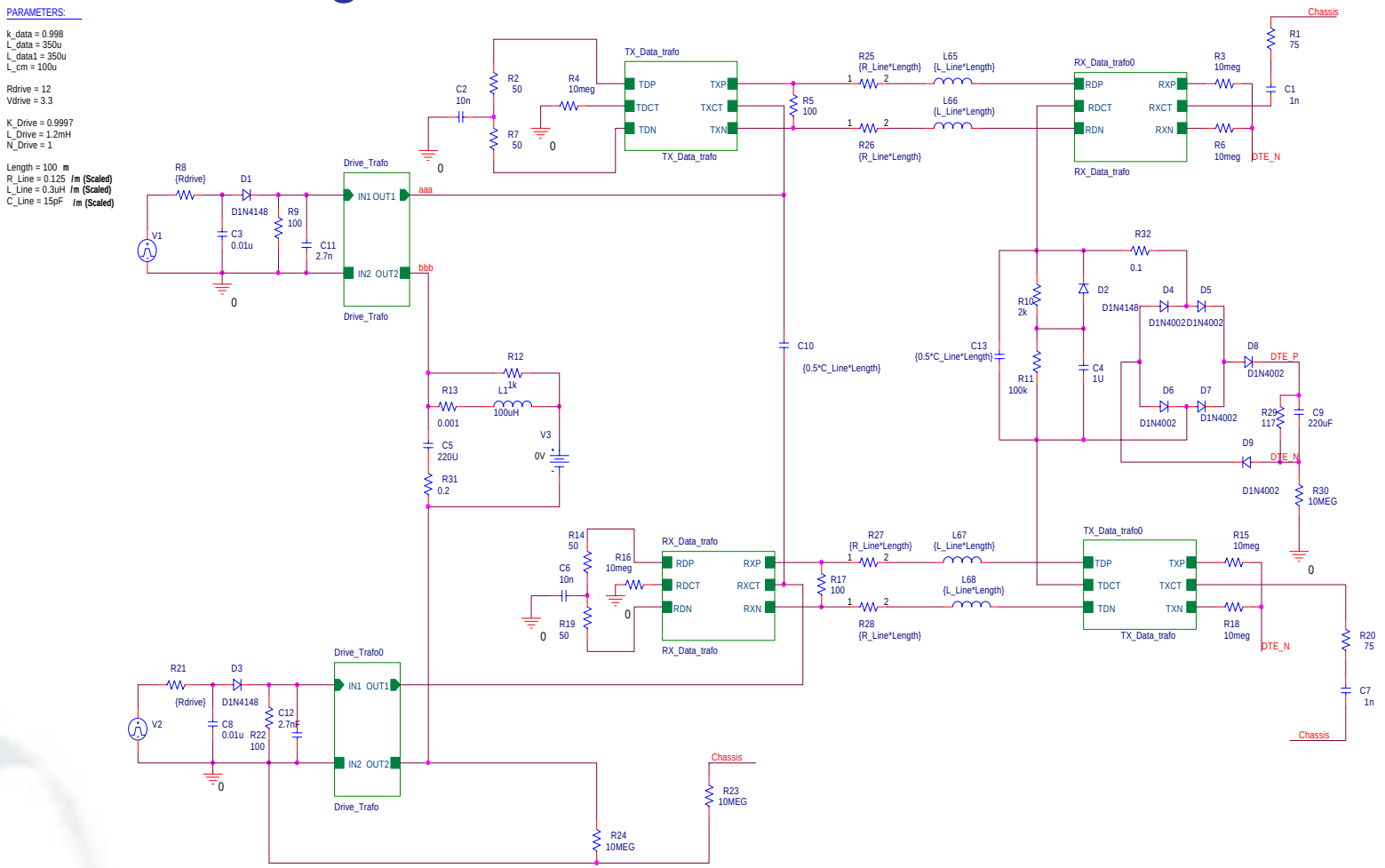
Annex A - Two Transformer solution
Requirements from coupling transformer

- **Im = Coupling transformer primary magnetizing current**
- **Isc = Coupling transformer secondary current during diode conduction mode.**
- **Zt = Total series impedance off whole link during diode conduction mode. Zt = 40-80Ohm**
- **Vt = Coupling transformer secondary peak voltage**
- **pw = Probing pulse width**
- **F = Probing pulse frequency**
- **Duty = pw*F**
- **Ls = series inductance caused by link inductance + common mode filter inductance located in the data transformer.**
- **Ls = 30-150uH**
- **Allowing 10% loss on detected pulse amplitude due to voltage drop on high impedance series elements.**
- **Lm/(Lm+Ls) = 0.9 => Lm>9Ls**
- **Idrive_avg = 0.5Im*Duty = 0.5*Duty*Vt*Duty/(F*Lm) = 0.5*Duty^2*Vt/(F*Lm)**
- **Lm>0.5*Duty^2*Vt/(Idrive_avg*F)**
- **Lm> max{9Ls , 0.5*Duty^2*Vt/(Idrive_avg*F) } =1.350mH**

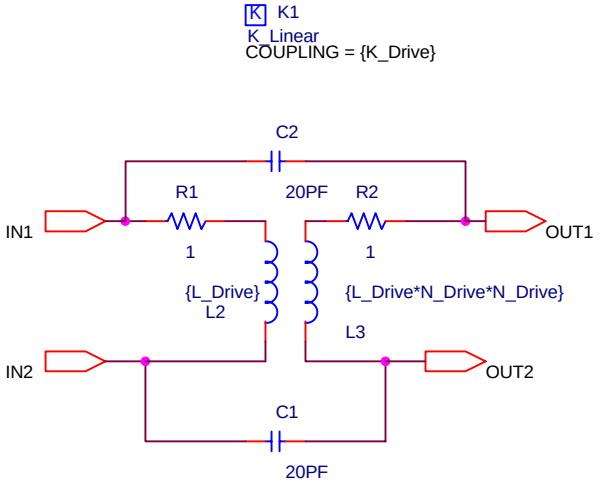
Annex B - Single Transformer solution Requirements From Coupling transformer

- Im = Coupling transformer primary magnetizing current
- Isc = Coupling transformer secondary current during diode conduction mode.
- Zt = Total series impedance off whole link during diode conduction mode. Zt = 40-80Ohm
- Vt = Coupling transformer secondary peak voltage
- pw = Probing pulse width
- F = Probing pulse frequency
- Duty = pw*F
- Ls = series inductance caused by link inductance + common mode filter inductance located in the data transformer
- For keeping detection resolution within safe margin: Im<Isc / 10
- Isc = Vt/Zt = 25mA - 50mA
- Lm>Vt/(Im/pw) = 2/(0.1*25mA/5uS)=4mH
- Lm>4mH

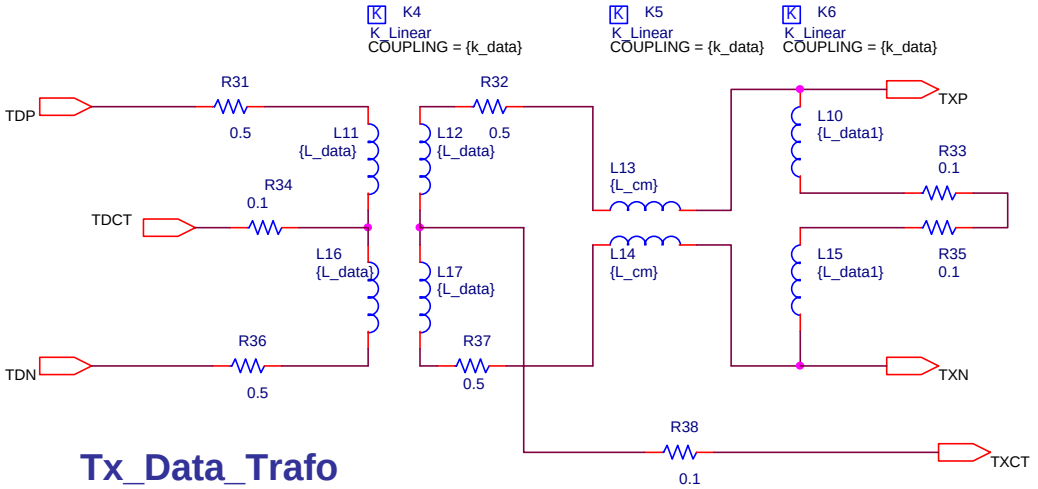
Annex C - Setup B Electrical Model for Circuit Elements During Detection Mode



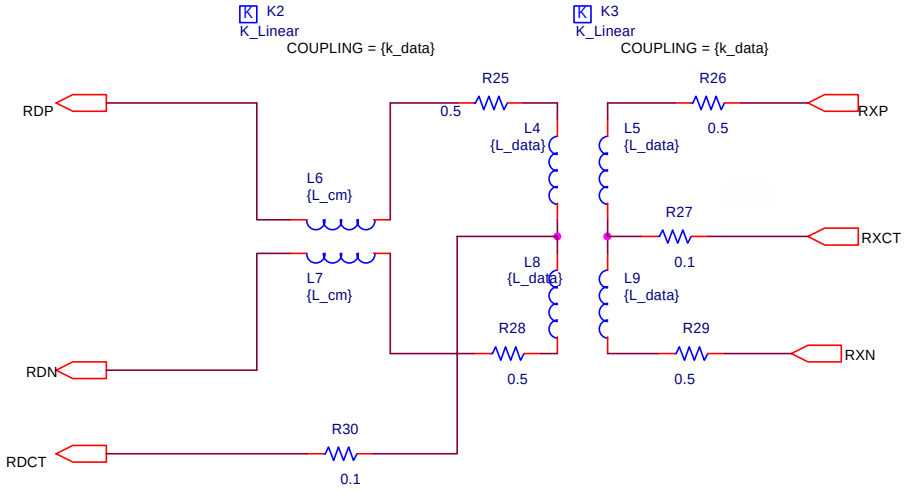
Annex C - Cont.



Drive_Trafo



Tx_Data_Trafo



Rx_Data_Trafo