"Resistive + Diodes" Signature and Detection

Protocol Summary and Overall Feasibility

IEEE 802.3af DTE Power via MDI Interim Meeting

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With Acknowledgements to:

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Jerry Bachand, John Ewalt

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  - Size
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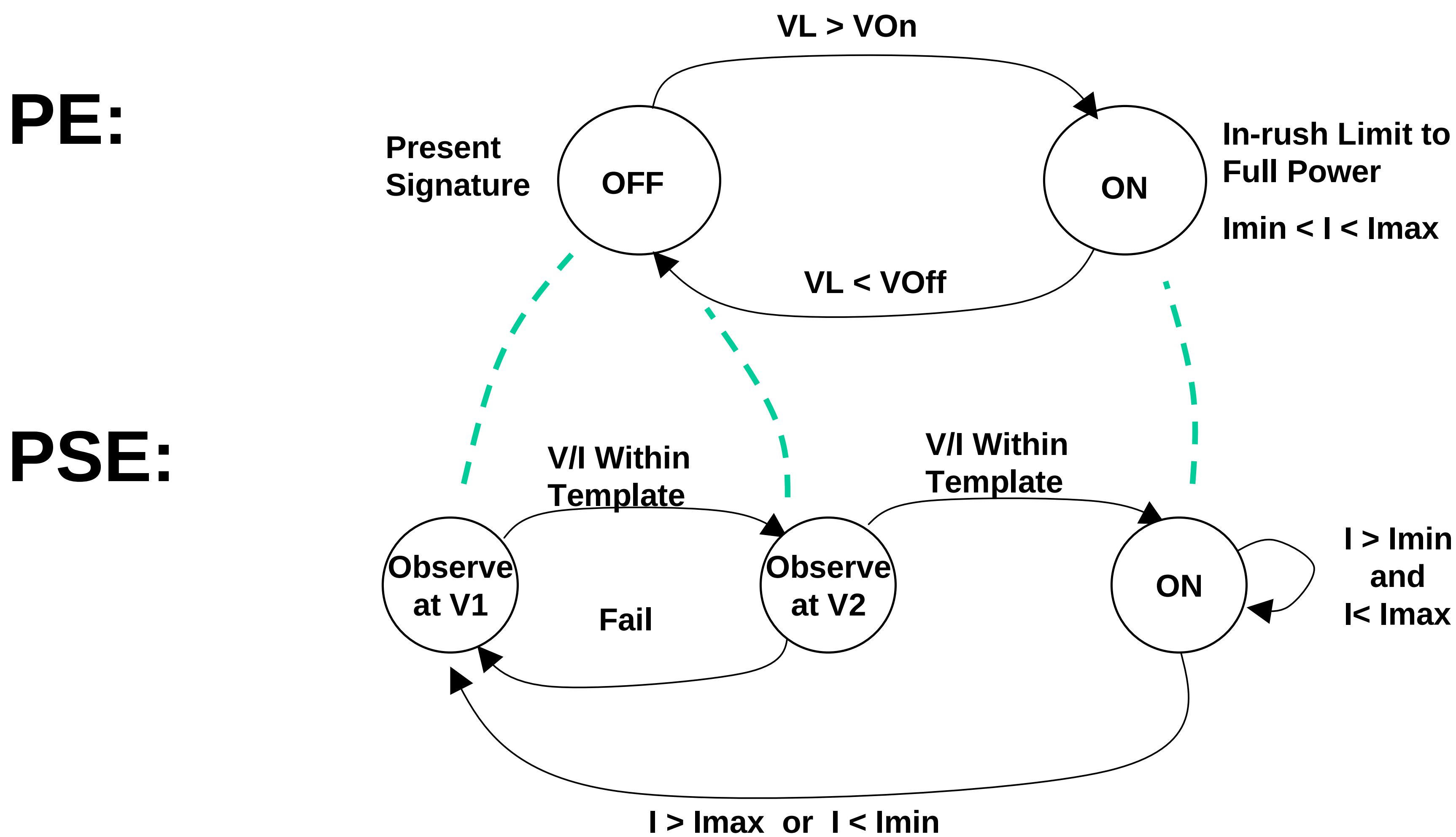
- Evaluation Prototypes
- Intellectual Property
- Summary

Detection and Signature Protocol Overview *(Updated)*

- At the Source:
  - OBSERVE DC current (high resistance) *at two voltages* for power-request signature from PE (multiple samples)
    - *Verifies expected linear characteristic over target range*
    - *Utilize a two diode voltage offset to discriminate against pure resistances*
  - APPLY full voltage (low resistance) after signature is detected.
  - REMOVE voltage when current becomes too high or too low.
- At the Load:
  - PRESENT power-request signature (high-resistance *and diodes)* while in off condition.
  - ACCEPT power at load resistance when full voltage is offered
  - CONTROL in-rush current
  - MAINTAIN appropriate current

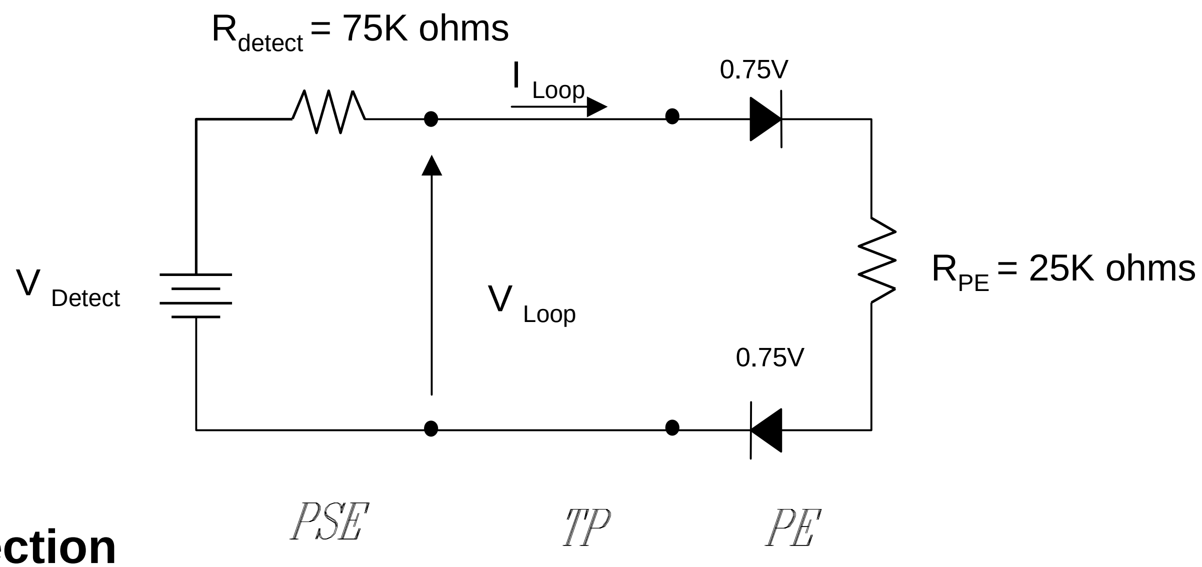
Protocol at DTE and Source



System Robustness

- Detection Margins, Hazard matrix
- Cable propagation
- Cross-talk
- EMI
- ESD

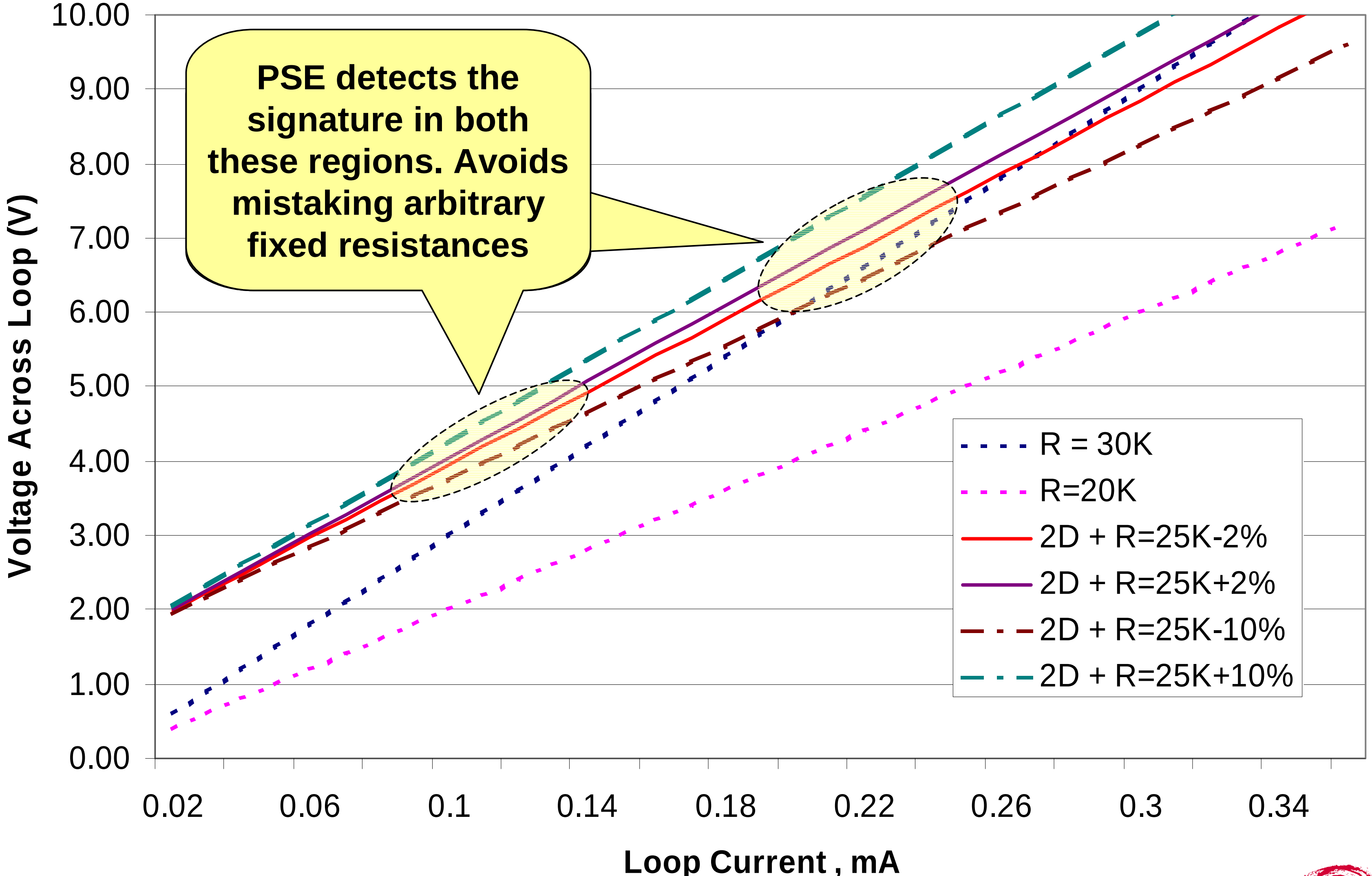
DC Detection Voltages



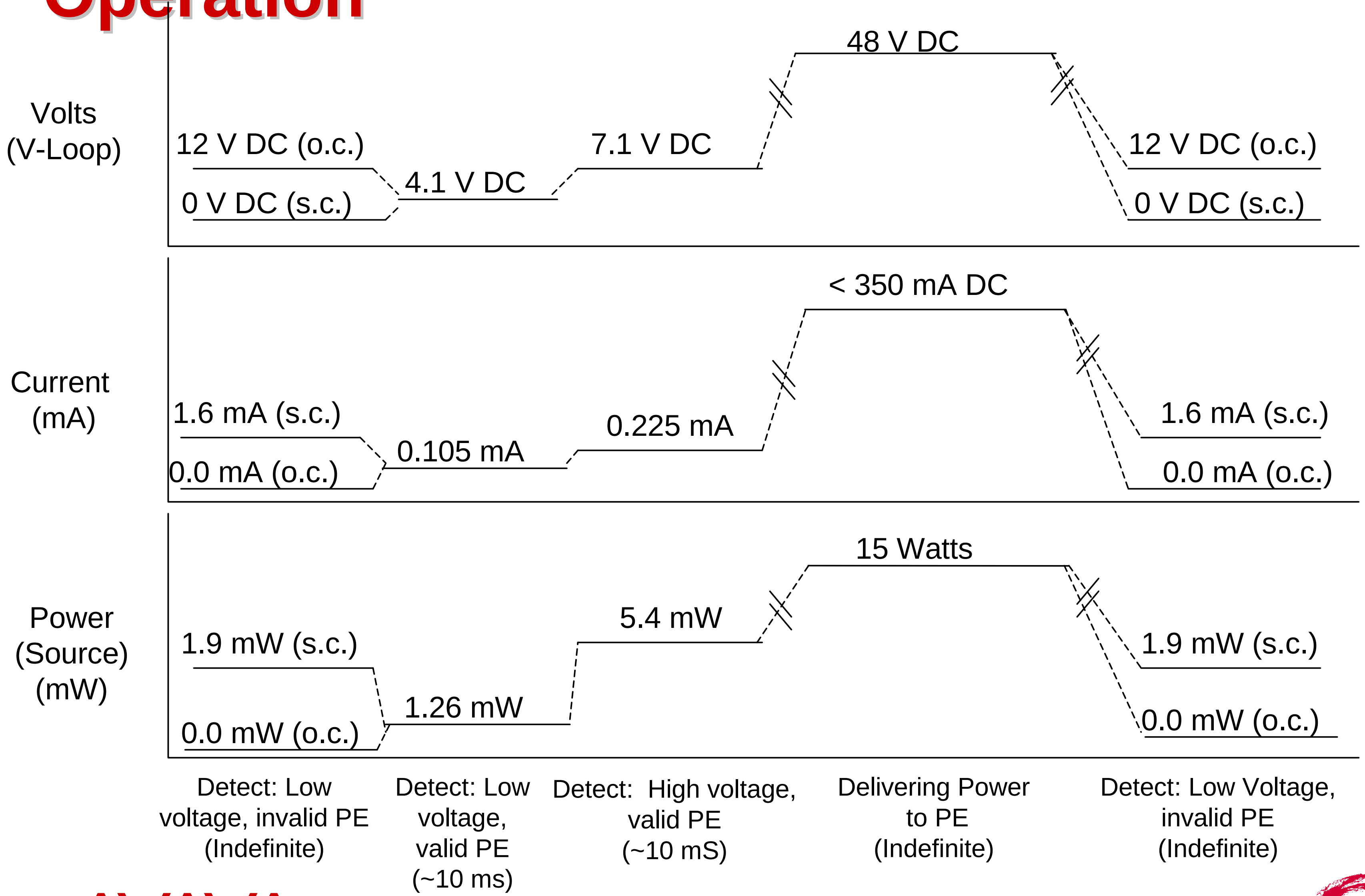
Use Two Detection Voltages

			Power (mW)	Power (mW)
V-Detect (V)	I-Loop (mA)	V-Loop(V)	Source	PE
24	0.225	7.125	5.40	1.60
12	0.105	4.125	1.26	0.43

Resistance Vs Resistance + Two Diodes V-I Curves



Voltages, Currents: Normal Operation



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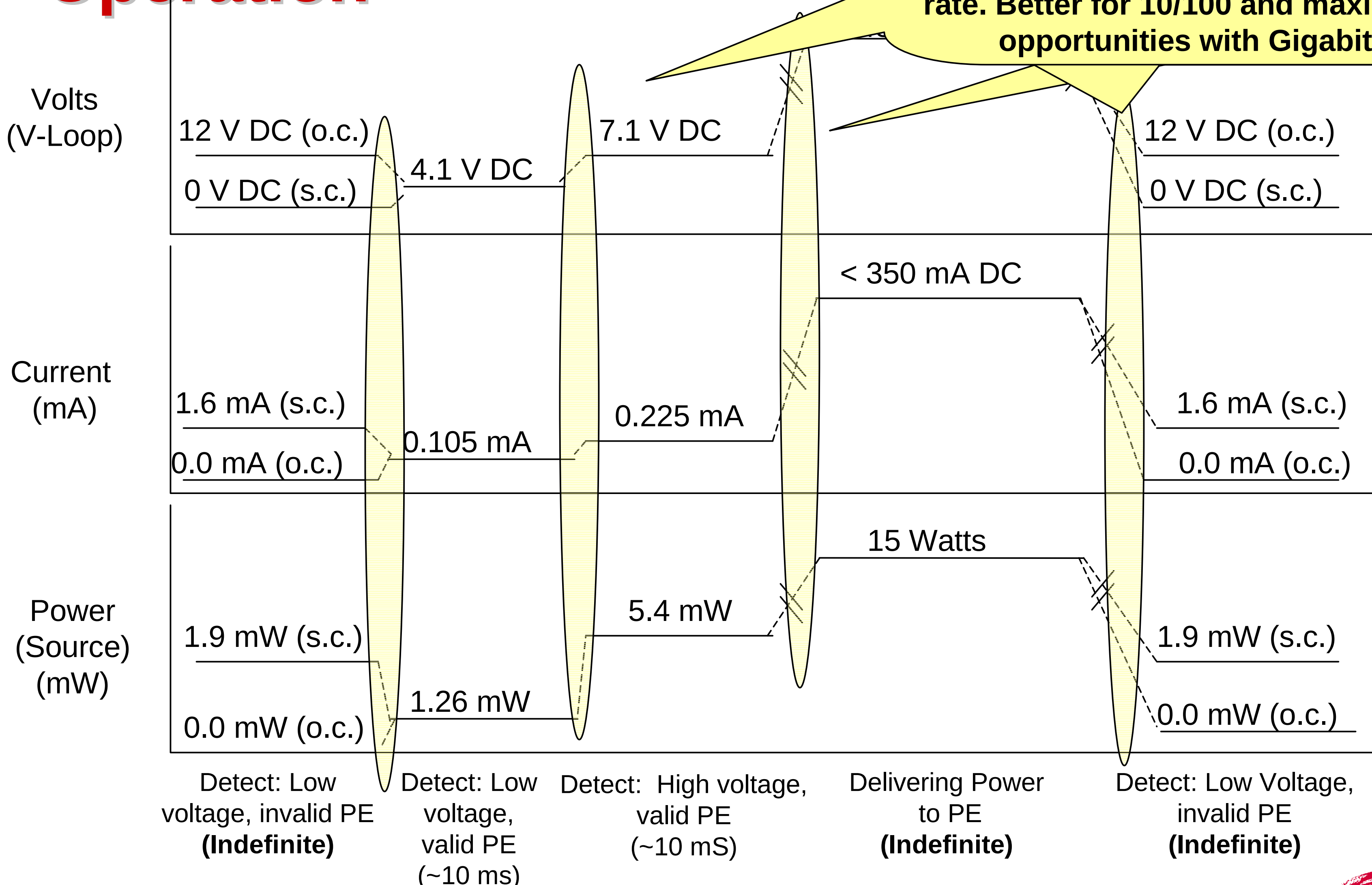
Voltages, Currents: Norma… Operation

Opportunity for Ethernet interference due to detection is *extremely infrequent*. And can control with slew rate. Better for 10/100 and maximizes opportunities with Gigabit.



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Hazard Matrix Experiment, Part I.

An approximate 24.2V power supply with a 75K Ohm Series Resistor was applied to wires 4,5 and 7,8 and the resulting voltage across the pairs was measured and recorded. This was also done for wires 1,2 and 3,6. The following Hazard Matrix Table shows how the resulting margins under a variety of conditions compare to the margins illustrated in the previous Signature Margin Table. Most equipment clustered around the expected "Open" or "Short" circuit regions as expected.

Hazard Matrix, Part I.

Condition: Make and Model	Status	1,2,3,6 Voltage (V)	4,5,7,8 Voltage (V)
Open Circuit:		24.200	24.200
Loop Back:		24.2 or 0.05	24.2 or 0.05
Full Short:		0.015	0.015
Partial Short:		0 or 24.2	0 or 24.2
Legacy:			
Compaq Netelligent 1108, 100BASE-TX Class II Repeater	ON	0.049	0.033
	OFF	0.049	0.033
Intel Express 510T Switch	ON	24.210	0.049
	OFF	24.180	0.049
Cisco Systems Fasthub 100 Series	ON	24.210	24.210
	OFF	24.180	24.180
3Com Superstack II Baseline 10/100 Switch	ON	24.180	0.049
	OFF	24.190	0.049
3Com Superstack II Switch 3300	ON	24.200	0.049
	OFF	24.190	0.049
3Com Fast Etherlink XL 10/100 Nic Card	ON	0.025	0.049
3Com Etherlink III PCMCIA 10BASE-T	OFF	0.049	0.048
Intel 8255x PCI 10/100 Ethernet Adapter	ON	0.049	0.049
3Com Etherlink III Bus-Master PCI Ethernet Adapter	ON	24.200	24.200
HP LaserJet 4MV Printer	ON	24.200	24.200
HP Ethernet Family Adapter with LAN Remote Power	ON	0.049	0.049
HP Color LaserJet 4500 DN	ON	0.049	0.050
Cisco Catalyst 3500 Series XL	ON	0.033	24.190
	OFF	0.033	24.190
Dana Minihub-8	ON	24.200	24.200

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Hazard Matrix, Part I.

Condition: Make and Model	Status	1,2,3,6 Voltage (V)	4,5,7,8 Voltage (V)
Legacy (Cont.):			
Ericsson Touchwave Webswitch 1608	ON	24.200	24.200
Cisco Access Digital Gateway Selsius	ON	24.200	24.200
Cisco 3620 Router	ON	24.200	24.200
Cisco 3620 Router "Con" Port	ON	24.200	24.200
Cisco 3620 Router "Aux" Port	ON	24.200	24.200
Cisco Access Analog Station Gateway	ON	24.200	24.200
	OFF	24.200	24.200
3Com NBX 100, 10BASE-T Uplink	ON	24.200	24.200
3Com NBX 100, Base 100 Ethernet Port	ON	24.200	24.200
AT&T Fax Machine 3510D Data Port	ON	24.200	24.200
	OFF	24.200	24.200
Cisco Access Analog Trunk Gateway (Ethernet)	ON	24.200	24.200
	OFF	24.200	24.200
Network Alchemy Ethernet HUB Card Data Port	ON	24.200	0.049
Network Alchemy Ethernet HUB Card Expansion Port	ON	1.790	24.200
Nortel Norstar Application Module	ON	0.049	0.049
3Com Office Connect Ethernet HUB 8C	ON	24.200	24.200
Canary 6 Port 100BASE-T4 Hub	ON	24.180	24.180
	OFF	24.190	24.190
HP Advancestack J2410A, 100VG	ON	24.190	24.190
*-Transceiver Slot	OFF	24.190	24.190
HP Advancestack J2410A, 100VG	ON	24.190	22.510
*-Extension Slot	OFF	24.190	24.190
Cisco Catalyst 6500	ON	24.1946	0.089
	OFF	24.2	0.04919
Lucent Cajun P120 Switch	ON	24.19	0.049
	OFF	24.1982	0.049
Lucent IP exch Adapter/8	ON	24.202	24.201
	OFF	24.203	24.2
Lucent/Ascend Superpipe 155	ON	0.0487	0.0487
	OFF	0.0487	0.0487

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Hazard Matrix, Part 1.

Condition: Make and Model	Status	1,2,3,6 Voltage (V)	4,5,7,8 Voltage (V)
Legacy (Cont.):			
3Com SuperStack 2 (Baseline Switch)	ON	24.202	24.202
	OFF	24.202	24.203
Cisco 2600 Router	ON	24.202	24.202
	OFF	24.202	24.203
Cisco 3600 Router	ON	0.0489	0.0498
	OFF	0.0489	0.0498
Lucent Tel Connect 8	ON	0.0489	0.0488
	OFF	0.0489	0.048
Lucent Cajun P333 Switch	ON	24.199	0.0343
	OFF	24.2	0.0343
Neo-Legacy:			
Cisco Catalyst 3500 Series XL with in-line power	ON	24.180	24.180
	OFF	24.180	24.180
3Com NBX 100 IP Phone	ON	24.200	24.200
*-Data Port	OFF	24.200	24.200
3Com NBX 100 IP Phone	ON	24.200	24.200
*-Voice Port	OFF	24.200	24.200
3Com NBX Analog Adapter	ON	24.200	24.200
*-Data Port	OFF	24.200	24.200
3Com NBX Analog Adapter	ON	24.200	24.200
*-Voice Port	OFF	24.200	24.200
3Com NBX 100 DSS/BLF Adjunct	ON	24.200	24.200
	OFF	24.200	24.200
Cisco 30 UIP IP Phone	ON	24.200	24.200
*-Data Port	OFF	24.200	24.200

Hazard Matrix, Part I.

Condition: Make and Model	Status	1,2,3,6 Voltage (V)	4,5,7,8 Voltage (V)
Neo-Legacy(Cont.):			
Cisco 30 UIP IP Phone	ON	24.200	24.200
*-Voice Port	OFF	24.200	24.200
Avaya IP Exchange Server	ON	0.020	0.020
Avaya IP Exchange Adapter LAN Port	ON	24.200	24.200
Avaya IP Exchange Adapter Voice Port	ON	24.200	24.200
Cisco 12 SPT IP Phone	ON	24.200	24.200
*-Data Port	OFF	24.200	24.200
Cisco 12 SPT IP Phone	ON	24.200	24.200
*-Voice Port	OFF	24.200	24.200
Power Device:	ON	-4to+4 or 21to28	-4to+4 or 21to28
	OFF	11 to 14	11 to 14
Crosstalk:		24.200	24.200
Random Plug:		0 to 24.2	0 to 24.2
Analog/Digital/PBX Telephone:			
Analog Phone Wall Jack	ON	24.200	-1.340
Lucent Merlin Legend ETR 18D	OFF	24.200	24.200
Lucent 8410D Phone (Holmdel)	OFF	9.420	24.200
Lucent MLX 20L Telephone	OFF	24.200	24.200
Lucnet MLX 16DP Telephone	OFF	24.200	24.200
Lucent Partner ETR 34D (Phone)	Line	24.202	24.202
	Aux	24.202	24.203
Lucent Partner ETR 18D (Phone)	Line	24.202	24.203
Lucent 8410D Digital Telephone	OFF	6.260	24.200

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Hazard Matrix, Part II.

A prototype module that replicates and automates the previous experiment was fabricated. With this, a second voltage measurement criteria was added to the algorithm that must *also* be satisfied in order for power to be applied. This 12V measurement, when coupled with the previous 24V measurement, ensures that purely resistive and highly non-linear loads will not match the signature. The 8410D phone, and a number of new units were tested and found not to promote power application.

Make/Model	Status	Power?
Lucent 8410D Phone	OFF	No
Lucent 4624	ON	No
IP phone	OFF	No
Cajun P220FE	ON	No
(Gigabit Switch)	OFF	No
Cabletron Systems	ON	No
Smart Switch 2200	OFF	No
Cisco 1600	ON	No
(Router)	OFF	No

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ESD Tests on Prototype

- A prototype was tested
- It survived all tests
- With no PE, the PSE survived 9kV from a Schaffner, NSG 435 ESD tester configured in contact discharge, 150pF, 330 Ohms, applied 10 times with and without power to the PSE, from pins 4,5 to 7,8 and reversed.
  - In the ON state, 9kV caused a latch up to occur
  - Unplugging the DTE and reconnecting restored service
- Code was verified to be correct after the tests
- 10kV of air discharge yielded similar results.

"Coupled Diode" Approach Concerns that "Resistive + Diodes" Does *Not* Have

1.) Transformer doesn't necessarily provide AC/ESD impulse isolation so this needs to be tested

2.) Strategy implies PHY redesign and consequential re-qualification on new generation devices with higher pincount to support the needed I/O

3.) Logic side power plane residence of detection implies EMI can leak from noisy logic to wire

4.) Approximately 1MHz bandwidth signature pulse signaling precludes aggressive filtering to limit noise emissions

5.) Conveyance of current use from supply to upper levels (to facilitate network power management) requires crossing the isolation barrier and additional monitoring circuits in the supply

6.) Longitudinal voltage characterization in terms of <1 volt sensitivity has not been done

7.) Parallel devices may get destroyed at application of higher power

8.) Use of constant signaling and reliance on transformer saturation to detect undercurrent is very coarse. >10mA signature pulses imply a >0.5W maintenance consumption

9.) 25 pair bundle interference with asynchronous units?

10.) Pulse shaping implies expensive immediate implementation

11.) 1uF >54V signature cap in PE is big and expensive

12.) Extra two diode drops Required in PE lowers maximum power delivered to PE load

Conclusions

- In a random sampling of a number of Devices and Hazard Matrix test conditions, Power was never applied inappropriately using the Proposed Protocol
- A prototype survived ESD tests, including passing ***10kV*** air discharge and ***9kV*** contact discharge. (Damage never was observed.)
- Prototype measured to operate at a range of ***1200 meters.*** (Ran out of wire.)

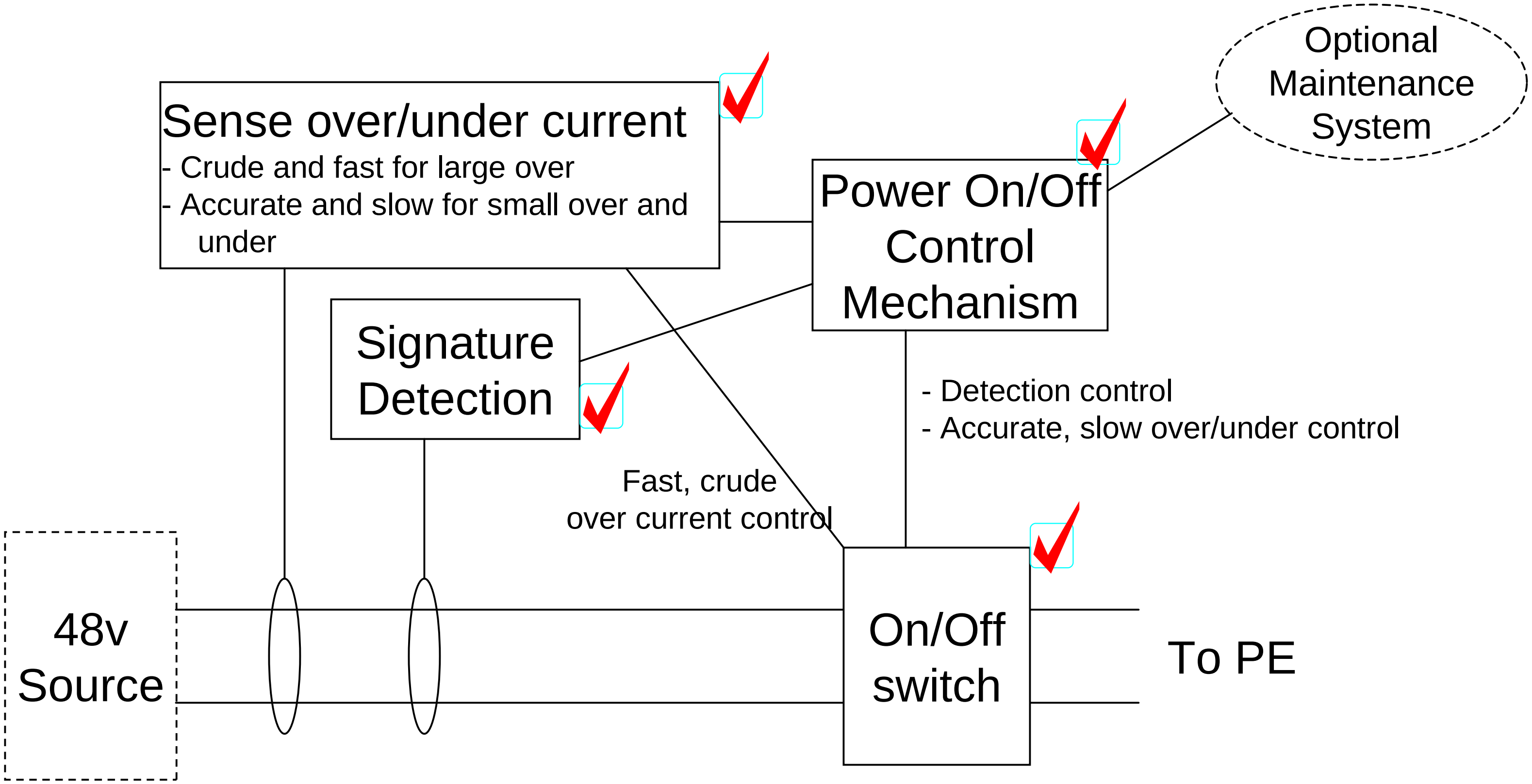
System Costs

- Prototype Schematics
- Prototype Bill of Materials
- Cost Extrapolation
- Space
- Suitable Configurations

Disclaimer

- Schematics and costs provided are based on the single port prototype
- The single port prototype represents a working, fully functional system, intended to demonstrate *feasibility* and *worst case* costs
- Any production version would likely be improved
- Production Environment A systems can achieve economies by sharing components
  - High level estimates are provided of potential costs but supporting schematics are not provided

Required Functionality for any PSE



✓ Included in single port prototype, Bill of Materials, Costs

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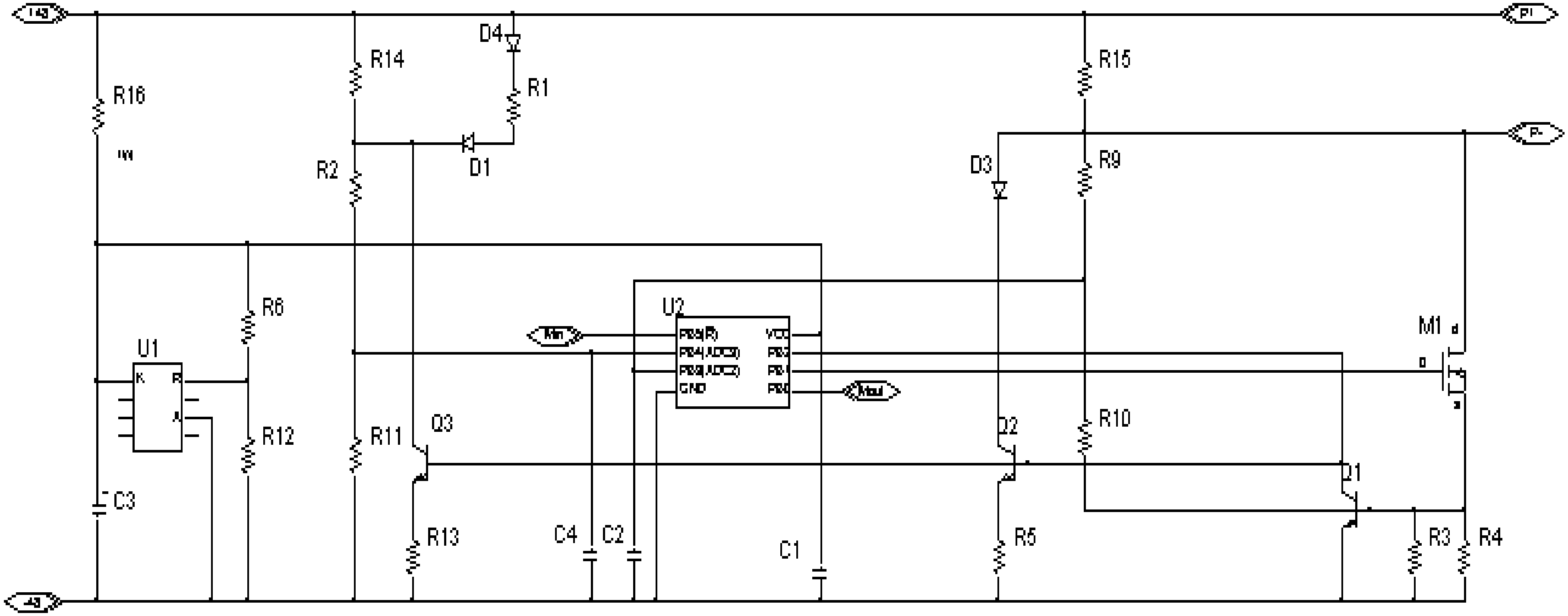
PSE - Detect and Power Control; Prototype Single Port "Power Controller"

Common ***Per Port***



5 Volt Supply	Reference Signature	Control	Signature Detect	Power Switch & Current Sense
$ 0.35	$0.10	$1.10	$0.09	$0.35

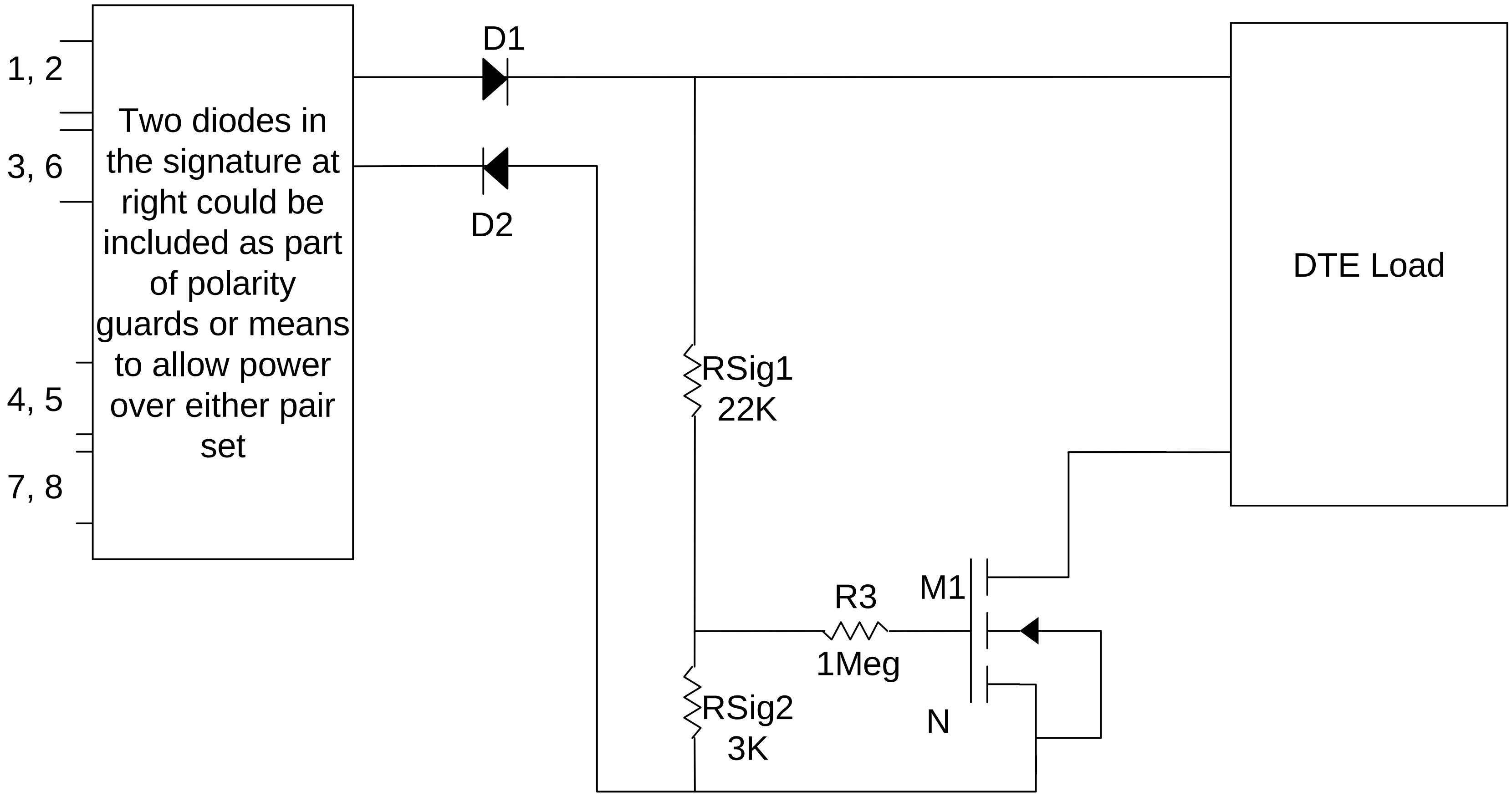
Bill of Materials - Prototype PSE “Power Controller”

Item	Count	Mfg ID	Attributes	RefDes
1	3	1N4002	DO-41	D1, D2, D3
2	1	ATtiny15L	ATtiny15L	U2
3	3	C	CK05, 100nF	C1, C2, C4
4	1	CV	CV, 22 uF	C3
5	3	MPSA06	TO-18	Q1, Q2, Q3
6	1	MTD3055EL	MTD3055EL	M1
7	2	R	RC05, 301K	R2, R9
8	1	R	RC05, 25K	R1
9	2	R	RC05, 2.05	R3, R4
10	2	R	RC05, 27.4K	R5, R13
11	4	R	RC05, 13.3K	R6, R10, R11, R12
12	1	R	RC05, 365	R7
13	1	R	RC05, 562	R8
14	2	R	RC05, 100K	R14, R15
15	1	R	RC05, 3.01K	R16
16	1	TL431	TL431	U1

PE - Signature and In-Rush Limiting

Signature:
25K ohm resistance
+ Two Diodes

- Isolation switch
- In-Rush current limiting
- Under current lock-out



Bill of Materials - PE Signature, In-Rush Limiting

Item	Count	Mfg ID	Attributes	RefDes
1	2	IN4002	DO-41	D1, D2
2	1	M1	MTD3055	M1
3	1	R	RC05, 3K	R2
4	1	R	RC05, 1Meg	R3
5	1	R	RC05, 22K	R1

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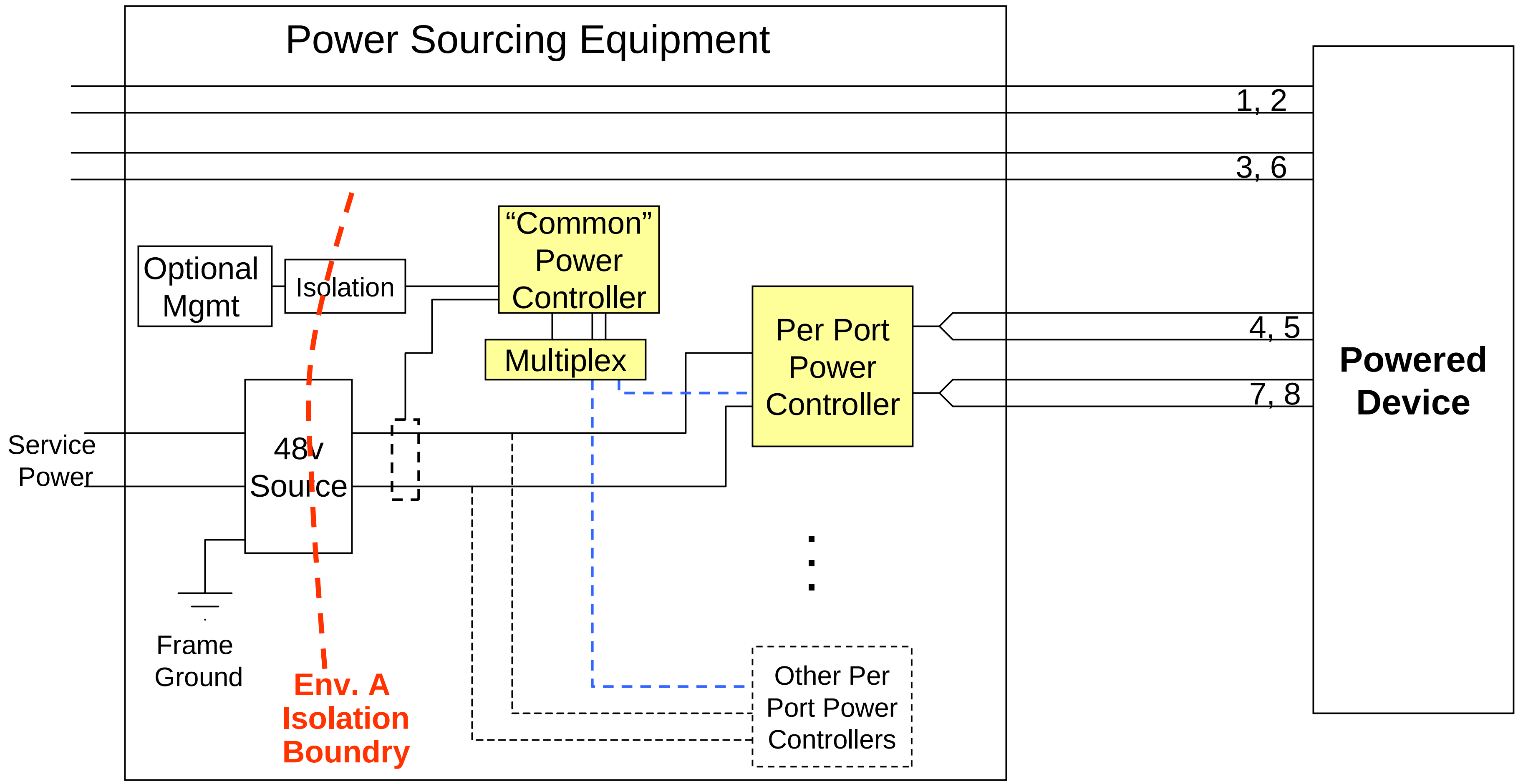
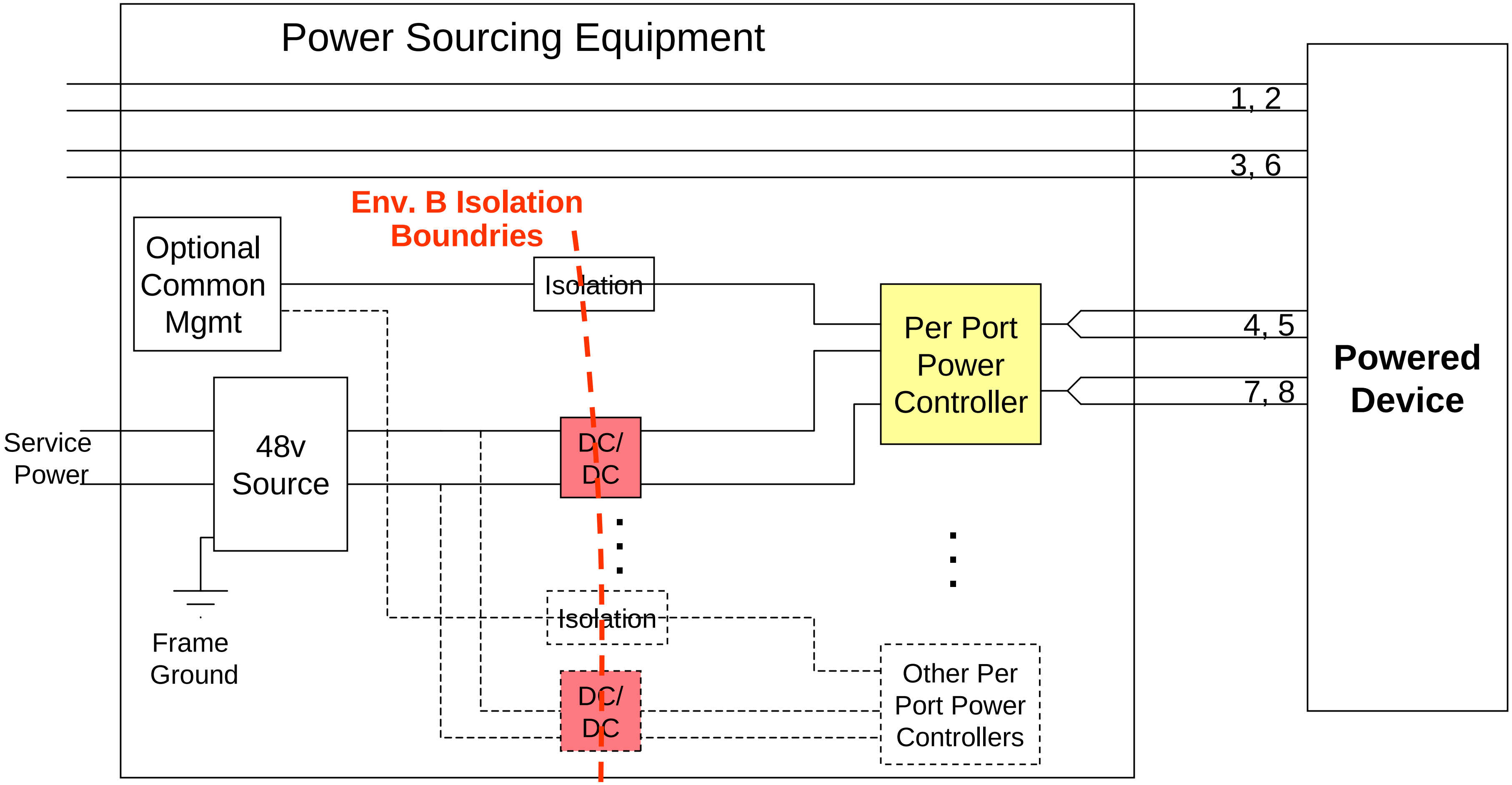
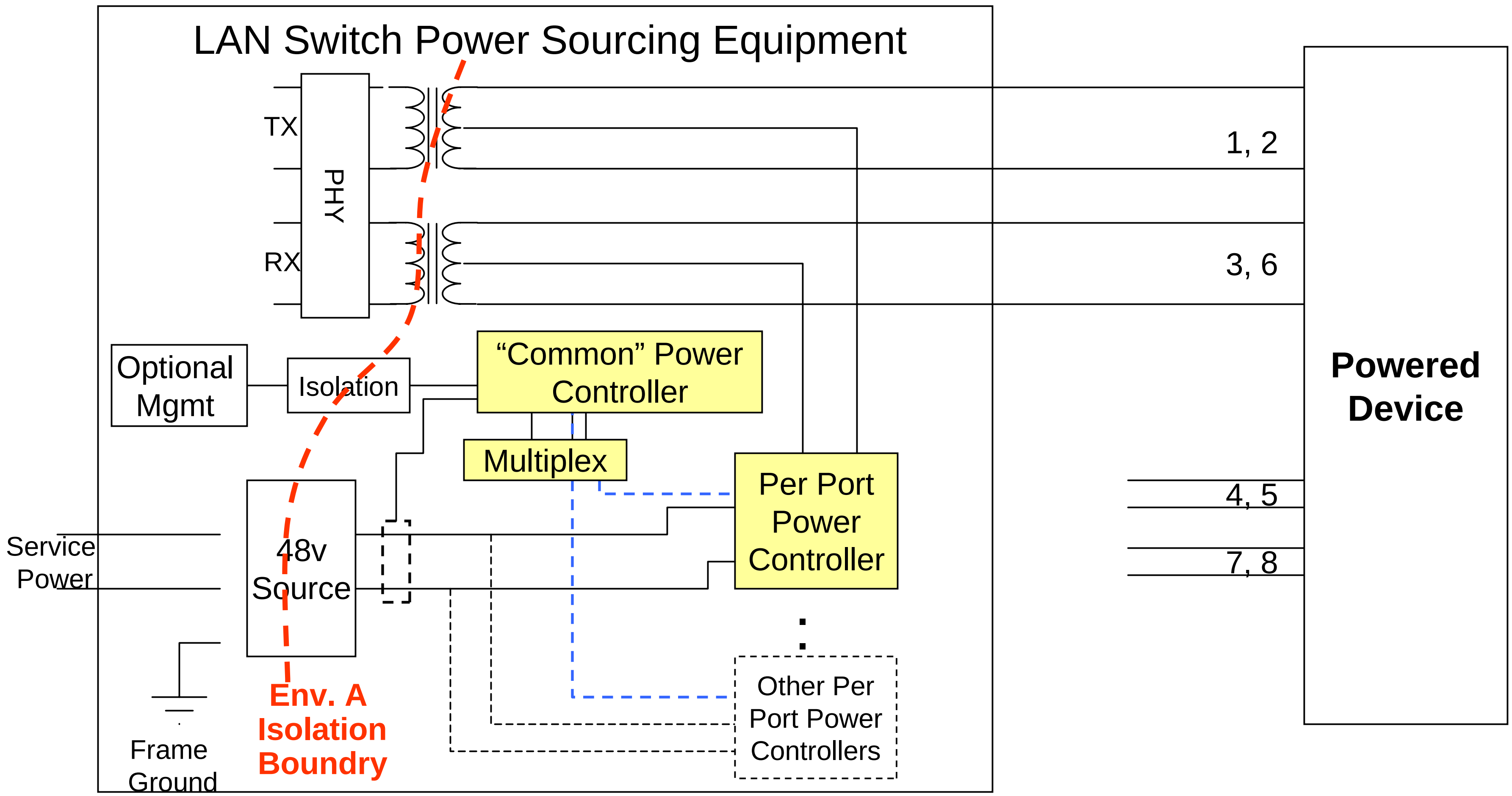
Mid-Span Configuration - Environment A



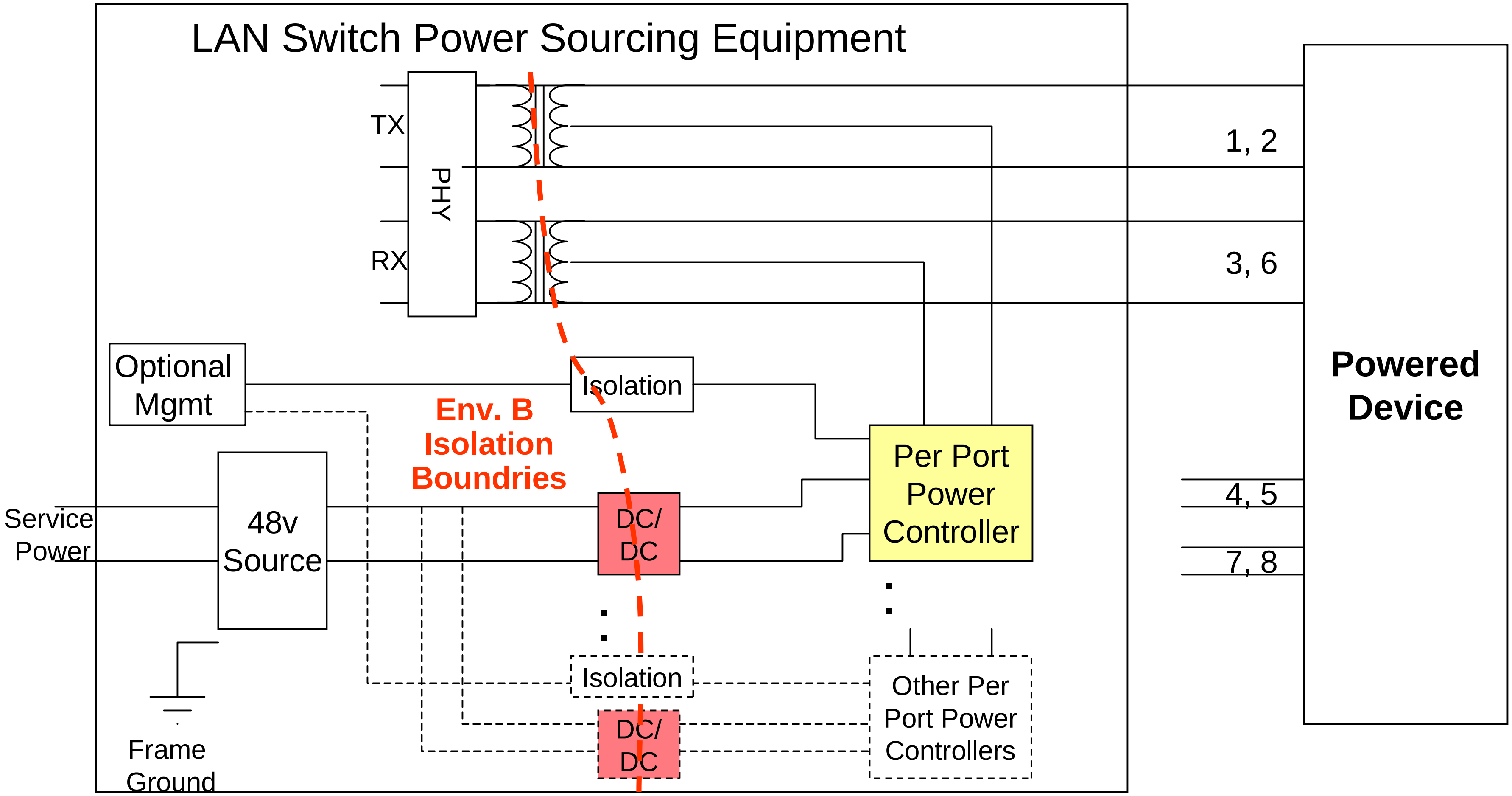
Mid-Span Configuration - Environment B



LAN Switch Configuration - Environment A (over signal pairs example)



LAN Switch Configuration - Environment B (over signal pairs example)



Cost Summary (Based on Bill of Materials Parts)

			Per Port Solution	Per Port Solution	Share over 8 ports	Share over 8 ports	Share over 24 ports	Share over24 ports
			Low Volume - 2000	***Est*** High Vol, Integration, 2001	Low Volume - 2000	***Est*** High Vol, Integration, 2001	Low Volume - 2000	***Est*** High Vol, Integration, 2001
Environment A								
	Per Port							
		Power Switch & Current Sense	0.35	0.25	0.35	0.25	0.35	0.25
		Signature Detect	0.09	0.07	0.09	0.07	0.09	0.07
	Common							
		Control	1.10	0.50	0.50	0.25	0.25	0.15
		Reference Signature	0.10	0.08	0.01	0.01	0.01	0.01
		5 volts supply	0.35	0.10	0.15	0.10	0.10	0.05
		Total (Per Port)	**1.99**	**1.00**	**1.10**	**0.68**	**0.80**	**0.53**
Environment B (additional)								
	Per Port Isolation							
		DC-DC converter	20.00	10.00	20.00	10.00	20.00	10.00
		Total (per port)	**21.99**	**11.00**	**21.99**	**11.00**	**21.99**	**11.00**
					No “sharing” advantage for Env B			
Optional Isolation for Mgmt Interface								
		Opto isolator-dual (per port)	0.60	0.50	0.60	0.50	0.60	0.50

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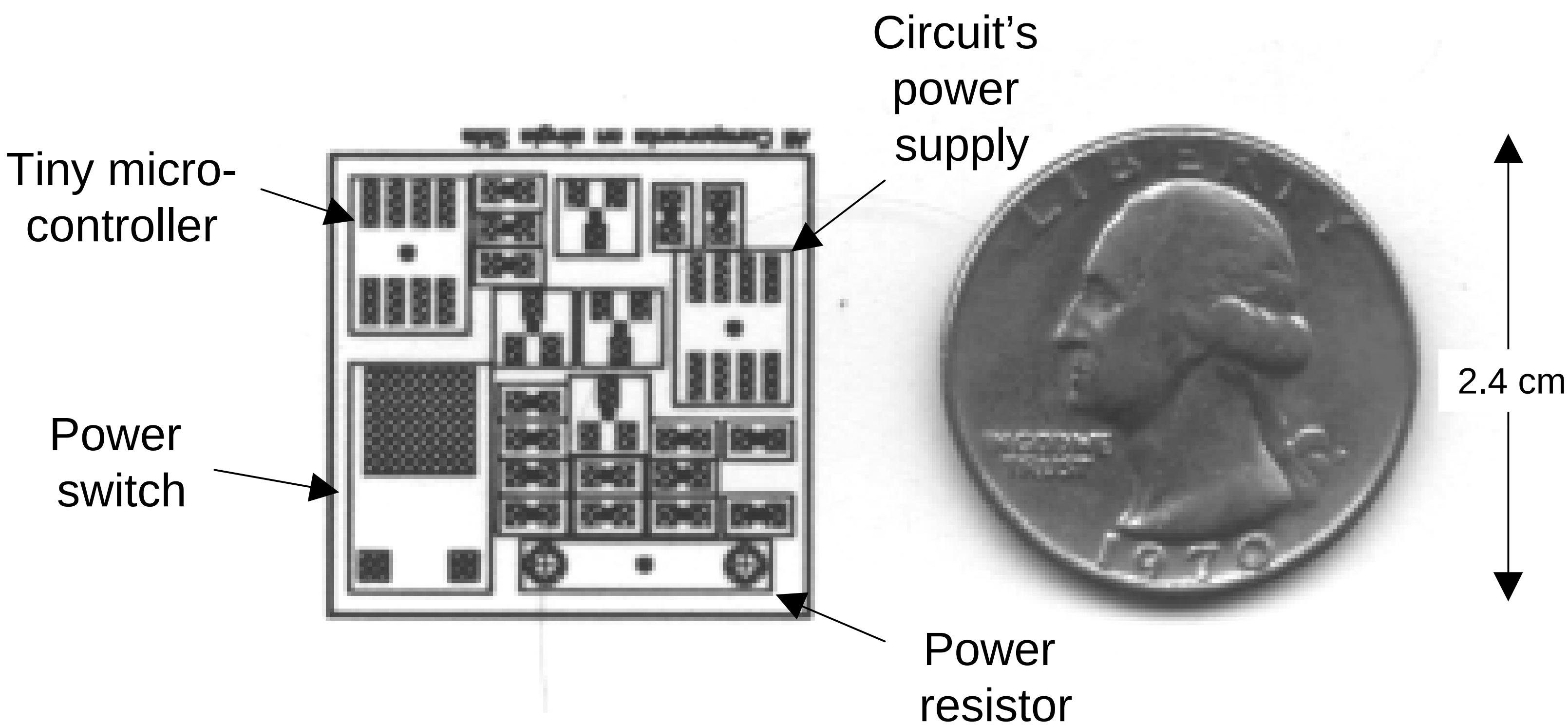
Layout of Detect and Power Control Circuit for PSE (Single Port)

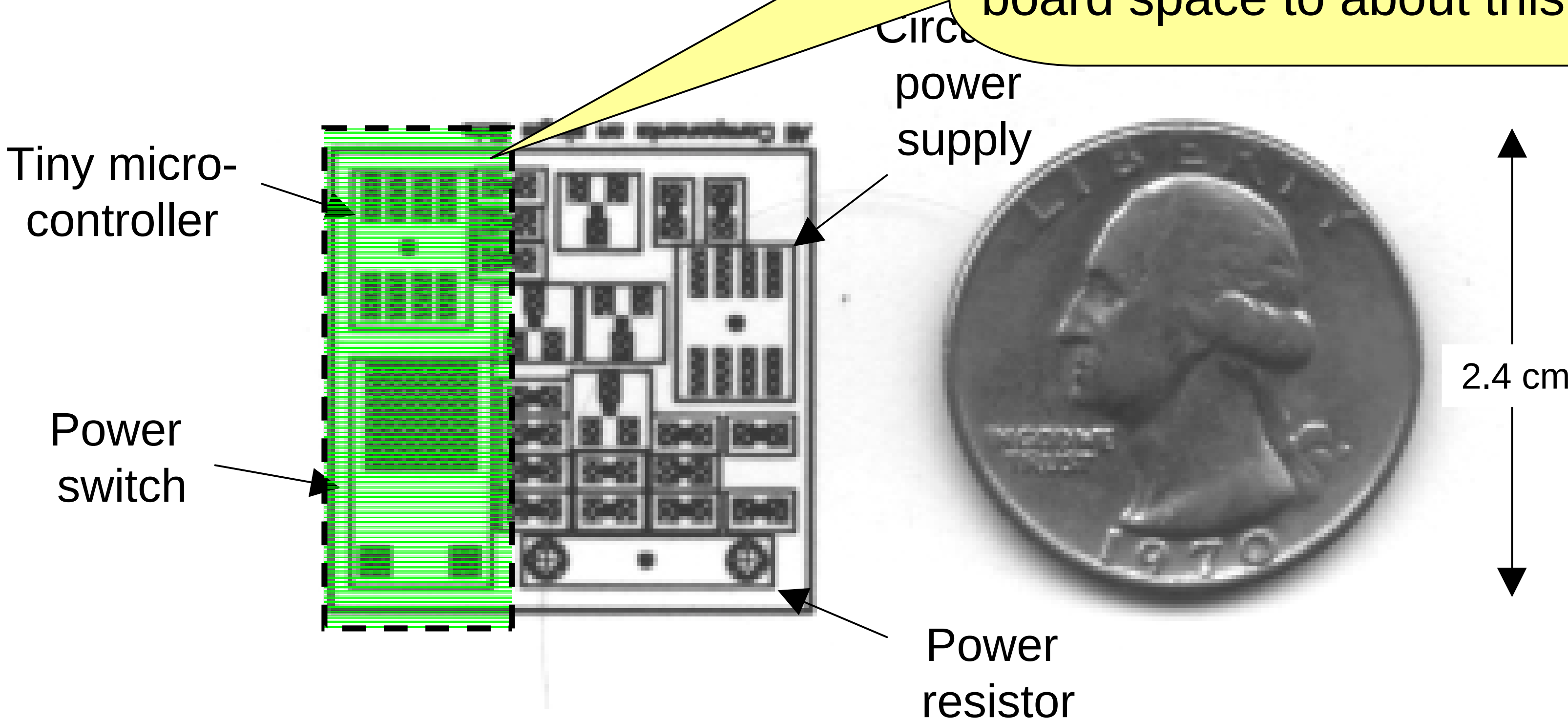
- Layout shown is for an individual port
- Space and cost can be further reduced by sharing over multiple ports
- Area can be reduced by placing resistors on back plus using a zener (sot23) instead of shunt regulator (so8)



Layout of Detect and Power Control Circuit for PSE (Single Port)

- Layout shown is for an individual port
- Space and cost can be further reduced by
- Area can be reduced by placing resistors o
  instead of shunt regulator (so8)

There is opportunity to integrate all but the MOSFET and a cap or two into a custom IC, reducing per port board space to about this area



Code for the Tiny Micro-Controller

```
 Title:          IPP15
;* Version:          1.0
;* Last updated:       00.09.05
;* Target:           ATtiny15l
;*
;* Written by         John Ewalt
;* Contact           jewalt@avaya.com
;*
.def   temp   =r16
.def   test1  =r17
.def   test2  =r18
.def   Tflag  =r19
.def   time2  =r20
.def   time1  =r21



;* Description:  This program controls the function of the IP phone power-
;*           supply.  It checks for a unique signature and then applies
;*           power to the IP phone.  Then it checks for over and under
;*           current conditions.  On an error, it resets.
;*
;******************************************************************************

.include "tn15def.inc"



.ORG    0x00
      rjmp   RESET         ;Reset Handle
      rjmp   ERROR         ;INT0 interrupt handler == It can only occur when there is an error
      NOP              ;Other interrupt handlers
      NOP
      NOP
      NOP
      NOP
      NOP
      NOP              ;ADC interrupt returns from where it was called!!

RESET:                ;this is the jump point for all Reset sources (POR,WDR,EXTR)
```

```
INIT:                    ;this is the init part of the program
      ldi    temp, 0x06
      out    DDRB, temp      ;sets PortB directions
      sbi    ACSR,ACD        ;disable comparator
      ldi    temp,0x00       ;set the pullup resistor on PI
      out    PORTB,temp
      ldi    temp,0x85       ;sets ADCSR   enables ADC, and sets ADC clock prescalar
      out    ADCSR,temp
      ldi    Tflag,0x04      ;Tflag [3..0] = flag for stable measurement
      rcall  DELAY
      rcall  MEAS
      sbi    PORTB,2         ;Set for high voltage test
      ldi    Tflag,0x04      ;Let MEAS routine overwrite REF
      rcall  DELAY
      rcall  MEAS
      cbi    DDRB,1          ;Set PB1 to an input to allow PULL-UP
      cbi    PORTB,1         ;enable PULL-UP resistor on PB1

EVERYTHINGON:
      ldi    temp,0x02       ;set INT0 to falling edge
      out    MCUCR,temp
      ldi    temp,0x40       ;set the INTF0 (interrupt 0 flag) to clear
      out    GIFR,temp
      ldi    temp,0x40       ;set INT0 enable
      out    GIMSK,temp
      ldi    Tflag,0x08      ;set Tflag
      sei               ;enable all unmasked interrupts
```

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Code for the Tiny Micro-Controller
(continued)

```
I_MEAS:
    rcall   DELAY
I_MEASi:
    ldi     temp,0x02       ;set to convert test voltage
    out     ADMUX,temp
    sbi     ADCSR,ADSC      ;begin ADC
ADC_n_PROGRSS3:
    sbic    ADCSR,ADSC      ;look to see if ADC is done
    rjmp    ADC_n_PROGRSS3
    in      test1,ADCL
    in      test2,ADCH
    tst     test2
    brne    RST_FLAG
    subi    test1,0x01      ;no subtract off the 10mV threshold
    brcs    DEC_TFLAG       ;if the voltage is less than 10mV, decrement Tflag
RST_FLAG:
    ldi     Tflag,0x08      ;It was good, so reset Tflag
    sbi     PORTB,1
    rjmp    I_MEAS          ;do it again
DEC_TFLAG:
    dec     Tflag           ;decrement Tflag
    breq    ERROR           ;if Tflag = 0 then goto ERROR
    rjmp    I_MEASi         ;there was an error so immediately check again
```

```
MEAS:
    ldi     temp,0x23       ;sets ADMUX   sets reference voltage and input line
    out     ADMUX,temp
    sbi     ADCSR,ADSC      ;begin ADC
ADC_n_PROGRSS1:
    sbic    ADCSR,ADSC      ;look to see if ADC is done
    rjmp    ADC_n_PROGRSS1
    in      test1,ADCH      ;get test results
    ldi     temp,0x22       ;set to convert test voltage
    out     ADMUX,temp
    sbi     ADCSR,ADSC      ;begin ADC
ADC_n_PROGRSS2:
    sbic    ADCSR,ADSC      ;look to see if ADC is done
    rjmp    ADC_n_PROGRSS2
    in      test2,ADCH
    sub     test1,test2     ;compare REF and test1
    brpl    GOODENOUGH      ;If the result is POSITIVE then jmp to GOODENOUGH
    mov     test2,test1     ;make a copy
    sub     test1,test2     ;subtract to zero
    sub     test1,test2     ;get the positive number
GOODENOUGH:
    subi    test1,0x02      ;----THIS IS THE DIFFERENCE VALUE--CHANGE TO INCREASE ACCURAC
    brcs    UP_TFLAG        ;if the test value is less than the difference value, its good
    dec     Tflag           ;The difference is too large, dec the count
    breq    ERROR           ;If Tflag equals zero, goto error
    rjmp    MEAS            ;test again
UP_TFLAG:
    inc     Tflag           ;the difference is small enough so increment counter
    sbrs    Tflag,3         ;Check to see if count has ended  (1000)
    rjmp    MEAS            ;if not, measure again
    ret                     ;if yes, return
```

Code for the Tiny Micro-Controller (continued)

```
ERROR:
      cli
      sbi    DDRB,1         ;set PortB1 as an output
      cbi    PORTB,1        ;clear PortB1 to turn the FET off
      cbi    PORTB,2        ;turn the red LED on
      rcall  DELAY          ;multiple delays
      rcall  DELAY
      rcall  DELAY
      rjmp   INIT           ;start over


DELAY:
      ldi    time2,0xff
DELAY1:
      ldi    time1,0xff
DELAY2:
      dec    time1
      brne   DELAY2
      dec    time2
      brne   DELAY1
      ret
```

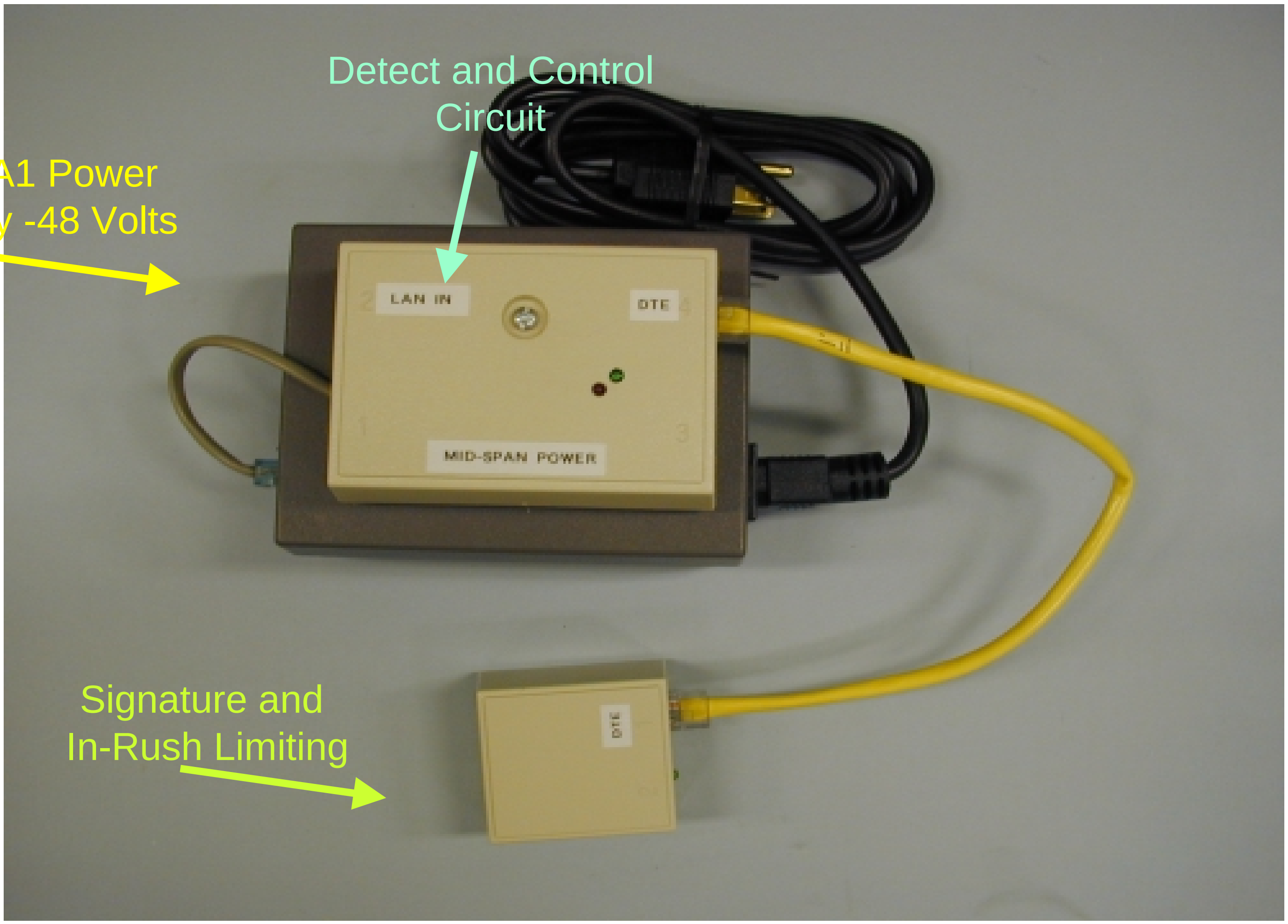
Evaluation Prototypes

- Four units available for evaluation
- Recently provided to
  - Roger Karam - Cisco
  - Dan Dove - HP
- Offered to others

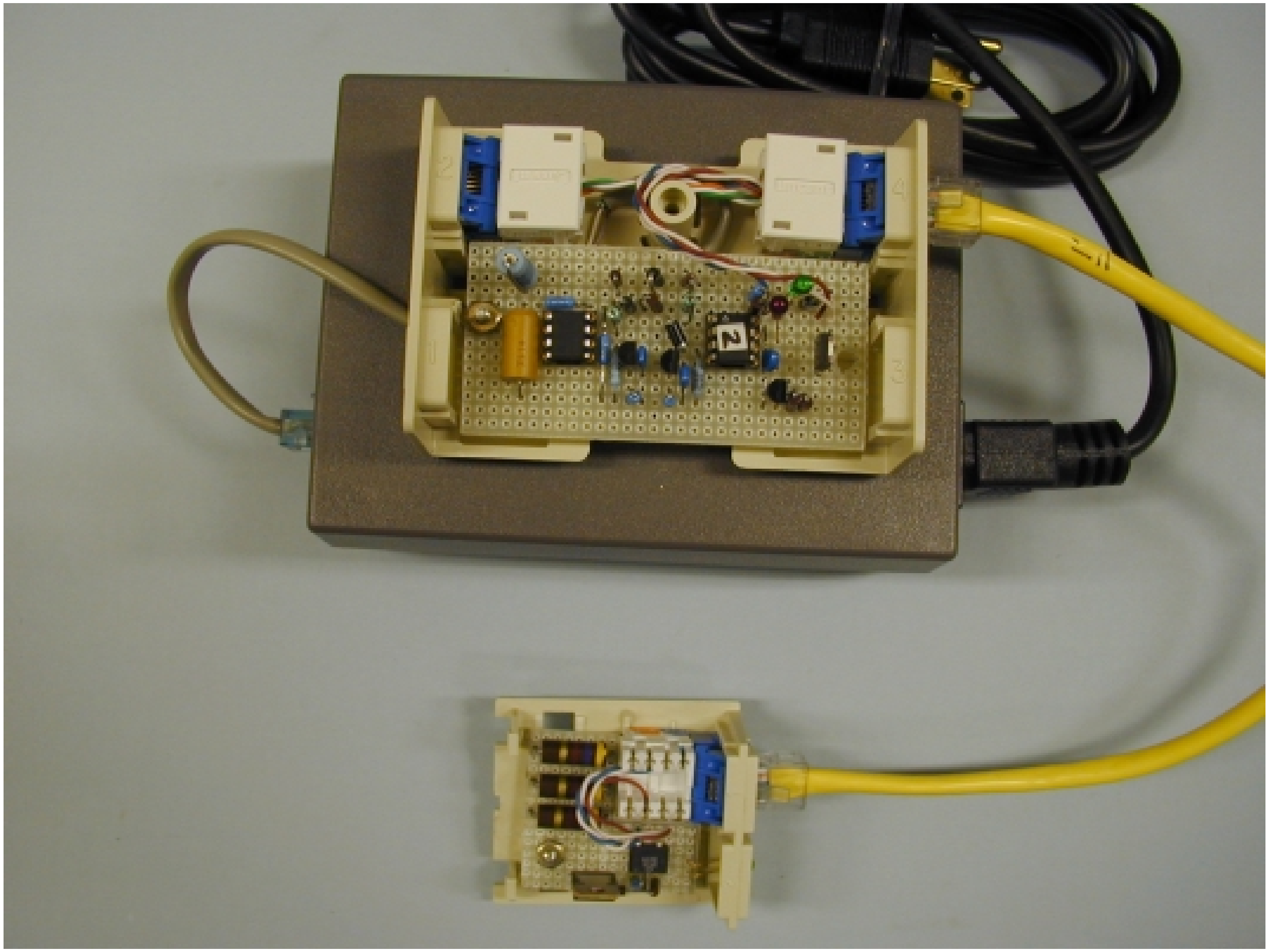
AVAYA communication

Lucent Technologies
Bell Labs Innovations

Prototype “Power Controller” and “Signature and In-Rush Limiting”



Prototype “Power Controller” and “Signature and In-Rush Limiting”



AVAYA communication

Lucent Technologies
Bell Labs Innovations

Intellectual Property

Neither Lucent Technologies or Avaya Communication has pursued or is pursuing Intellectual Property rights regarding the technology we have put forth in this proposal

Summary

- Updated detection protocol and signature
  - Second detect measurement at lower voltage added
  - Utilize voltage drop of two diodes (most likely present in polarity guard anyway) for discrimination against arbitrary pure resistances
- Strengths of this approach
  - Ensures lowest additional noise for Ethernet and future applications, since DC based
  - Robust in delivering power: Operational range not an issue
  - Robust against false detection: unusual signature of *25K ohms plus two diode drop* is offered power
  - Inherent safe against misapplication of power due to high resistance signature (25K ohms + 2 Diode drops)
    - ***If*** a mistake were ever made, current/power delivered would be extremely small (< 80 mW, corresponding to 30K ohms)

Summary (Continued)

- Strengths of this approach (continued)
  - Simple to specify, document, implement, integrate, troubleshoot, train, ….
  - Easily supports rich management (e.g., easy to monitor current/power levels ***per port***)
  - Amenable to mid-span and LAN switch implementations
    - Small space - even per port design small enough for LAN switch
    - Low cost
      - ***Can be integrated***, lowering costs
      - ***Can be shared*** across multiple Ports
  - Maintains maximum power to PE, power efficiency
    - Signature requires no more than standard polarity guard diode drops (two diodes), maximizing power to load
    - Easily supports precise control of power shut off for moderate *over voltages*; preserves maximum power to PE
    - Low power consumption in idle and detecting state(s)