mysticom

Technology to the Core

Revisiting CX4 Link Budget & Template

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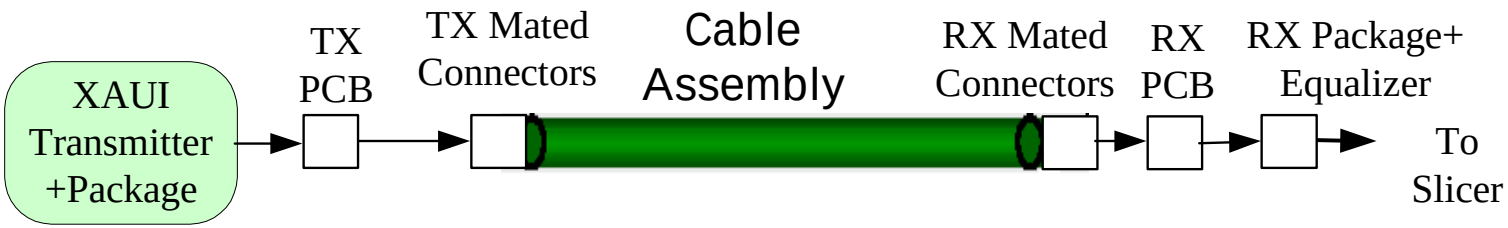
Overview

- Link budget - revisit
- Reflections Modeling
- Template results including reflections
- Summary and Conclusions

Link Budget

- Estimate eye opening at receiver by considering 3 data streams:
  - Low frequency 11111 00000 11111 …
  - Mid frequency 11 00 11 00 …
  - High frequency 101010 …
- Neglecting jitter, return loss and cross-talk

System Description



Link Budget Elements

- Assumption: Assembly loss comprised per Diminico's model
  - a=2.629E-1, b=3.408E-3, c=1.276E1, d=0.5

$$Insertion\_Loss = a\sqrt{f} + b \cdot f + \frac{c}{\sqrt{f}} + d$$

f in MHz

Insertion_Loss in dB

System Description Cont'd

- PBC insertion loss (assume 2")
  - a=6.5E-6, b=2E-10, c=3.3E-20, e=2.718

$$PCB\_Loss = \left(a\sqrt{f} + b\cdot f + c\cdot f^{2}\right)\cdot 2\cdot \log_{10}(e)$$

f in Hz

Insertion_Loss in dB

- Equalizer Transfer function

$$H(S) = K\frac{1+S\tau_1}{1+S\tau_2} \Rightarrow H(f) = 0.75\frac{1+j\frac{2\cdot f}{f_0}}{1+j\frac{3}{2}\frac{f}{f_0}}$$

$$where:\ f_0 = 1.56GHz$$

Link Budget for 15m
Worst Case Cable Assembly

CX4 Link Budget

Symbol rate	3.13E+09	Hz	
pi	3.141592654		
Preemphasis	0.35	52%	using CX4 definition for pre-emphasis
Cable length	**15**	Meters	Assume Chris's Model

Loss[dB]

Point in Path	Flow	Fmid	Fhigh
	3.125E+08	7.813E+08	1.563E+09
Tx package	0	-0.13	-2
Preemphasis	-5.15	-2.1	0
TX PCB	0.157	0.311	0.565
Cable Assembly	-6.93	-10.97	-16.54
RX PCB	0.157	0.311	0.565
Reflections Margin	-2.0	-2.0	-2.0
Equalizer	-3	-2	0
Total Insertion Loss [dB]	-16.8	-16.6	-19.4

Eye opening at receiver input

Launch voltage	Flow	Fmid	Fhigh
1200	174	178	128
1000	145	148	107
750	109	111	80

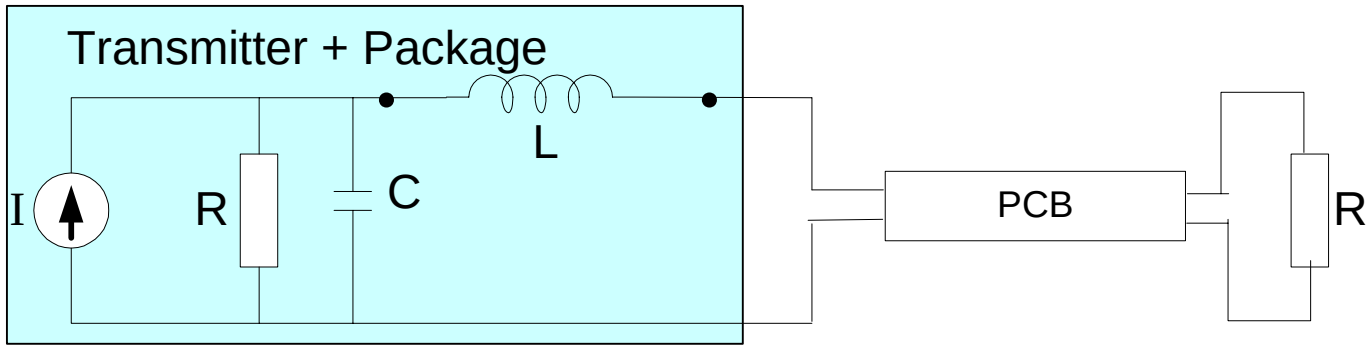
Observation 1

- Using only pre-emphasis an input sequence of

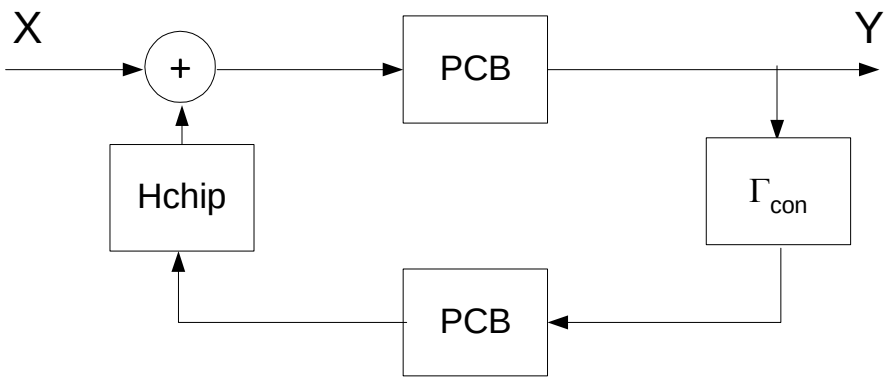
  101010… has marginal eye-opening

- When jitter, cross-talk and reflections accounted for,
  - one probably can not overcome a 15m worst case cable assembly with pre-emphasis only
  - Require both pre-emphasis and equalizer
  - Equalizer needs to have some gain (~3dB @1.56GHz)

Reflections Modeling



Simplified transmitter + PCB model



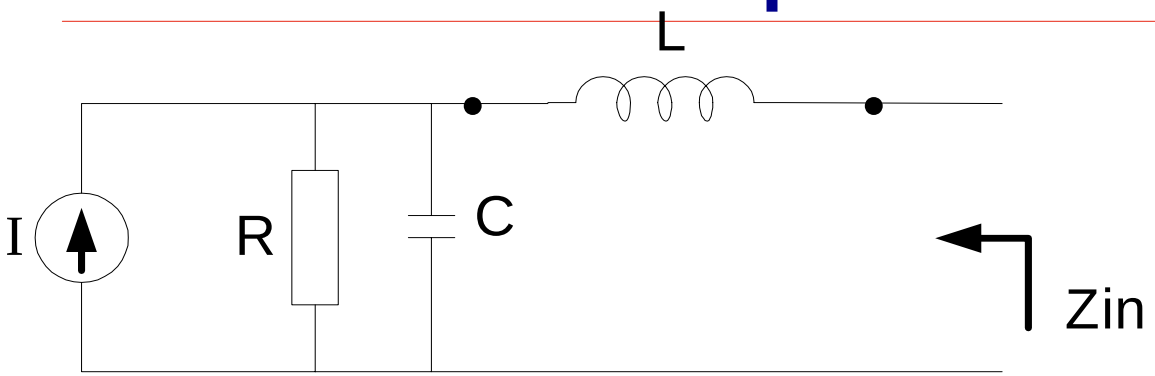
$$\frac{Y}{X} = \frac{PCB}{1 - \Gamma_{con}(PCB)^2 H_{chip}}$$

Simplified model for accounting for reflection effects

Reflections Modeling – Cont'd

- Connector Return Loss
  - Initially taken to be a frequency flat reflection having attenuation of gama.
  - In next step, frequency selectivity of reflection will be based on cable assembly RL limit provided by Chris Diminico in Raleigh
- Chip side return loss
  - Frequency selectivity on chip side is based on input impedance as seen from the PCB assuming the transmitter is modeled by a capacitor in parallel to a resistor.
  - In future can consider implications of introducing inductance as well

Return Loss at Chip

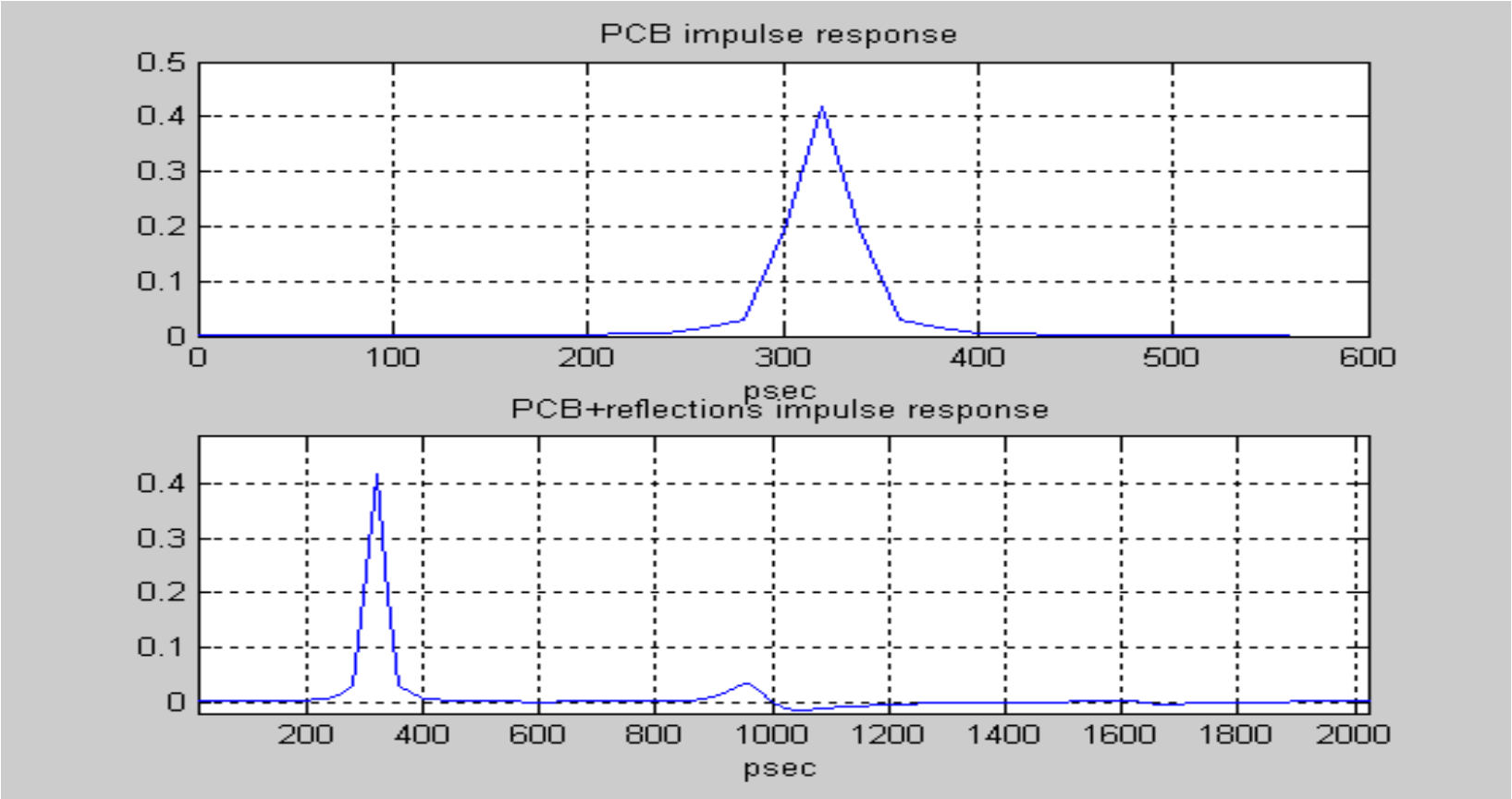


Neglecting the inductance: $$Z_{in}(\omega) \approx R \frac{1}{1 + j\omega RC}$$

$$RL(\omega) = -20\log_{10}\left(\left|\Gamma_{chip}(\omega)\right|\right) = -20\log_{10}\left(\frac{\omega\frac{RC}{2}}{\sqrt{1+\left(\omega\frac{RC}{2}\right)^2}}\right)$$

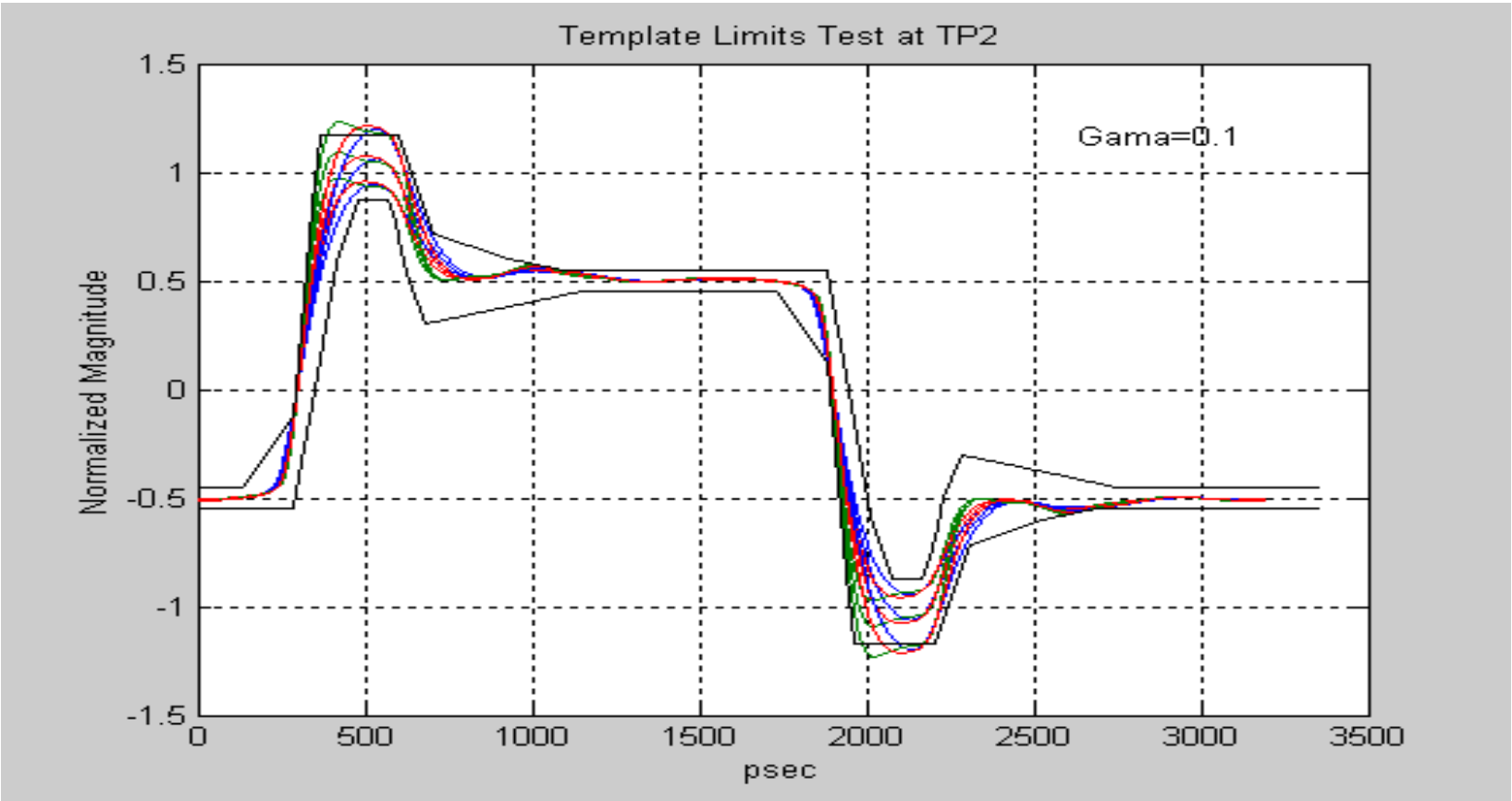
$$RL(0) \to \infty \qquad RL(\infty) \to 0 \qquad \omega = \frac{2}{RC} \to RL = 3dB$$

PCB impulse response : w/o reflections

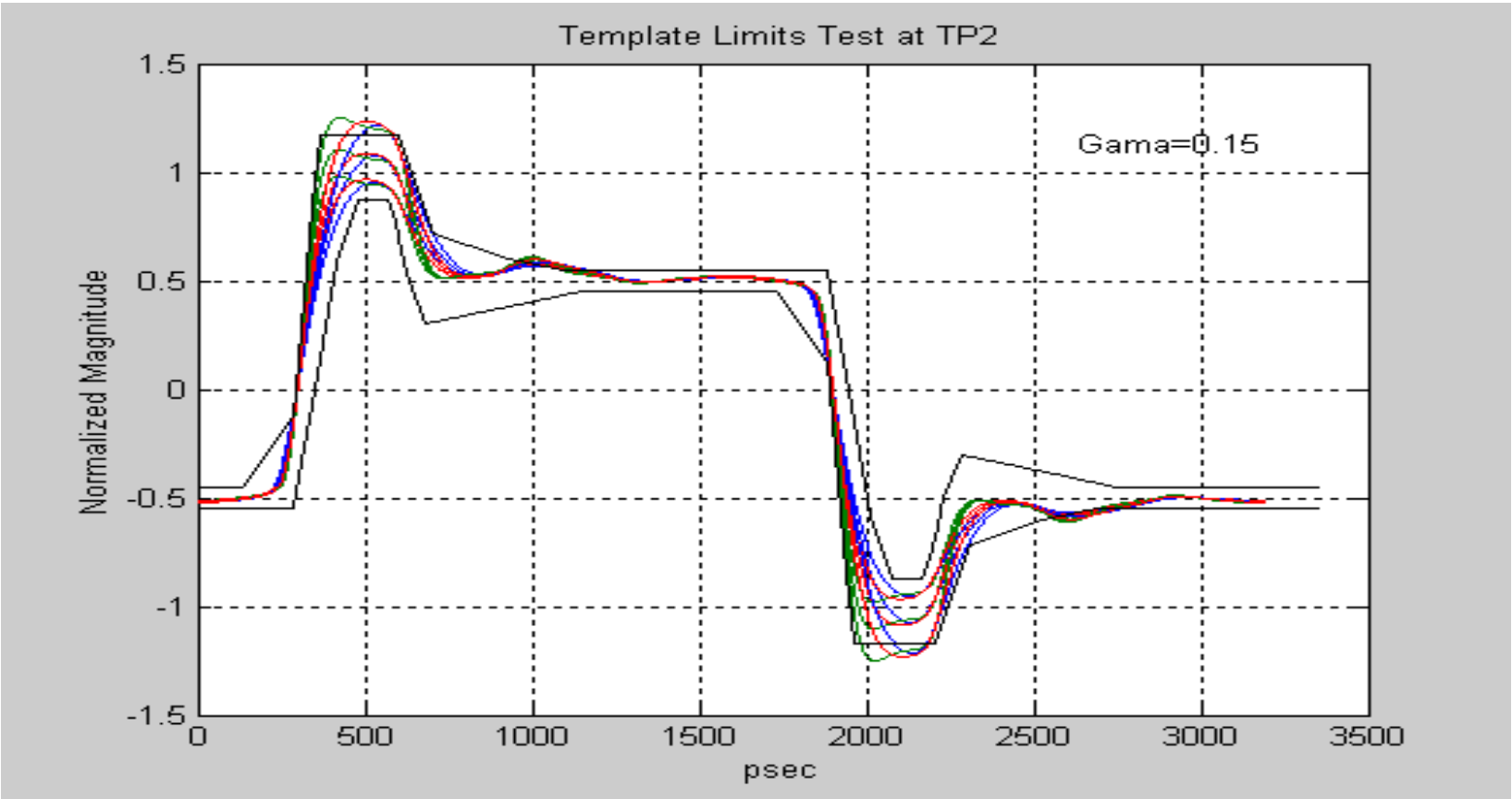


Sanity check A: 170ps/inch*2inch=340ps fits to main pulse @ 320ps
Sanity check B: (1+2)*320psec = 960ps fits to secondary pulse @960ps

Reflections Effect on Template



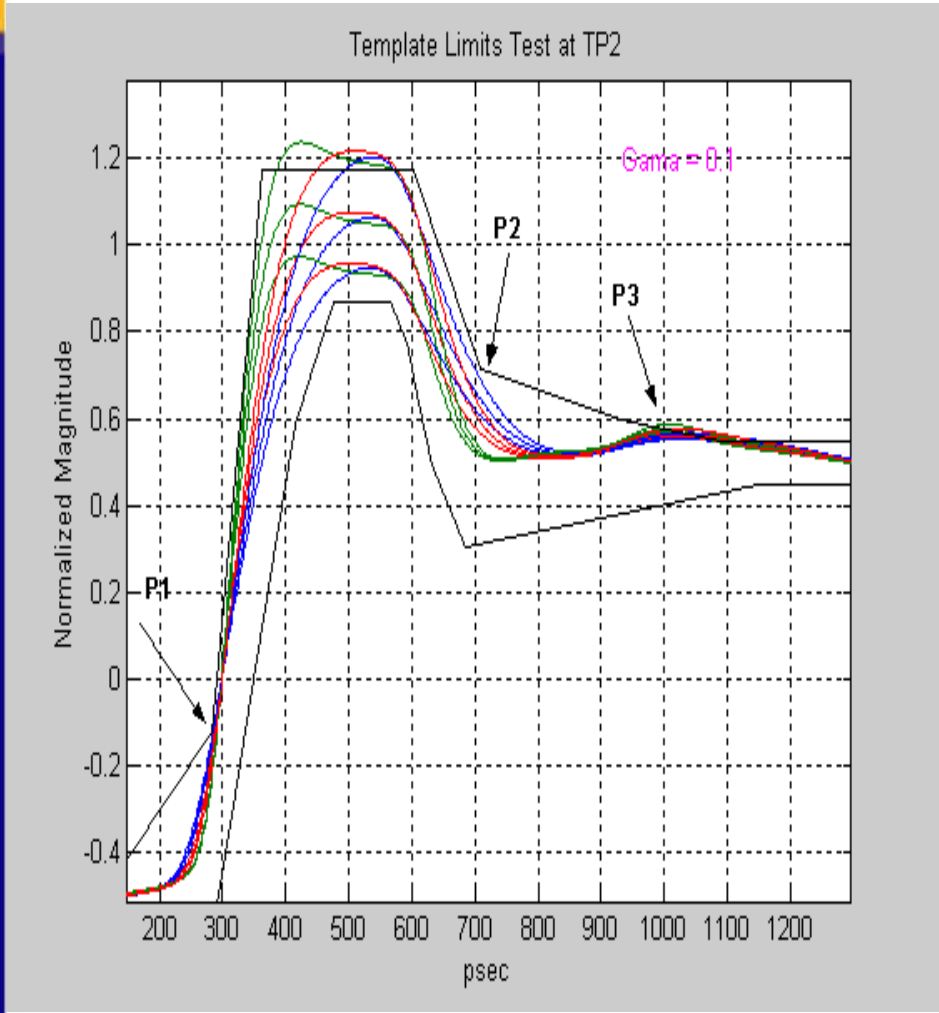
Reflections Effect on Template – Cont'd



Recommendations

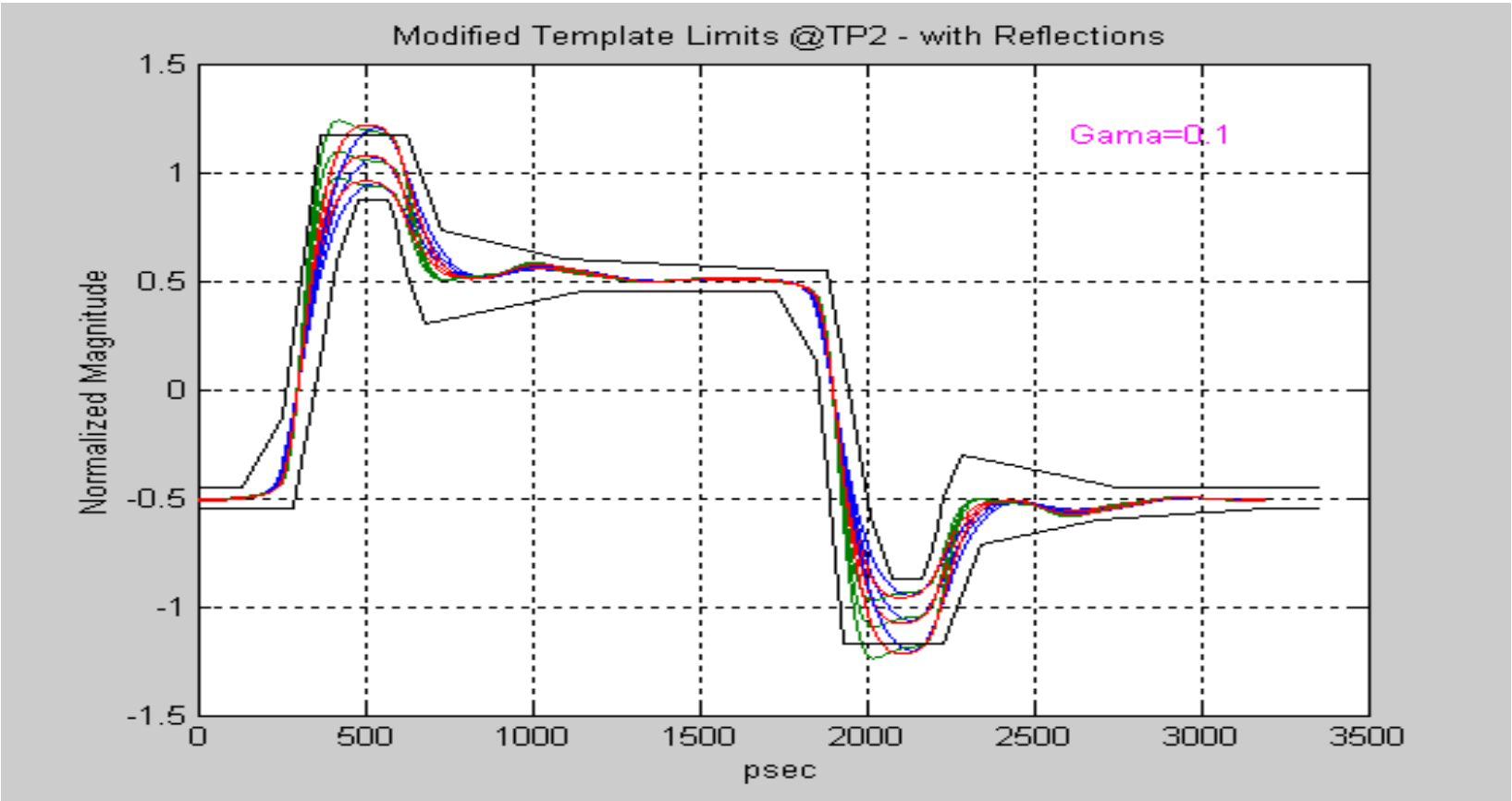
- Tweak the Upper & Lower limits around the problematic areas to accommodate the template with reflections.

Proposed modifications - Example

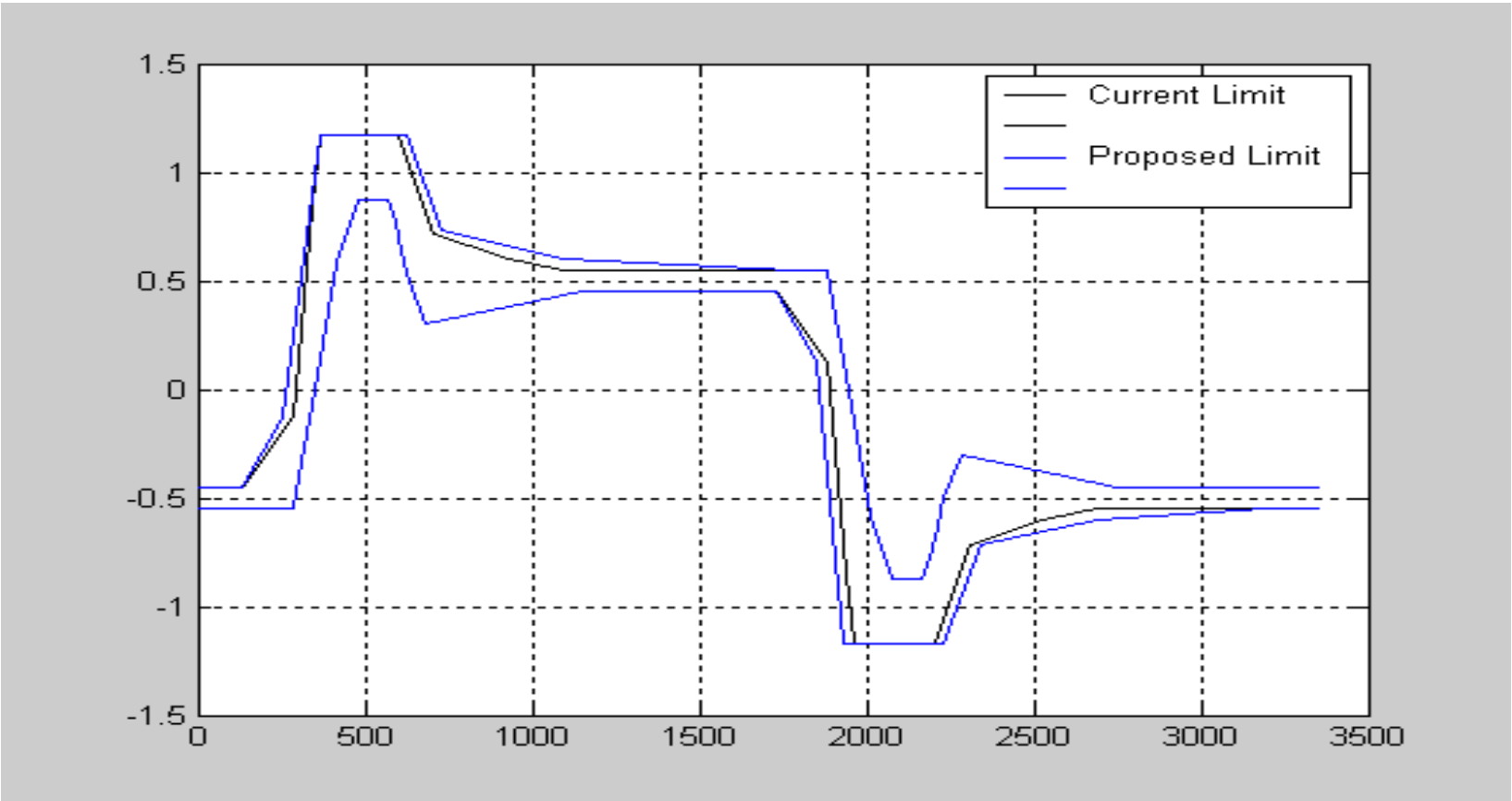


- P1: move to 260ps
- P2: move to 750ps
- P3: move from 0.55 to 0.6

Proposed Modified Template



Difference between Current and Proposed Templates

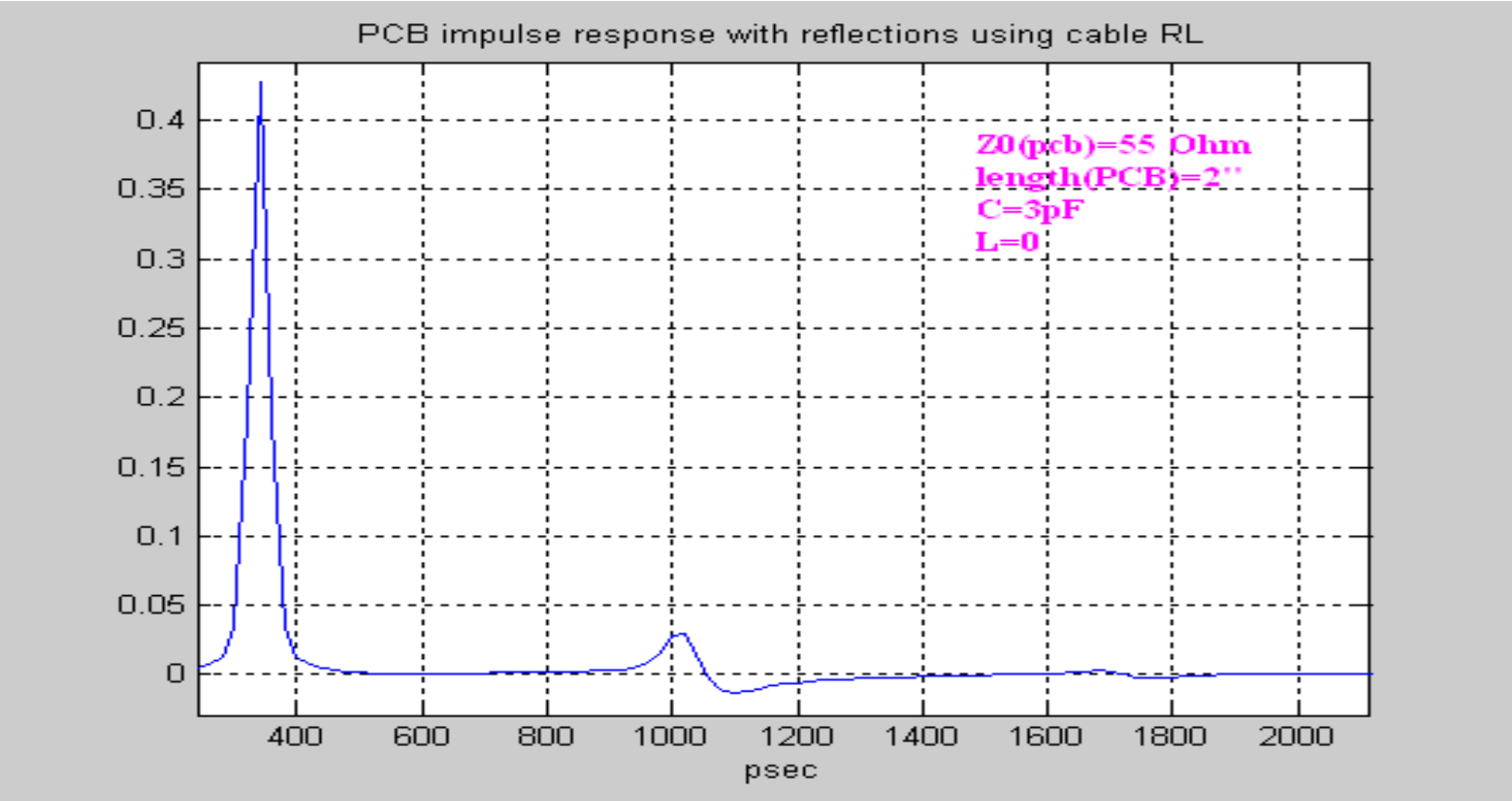


Proposed Modified Template – Cont'd

Template Data			
Time	Upper limit	Time	Lower limit
0	-0.450	0	-0.550
131	-0.450	189	-0.550
253	-0.125	287	-0.550
363	1.175	319	-0.266
451	1.175	349	0.000
622	1.175	414	0.586
729	0.735	477	0.870
1091	0.600	509	0.870
1789	0.550	565	0.870
1887	0.550	591	0.776
1919	0.266	611	0.635
1949	0.000	631	0.494
2014	-0.586	685	0.306
2077	-0.870	989	0.400
2109	-0.870	1149	0.450
2165	-0.870	1731	0.450
2191	-0.776	1853	0.125
2211	-0.635	1933	-1.175
2231	-0.494	2051	-1.175
2285	-0.306	2232	-1.175
2589	-0.400	2339	-0.715
2749	-0.450	2691	-0.600
3200	-0.450	3200	-0.550
3360	-0.450	3360	-0.550

Using Cable Assembly RL

Question: What will the PCB impulse response (including reflection) look like if we were to use cable assembly RL rather than flat response ?



Summary and Next Steps

- Revisited the link budget
- Effects of reflections on the transmit template were estimated
  - Require a slight modification of the template limits
  - Proposed modified template limits
- Next steps: refine the reflections model