

IEEE P803.2an Task Force Santa Clara, February '05

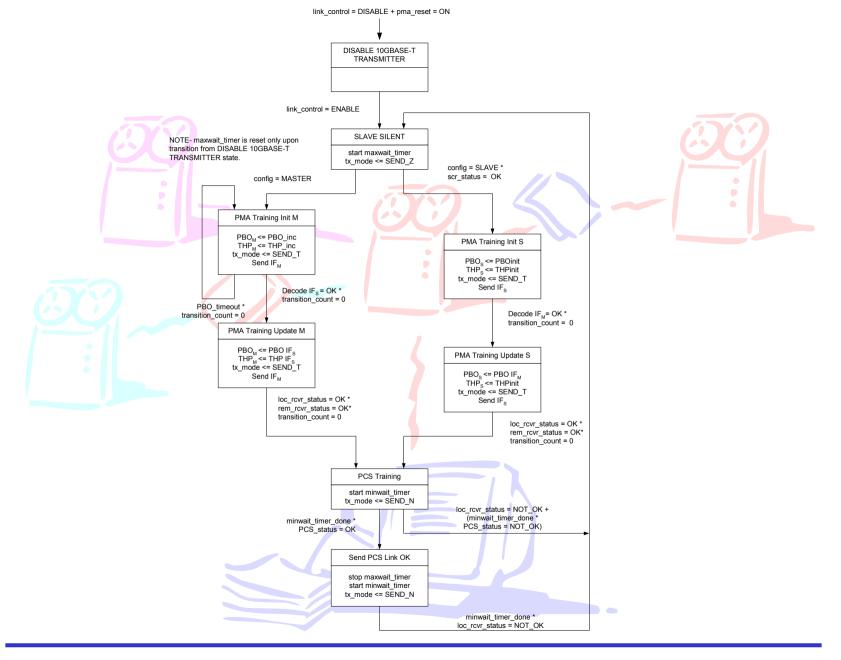
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# **Info Field Proposal**

- Info Field: 16 bytes
  - Start of Frame Delimiter: 4 bytes
    - BBA70000- minimum hamming distance of 7
  - Current TX setting: 1 byte
    - X, PBO(2:0), THP(3:0)
  - Next TX setting: 1 byte
    - X, PBO(2:0), THP(3:0)
  - Requested TX setting: 1 byte
    - X, PBO(2:0), THP(3:0)
  - Message Field: 1 byte
    - X(7:5),PBO\_increase (master only), loc\_rcvr\_status, trans\_to\_Training\_Update, trans\_to\_PCS\_Training, trans\_to\_slave\_silent
  - SNR Margin : 4 bits
    - SNR Margin in ½ dB steps from –2.5dB to +5dB
  - Transition Counter: 12 bits
    - Trans\_counter(11:0): # of frames until next transition
  - Reserved Field: 4 bytes
    - For future use or vendor field.
  - CRC16: 2bytes  $(x+1)(x^{15}+x+1)$

## **PHY Control State Diagram**

- Issues:
  - Missing timer
    - The Master must pass through Slave Silent to start the maxwait timer.
  - Unused timers
    - Remove the timers in PMA Training states
      - The transitions have implicit handshaking.
  - Missing transition
    - There is no exit from PCS Training unless PCS\_status=OK
  - Endless loops
    - Loops at PMA Training Update are not necessary



## **PHY Control State Diagram**

- Initial settings
- Master
  - PBO\_inc
    - 1 of 3 PBO settings for 0m, short and medium cable lengths, the master will increment the setting after PBO timeout (described in Tellado\_1\_0205)
  - THP\_inc
    - 1 of 3 THP settings for 0m (bypass), short and medium cable lengths, the master will increment the setting after PBO timeout (described in Tellado\_1\_0205) or optionally (as set during autoneg) stays in bypass.
- Slave
  - PBOinit
    - The slave will estimate the cable length and respond with the appropriate PBO setting.
  - THPinit
    - The slave will estimate the cable length and respond with the appropriate THP setting.

### **Link Monitor**

#### Issues

- Link fail timer
  - The link\_fail\_inhibit\_timer (pg 36 ln 32) will timeout in 750ms.
  - If the state machine has not transitioned to Link Up, then the link has failed and autoneg starts over.
  - If the time difference between PHY's entering startup is 192ms (pg 36 ln 46) then only 558ms is available for startup.
  - I propose to set link\_status= OK as soon as the training pattern has been detected.
  - The maxwait\_timer is responsible for timing the startup and setting link\_status=FAIL if startup has not completed.
- Transitions to Link Down
  - The current diagram does not match the text (PCS\_status vs. loc rcvr status.
  - The diagram allows an immediate transition to Link Down if PCS\_status=NOT\_OK in the Hysteresis state.
  - I propose that the transition to Link Down occur only after the maxwait\_timer has timed out and either PCS\_status = NOT\_OK or loc\_rcvr\_status = NOT\_OK.

### **Link Monitor**

### Timers

- maxwait\_timer
  - Limits the time allowed in the Training states before the link has failed.
  - 1000BASE-T was 750ms
  - TBD- needs more study
    - Range could be 750ms to seconds
- Minwait\_timer
  - Sets the minimum amount of time in the PCS Training state
  - ie. the minimum time after transitioning from 2PAM to 16PAM until ready for Link Up
  - Proposal: 1ms (~3000 frames)
    - Equal to 8 x LFER monitor timers

### **Proposed Link Monitor**

